SUMMARY

- Circuits are important in electrical engineering because they process signals that carry energy and information. A **circuit** is an interconnection of electrical devices. A **signal** is an electrical current or voltage that carries energy or information. An **interface** is a pair of accessible terminals at which signals may be observed or specified.
- This book defines overall course objectives at the analysis, design, and evaluation levels. In **circuit analysis** the circuit and input signals are given and the object is to find the output signals. The object of **circuit design** is to devise one or more circuits that produce prescribed output signals for given input signals. The **evaluation** problem involves appraising alternative circuit designs using criteria such as cost, power consumption, and parts count.
- Charge (q) and energy (w) are the basic physical variables involved in electrical phenomena. Current (i), voltage (v), and power (p) are the derived variables used in circuit analysis and design. In the SI system, charge is measured in coulombs (C), energy in joules (J), current in amperes (A), voltage in volts (V), and power in watts (W).
- **Current** is defined as dq/dt and is a measure of the flow of electrical charge. **Voltage** is defined as dw/dq and is a measure of the energy required to move a small charge from one point to another. **Power** is defined as dw/dt and is a measure of the rate at which energy is being transferred. Power is related to current and voltage as $p = vi$.
- The **reference marks** (arrows and plus/minus signs) assigned to a device are reference directions, not indications of the way a circuit responds. The actual direction of the response is determined by comparing the reference direction and the algebraic sign of the answer found by circuit analysis using physical laws.
- Under the **passive sign convention**, the current reference arrow is directed toward the terminal with the positive voltage reference mark. Under this convention, the device power is positive when it absorbs power and is negative when it delivers power. When current and voltage have the same (opposite) algebraic signs, the device is absorbing (delivering) power.

PROBLEMS

ERO 1–1 ELECTRICAL SYMBOLS AND UNITS (SECT. 1–2)

Given an electrical quantity described in terms of words, scientific notation, or decimal prefix notation, convert the quantity to an alternate description.
See Exercise 1–1

1–1 Write the following statements in symbolic form:
- **(a)** twelve milliamps
- **(b)** four hundred fifty five kilohertz
- **(c)** two hundred picoseconds
- **(d)** five megawatts

1–2 Express the following quantities using appropriate engineering prefixes (i.e., state the numeric to the nearest standard prefix).
- **(a)** 0.022 volts
- **(b)** 23×10^{-9} farads
- **(c)** 56,000 ohms
- **(d)** 7.52×10^{5} joules
- **(e)** 0.000235 henrys

1–3 An ampere-hour (Ah) meter measures the time-integral of the current in a conductor. During an 8-hour period a certain meter records 3300 Ah. Find the number of coulombs that flowed through the meter during the recording period.

1–4 Commercial electrical power companies measure energy consumption in kilowatt-hours, denoted kWh. One kilowatt-hour is the amount of energy transferred by 1 kW of power in a time period of 1 hour. During a one-month time period, a power company billing statement reports a user's total energy usage to be 2128 kWh. Determine the number of joules used during the billing period.

1–5 Fill in the blanks in the following statements.

(a) To convert capacitance from microfarads to picofarads, multiply by ________.

(b) To convert resistance from kilohms to megohms, multiply by ________.

(c) To convert current from amperes to milliamperes, multiply by ________.

(d) To convert power from watts to megawatts, multiply by ________.

ERO 1–2 CIRCUIT VARIABLES (SECT. 1–3)

Given any two of the three signal variables (i, v, p) or the two basic variables (q, w), find the magnitude and direction (sign) of the unspecified variables.
See Examples 1–1, 1–2, 1–3 and Exercises 1–1, 1–2, 1–3

1–6 The charge flowing through a device is $q(t) = 3t - 2$ mC. Find the current through the device.

1–7 The charge flowing through a device is $q(t) = 20e^{-3t}$ μC. Find the current through the device..

1–8 Figure P1–8 shows a plot of the net positive charge flowing in a wire versus time. Sketch the corresponding current during the same time period.

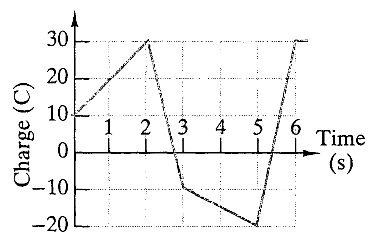


FIGURE P1–8

1–9 The current through a device is $i(t) = 3t^2$ A. Find the total charge that flowed through the device between $t = 0$ and $t = 2$ s.

1–10 The current through a device is $i(t) = 3e^{-2t}$ A. Find the total charge that flowed through the device between $t = 0$ and $t = 0.1$ s.

1–11 For $t \le 5$ s the current through a device is $i(t) = 10$ A. For $5 < t \le 10$ s the current is $i(t) = 20 - 2t$ A, and it is zero for $t > 10$. Sketch $i(t)$ versus time and find the total charge through the device between $t = 0$ s and $t = 10$ s.

1–12 The charge flowing through a device is $q(t) = 1 - e^{-2000t}$ μC. Sketch the current through the device versus time for $t > 0$.

1–13 The 12-V automobile battery in Figure P1–13 has an output capacity of 200 ampere-hours (Ah) when connected to a headlamp that absorbs 50 watts of power. Assume that the battery voltage is constant.

(a) Find the current supplied by the battery.

(b) How long can the battery power the headlight?

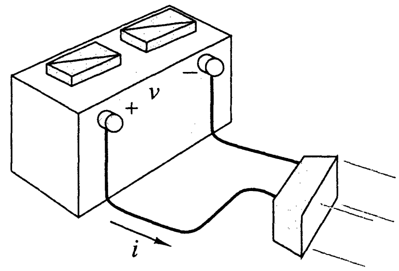


FIGURE P1–13

1–14 An incandescent lamp absorbs 75 W when connected to a 120-V source.

(a) Find the current through the lamp.

(b) Find the cost of operating the lamp for 8 hours when electricity costs 6.8 cents/kW-hr.

1–15 A total charge of 50 ampere-hours is supplied to a 12-V battery during recharging. Determine the number of joules supplied to the battery. Assume that battery voltage is constant.

1–16 The voltage across a device is 25 V when the current through the device is $i(t) = 3e^{-2t}$ A. Find the total energy delivered to the device between $t = 0$ and $t = 0.5$ s.

1–17 When illuminated the i–v relationship for a photocell is $i = e^{v} - 10$ A. Calculate the device power and state whether the device is absorbing or delivering power when $v = -3$ V. Repeat for $v = 1.5$ V and 3 V.

1–18 Using the passive sign convention, the current through and voltage across a two-terminal device are $i = 1 - 2e^{-t}$ A and $v = 25$ V. Calculate the device power and state whether the device is absorbing or delivering power when $t = 0.5$ s, $t = 1$ s, and $t = 10$ s.

1–19 The maximum power the device can dissipate is 0.25 W. Determine the maximum current allowed by the device power rating when the voltage is 50 V.

1–20 A laser produces 5-kW bursts of power that last 20 ns. If the burst rate is 40 bursts per second, what is the average power in the laser's output?

1–21 Two electrical devices are connected as shown in Figure P1-21. Using the reference marks shown in the figure, find the power transferred and state whether the power is transferred from A to B or B to A when

(a) $v = +33$ V and $i = -2.2$ A

(b) $v = -12$ V and $i = -1.2$ mA

(c) $v = +37.5$ V and $i = +40$ mA

(d) $v = -15$ V and $i = -43$ mA

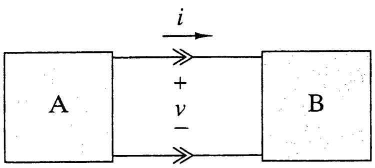


FIGURE P1–21

1–22 Figure P1–22 shows an electric circuit with a voltage and a current variable assigned to each of the six devices. The device signal variables are observed to be as follows:

Device 1, $v = 15$ V, $i = -1$ A, and $p = ?$
Device 2, $v = 5$ V, $i = ?$, and $p = 5$ W
Device 3, $v = ?$ V, $i = 0.5$ A, and $p = 5$ W
Device 4, $v = 4$ V, $i = 0.5$ A, and $p = ?$
Device 5, $v = ?$ V, $i = 3$ A, and $p = 18$ W
Device 6, $v = ?$ V, $i = -2.5$ A, and $p = -15$ W

Find the unknown signal variable associated with each device and state whether the device is absorbing or delivering power. Use the power balance to check your work.

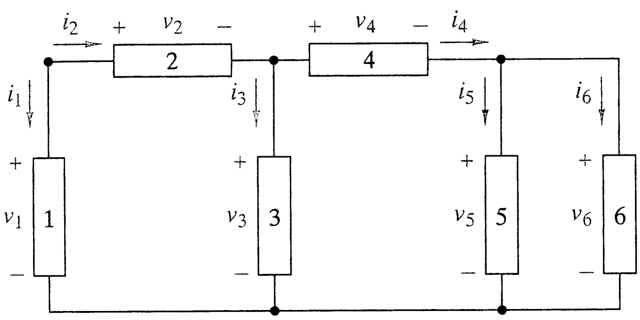


FIGURE P1–22

1–23 Figure P1–22 shows an electric circuit with a voltage and a current variable assigned to each of the six devices. The device signal variables are observed to be as follows:

Device 1, $v = 30$ V, $i = -2$ A, and $p = ?$
Device 2, $v = 10$ V, $i = ?$, and $p = 20$ W
Device 3, $v = 20$ V, $i = ?$, and $p = 20$ W
Device 4, $v = 8$ V, $i = 1$ A, and $p = ?$
Device 5, $v = ?$ V, $i = -5$ A, and $p = -60$ W
Device 6, $v = 12$ V, $i = 6$ A, and $p = ?$ W

Find the unknown signal variable associated with each device and state whether the device is absorbing or delivering power. Use the power balance to check your work.

1–24 Using the passive sign convention, the voltage across a device is $v(t) = 5\cos(10t)$ V and the current through the device $i(t) = 0.5\sin(10t)$ A. Calculate the device power at $t = 0.2$ s and $t = 0.4$ s and state whether the device is absorbing or delivering power.

1–25 For $t \geq 0$ the voltage across and current through a device are $v(t) = 10(1 - e^{-25t})$ V and $i(t) = 0.5e^{-25t}$ A. Find the energy delivered to the device between $t = 0$ and $t = 1$ s.

INTEGRATING PROBLEMS

1–26 Power Ratio in dB

In complete darkness the voltage across and current through a two-terminal light detector are +5.6 V and +8 nA. In full sunlight the voltage and current are +0.9 V and +4 mA. Express the light/dark power ratio of the device in decibels (dB), where the power ratio in dB is

$$P_{dB} = 10 \log_{10} (p_2/p_1).$$

1–27 AC to DC Converter

A manufacturer's data sheet for the converter in Figure P1-27 states that the AC input voltage is 120 V, the DC output is 24 V, and the efficiency is 82% when the output power is 200 W. Find the input and output currents.

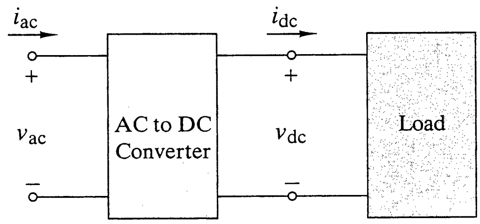


FIGURE P1–27

1–28 Storage Battery Efficiency

The ampere-hour efficiency of a storage battery is the ratio of its ampere-hour output to the ampere-hour input required to recharge the battery. A certain 24-V battery has a rated output of 400 ampere-hours. When the battery is completely drained, a battery charger must deliver 75 A for 6 hours to recharge the battery. Assume that the battery voltage is constant.

(a) Determine the ampere-hour efficiency of the battery.
(b) Determine the number of joules required to recharge the battery.

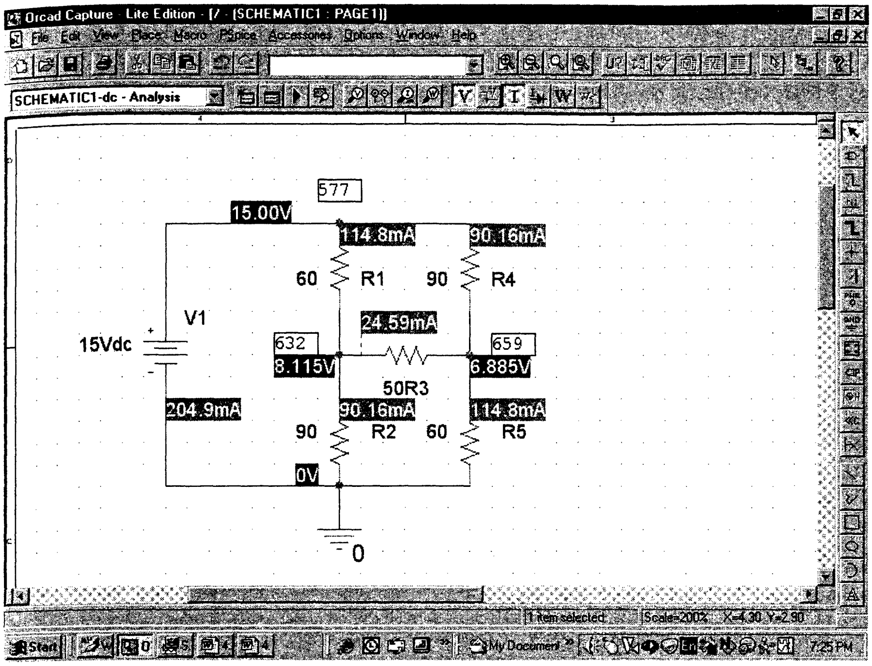


FIGURE 2-81

SUMMARY

- An **electrical device** is a real physical entity, while a **circuit element** is a mathematical or graphical model that approximates major features of the device.
- Two-terminal circuit elements are represented by a circuit symbol and are characterized by a single constraint imposed on the associated current and voltage variables.
- An **electrical circuit** is an interconnection of electrical devices. The interconnections form nodes and loops.
- A **node** is an electrical juncture of the terminals of two or more devices. A **loop** is a closed path formed by tracing through a sequence of devices without passing through any node more than once.
- Device interconnections in a circuit lead to two connection constraints: **Kirchhoff's current law (KCL)** states that the algebraic sum of currents at a node is zero at every instant; and **Kirchhoff's voltage law (KVL)** states that the algebraic sum of voltages around any loop is zero at every instant.
- A pair of two-terminal elements are connected in **parallel** if they form a loop containing no other elements. The same voltage appears across any two elements connected in parallel.
- A pair of two-terminal elements are connected in **series** if they are connected at a node to which no other elements are connected. The same current exists in any two elements connected in series.
- Two circuits are said to be **equivalent** if they each have the same *i–v* constraints at a specified pair of terminals.

- Series and parallel equivalence and voltage and current division are important tools in circuit analysis and design.
- **Source transformation** changes a voltage source in series with a resistor into an equivalent current source in parallel with a resistor, or vice versa.
- **Circuit reduction** is a method of solving for selected signal variables in ladder circuits. The method involves sequential application of the series/parallel equivalence rules, source transformations, and the voltage/current division rules. The reduction sequence used depends on the variables to be determined and the structure of the circuit and is not unique.

PROBLEMS

ERO 2–1 ELEMENT CONSTRAINTS (SECT. 2–1)

Given a two-terminal element with one or more electrical variables specified, use the element i–v constraint to find the magnitude and direction of the unknown variables.
See Example 2–1

2–1 Figure P2–1 shows a general two-terminal element with voltage and current reference marks assigned. Find the unknown electrical variables when the element is:

(a) A linear 5-kΩ resistor with $v = 50$ V.

(b) An ideal 10-mA current source with the arrow directed upward and $p = 30$ mW.

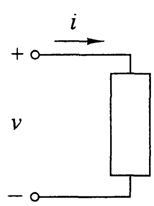


FIGURE P2–1

2–2 Figure P2–1 shows a general two-terminal element. Determine as much as you can about the element value and signal variables when the element is:

(a) An ideal 15-V voltage source with the plus terminal at the top and $i = 5$ mA.

(b) An ideal switch with $i = 20$ A.

2–3 When the voltage across a linear resistor is 12 V the current is 3 mA. Find the conductance of the resistor.

2–4 The design guidelines for a circuit call for using only ¼-W resistors. The maximum voltage level in the circuit is known to be 12 V. Determine the smallest allowable value of resistance.

2–5 The i–v measurements for an unknown element are as follows: $i = 7.5$ mA @ $v = 15$ V, $i = 4.3$ mA @ $v = 8.6$ V, $i = -4$ mA @ $v = -8$ V. Use these measurements to estimate the current through the element when $v = -15$ V. Is the device linear?

2–6 The i–v relationship of a nonlinear resistor is $v = 75i + 0.2i^3$.

(a) Calculate v and p for $i = \pm0.5, \pm1, \pm2, \pm5$, and ±10 A.

(b) If the operating range of the device is limited to $|i| < 0.5$ A, what is the maximum error in v when the device is approximated by a 75-Ω linear resistance?

2–7 A certain 10-kΩ resistor dissipates 12 mW. Find the current through the device.

2–8 A certain type of film resistor is available with resistance values between 10 Ω and 100 MΩ. The maximum ratings for all resistors of this type are 400 V and ½ W. Show that the voltage rating is the controlling limit when $R > 320$ kΩ, and that the power rating is the controlling limit when $R < 320$ kΩ.

2–9 Figure P2–9 shows the circuit symbol for a class of two-terminal devices called diodes. The i–v relationship for a p–n junction diode is

$$i = 2 \times 10^{-16}(e^{40v} - 1)$$

(a) Use this equation to find i and p for $v = 0, \pm0.1, \pm0.2, \pm0.4$, and ±0.8 V. Use these data to plot the i–v characteristic of the element.

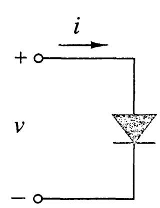


FIGURE P2–9

(b) Is the diode linear or nonlinear, bilateral or nonbilateral, and active or passive?
(c) Use the diode model to predict i and p for $v = 5$ V. Do you think the model applies to voltages in this range? Explain.
(d) Repeat (c) for $v = -5$ V.

2–10 The resistance of a device is given by

$$R = 0.3T_C + 100$$

where T_C is the device temperature in degrees Celsius. Find the voltage across the device when the current is 1 mA and the temperature is 400°C.

ERO 2–2 CONNECTION CONSTRAINTS (SECT. 2–2)

Given a circuit composed of two-terminal elements:
(a) Identify nodes and loops in the circuit.
(b) Identify elements connected in series and in parallel.
(c) Use Kirchhoff's laws (KCL and KVL) to find selected signal variables.
See Examples 2–4, 2–5, 2–6 and Exercises 2–1, 2–2, 2–3, 2–4, 2–5

2–11 For the circuit in Figure P2–11,
(a) Identify the nodes and at least two loops.
(b) Identify any elements connected in series or in parallel.
(c) Write KCL and KVL connection equations for the circuit.
(d) If $i_1 = 6$ mA and $i_2 = -4$ mA, find the other element currents.

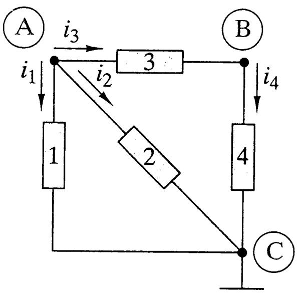


FIGURE P2–11

2–12 The currents in Figure P2–11 are observed to be $i_1 = 20$ mA and $i_3 = -30$ mA. Find the other element currents in the circuit.

2–13 For the circuit in Figure P2–13,
(a) Identify the nodes and at least three loops in the circuit.
(b) Identify any elements connected in series or in parallel.
(c) Write KCL and KVL connection equations for the circuit.
(d) If $v_3 = -8$ V, $v_4 = -8$ V, and $v_5 = 9$ V, find the other element voltages.

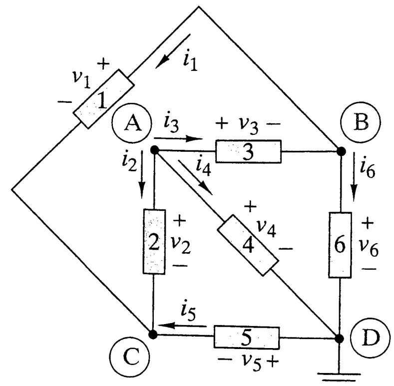


FIGURE P2–13

2–14 In Figure P2–13 $v_1 = -8$ V, $v_4 = 8$ V, and $v_6 = 6$ V. Find the other element voltages.

2–15 The circuit in Figure P2–15 is organized around the three signal lines A, B, and C.
(a) Identify the nodes and at least three loops in the circuit.
(b) Write KCL connection equations for the circuit.
(c) If $i_3 = 15$ mA, $i_4 = -12$ mA, and $i_5 = 5$ mA, find the other element currents.

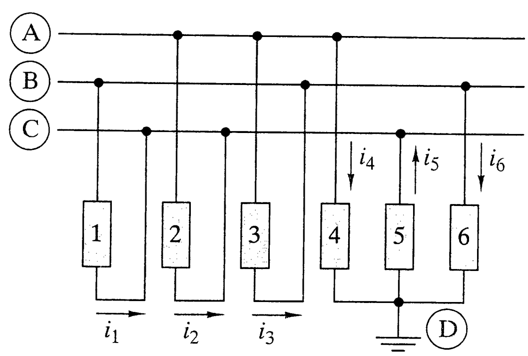


FIGURE P2–15

2–16 In Figure P2–16 $v_1 = 5$ V, $v_3 = -10$ V, and $v_4 = 10$ V. Find v_2 and v_5.

2–17 In the circuit in Figure P2–17 $i_1 = 2$ A, $i_2 = -5$ A, and $i_3 = 4$ A. Use KCL to find i_4 and i_5.

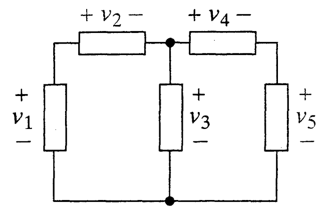


FIGURE P2–18

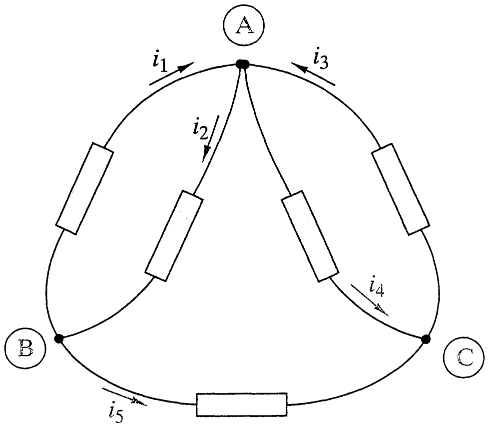


FIGURE P2–17

2–18 The connection equations for a certain circuit are

$$v_1 - v_2 - v_3 = 0 \qquad i_1 + i_2 = 0$$
$$v_3 + v_4 + v_5 = 0 \qquad -i_2 + i_3 - i_4 = 0$$
$$i_4 - i_5 = 0$$
$$-i_1 - i_3 + i_5 = 0$$

Draw the circuit diagram and indicate the reference marks for the element voltages and currents.

2–19 The incident matrix $A = [a_{ij}]$ of a circuit has one row for each node and one column for each element. If the jth element is not connected to the ith node, then $a_{ij} = 0$. If the jth element is connected to the ith node, then $a_{ij} = \pm 1$, where the plus sign applies if the current reference direction is into the node and the minus sign applies if it is away from the node. The incident matrix of a circuit is

$$A = \begin{bmatrix} -1 & +1 & 0 & -1 & 0 \\ 0 & -1 & -1 & 0 & +1 \\ +1 & 0 & +1 & +1 & -1 \end{bmatrix}$$

Draw the circuit diagram and indicate the reference directions for currents and voltages using the passive sign convention.

2–20 Given the definition in Problem 2–19, construct the incident matrix for the circuit corresponding to the connection equations in Problem 2–18.

ERO 2–3 COMBINED CONSTRAINTS (SECT. 2–3)

Given a circuit consisting of independent sources and linear resistors, use the element constraints and connection constraints to find selected signal variables.
See Examples 2–7, 2–8, 2–9, 2–10 and Exercise 2–6

2–21 Find v_x and i_x in Figure P2–21.

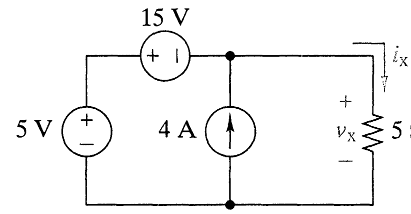


FIGURE P2–21

2–22 First use KVL to find the voltage across each resistor in Figure P2–22. Then use Ohm's law and KCL to find the current through every element, including the voltage sources.

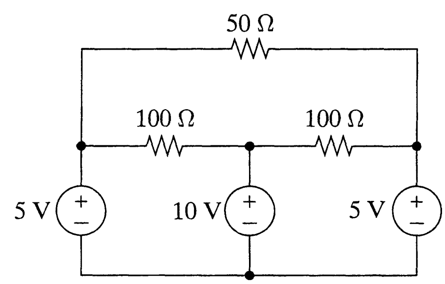


FIGURE P2–22

2–23 Find v_x in Figure P2–23.

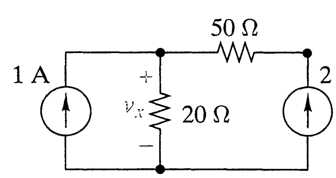


FIGURE P2–23

2–24 Figure P2–24 shows a subcircuit connected to the rest of the circuit at four points.

(a) Use element and connection constraints to find v_x and i_x.

(b) Show that the sum of the currents into the rest of the circuit is zero.

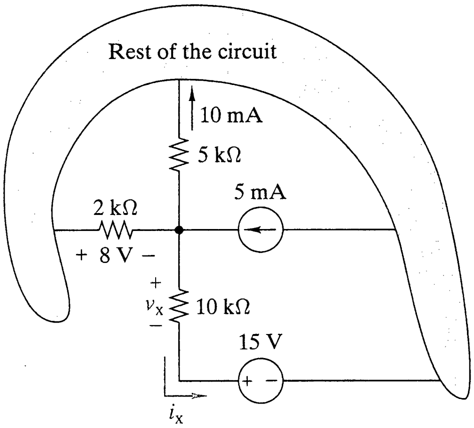


FIGURE P2–24

2–25 The circuit in Figure P2–25 is a model of the feedback path in an electronic amplifier circuit. The current i_x is known to be 4 mA. (a) Find the value of R. (b) Show that the sum of currents into the rest of the circuit is zero.

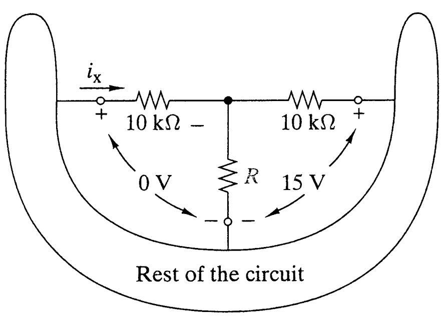


FIGURE P2–25

2–26 Figure P2–26 shows a resistor with one terminal connected to ground and the other connected to an arrow. The arrow symbol is used to indicate a connection to one terminal of a voltage source whose other terminal is connected to ground. The label next to the arrow indicates the source voltage at the ungrounded terminal. Find the voltage across, current through, and power dissipated in the resistor.

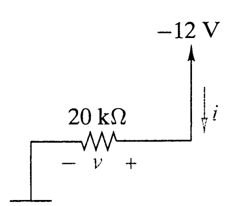


FIGURE P2–26

ERO 2–4 EQUIVALENT CIRCUITS (SECT. 2–4)

(a) Given a circuit consisting of linear resistors, find the equivalent resistance between a specified pair of terminals.
(b) Given a circuit consisting of a source-resistor combination, find an equivalent source-resistor circuit.

See Example 2–11, 2–12 and Exercises 2–7, 2–8, 2–9

2–27 Find the equivalent resistance R_{EQ} in Figure P2–27.

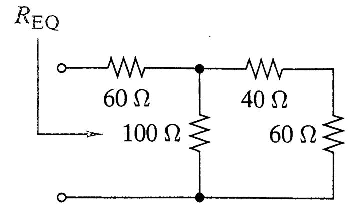


FIGURE P2–27

2–28 Find the equivalent resistance R_{EQ} in Figure P2–28.

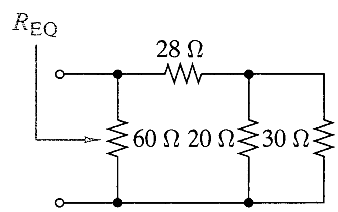


FIGURE P2–28

2–29 Find the equivalent resistance R_{EQ} in Figure P2–29 when the switch is open. Repeat when the switch closed.

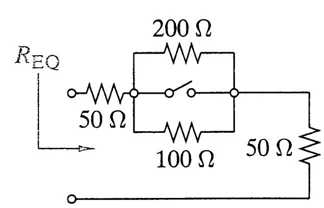


FIGURE P2–29

2–30 Find the equivalent resistance between terminals A–B, B–C, A–C, C–D, B–D, and A–D in the circuit of Figure P2–30.

2–31 Find the equivalent resistance between terminals A–B, A–C, A–D, B–C, B–D, and C–D in the circuit of Figure P2–31.

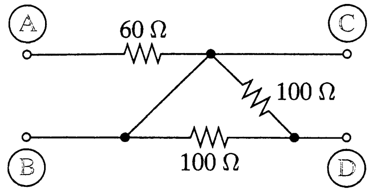


FIGURE P2–30

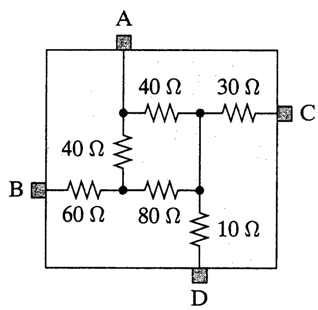


FIGURE P2–31

2–32 Find the equivalent resistance R_{EQ} in Figure P2–32 when R_L = 10 kΩ. Repeat when R_L = 0. Select the value of R_L so that R_{EQ} = 22 kΩ.

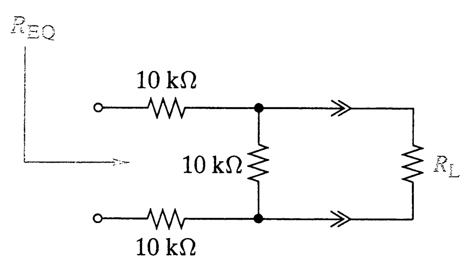


FIGURE P2–32

2–33 An ideal 15-V voltage source is connected in series with a 50-Ω resistor. Use source transformations to obtain an equivalent practical current source.

2–34 A 5-mA practical current source is connected in parallel with a 2-kΩ resistor. The voltage across the resistor is observed to be 5 V. Find the source resistance of the practical current source.

2–35 The circuit of Figure P2–35 is an R-2R resistance array package. All of the following equivalent resistances can be obtained by making proper connections of the array *except for one*: $R/2$, $2R/3$, R, $8R/5$, $2R$, $3R$, and $4R$. Show how to interconnect the terminals of the array to produce the equivalent resistances, and identify the one that cannot be obtained using this array.

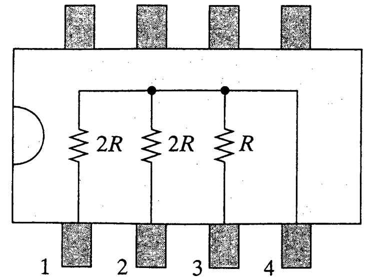


FIGURE P2–35

2–36 Select the value of R_x in Figure P2–36 so that R_{EQ} = 49 kΩ.

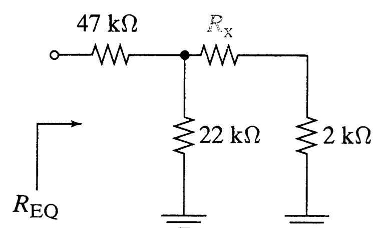


FIGURE P2–36

2–37 Using no more than 14 resistors, show how to interconnect standard 4.3-kΩ resistors to obtain equivalent resistances of 1 kΩ ±10%, 5 kΩ ±10%, and 10 kΩ ±10%.

2–38 Select the value of R in Figure P2–38 so that R_{AB} = R_L.

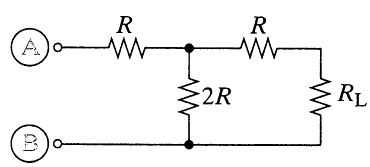


FIGURE P2–38

2–39 What is the range of R_{EQ} in Figure P2–39?

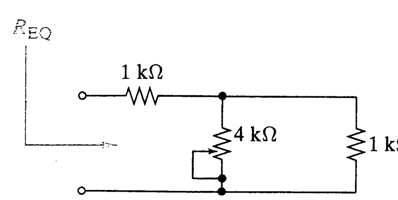


FIGURE P2–39

2–40 Find the equivalent resistance between terminals A and B in Figure P2–40.

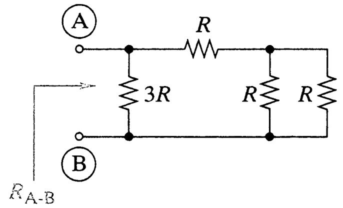


FIGURE P2–40

ERO 2–5 VOLTAGE AND CURRENT DIVISION (SECT. 2–5)

(a) Given a circuit with elements connected in series or parallel, use voltage or current division to find specified voltages or currents.
(b) Design a voltage or current divider that delivers specified output signals within stated constraints.
See Examples 2–13, 2–14, 2–16, 2–17, 2–18 and Exercises 2–10, 2–11, 2–12

2–41 Use voltage division in Figure P2–41 to obtain an expression for v_L in terms of R, R_L, and v_S.

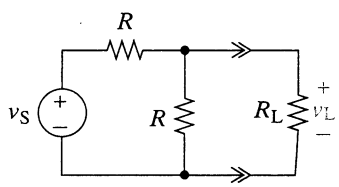


FIGURE P2–41

2–42 Find v_x in Figure P2–42.

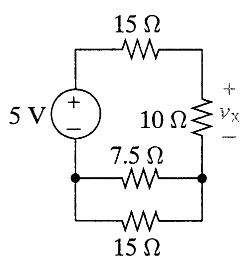


FIGURE P2–42

2–43 Find i_x in Figure P2–43.

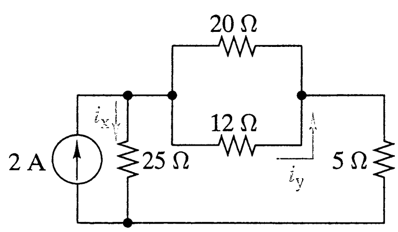


FIGURE P2–43

2–44 Find i_y in Figure P2–43.

2–45 The electronic switch in Figure P2–45 is controlled by the voltage between gate G and ground. The switch is closed (R_{ON} = 100 Ω) when $v_G > 2$ V and open (R_{OFF} = 500 MΩ) when $v_G < 0.8$ V. Use voltage division to predict v_O when $v_G = 5$ V and $v_G = 0.5$ V.

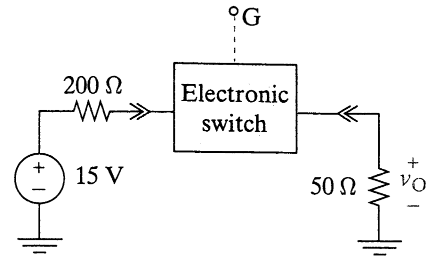


FIGURE P2–45

2–46 Figure P2–46 shows a resistance divider connected in a general circuit.

(a) What is the relationship between v_1 and v_2 when $i_1 = 0$?
(b) What is the relationship between v_1 and v_2 when $i_2 = 0$?
(c) What is the relationship between i_1 and i_2 when $v_1 = 0$?
(d) What is the relationship between i_1 and i_2 when $v_2 = 0$?

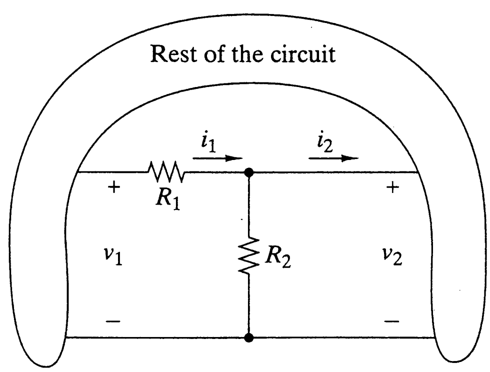


FIGURE P2–46

2–47 Figure P2–47 shows an ammeter circuit consisting of a D'Arsonval meter, a two-position selector switch, and two shunt resistors. A current of 0.5 mA produces full-scale deflection of the D'Arsonval meter, whose internal resistance is R_M = 50 Ω. Select the shunt resistance R_1 and R_2 so that i_x = 10 mA produces full scale deflection when the switch is in position A, and i_x

= 50 mA produces full-scale deflection when the switch is in position B.

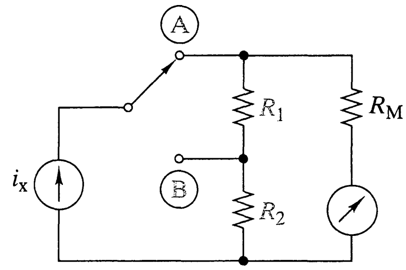


FIGURE P2-47

2-48 Figure P2-48 shows the R-2R integrated circuit package connected as a voltage divider and across a 15-V source. The divider output is 5 V for the connections shown in the figure. Show how to interconnect the source and the R-2R package to obtain outputs of 3 V, 6 V, 9 V, and 12 V.

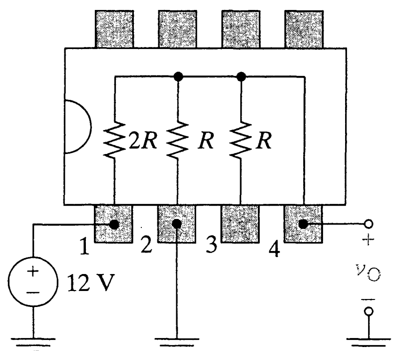


FIGURE P2-48

2-49 Find the value of R_x in Figure P2-49 such that v_L = 2 V.

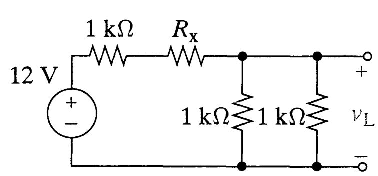


FIGURE P2-49

2-50 Find the value of R_x in Figure P2-50 such that v_L = 3 V.

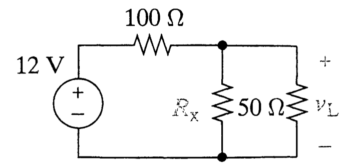


FIGURE P2-50

ERO 2-6 CIRCUIT REDUCTION (SECT. 2-6)

Given a circuit consisting of linear resistors and an independent source, find selected signal variables using successive application of series/parallel equivalence, source transformations, and voltage/current division.
See Example 2-20, 2-21, 2-22, 2-23 and Exercises 2-13, 2-14, 2-15

2-51 Use circuit reduction to determine v_x and i_x in the circuit shown in Figure P2-51.

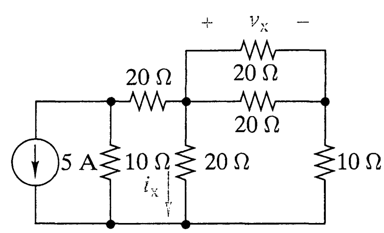


FIGURE P2-51

2-52 Use circuit reduction to find i_S and i_x in the circuit shown in Figure P2-52.

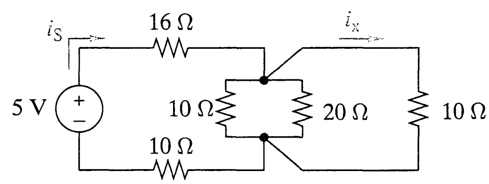


FIGURE P2-52

2-53 Use circuit reduction to find v_x and i_x in the circuit shown in Figure P2-53.

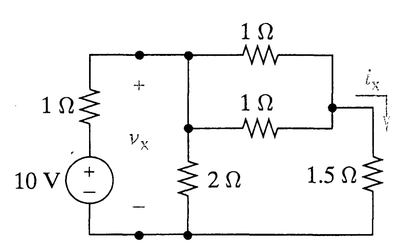


FIGURE P2-53

2–54 Use circuit reduction to find v_x and i_x in the circuit shown in Figure P2–54.

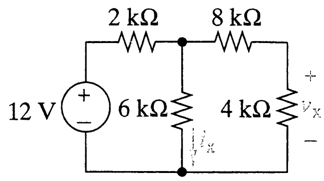


FIGURE P2–54

2–55 The resistance array circuit in Figure P2–55 has external terminals at pads A, B, C, and D. Connect the "+" terminal of a 10-V voltage to terminal A and the "−" to terminal C. Find the voltage v_{AB}.

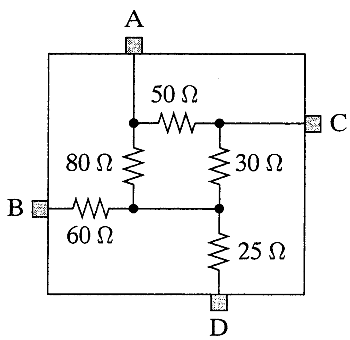


FIGURE P2–55

2–56 The resistance array circuit in Figure P2–55 has external terminals at pads A, B, C, and D. Connect the "+" terminal of a 10-V voltage to terminal A and the "−" to terminal B. Find the voltage v_{DB}.

2–57 The resistance array circuit in Figure P2–55 has external terminals at pads A, B, C, and D. Connect the "+" terminal of a 5-V voltage to terminal C and the "−" to ground. Connect terminal B to ground. Find the voltage v_{DB}.

2–58 Select the value of R_L in Figure P2–58 so that the power delivered to R_L is at least 50 mW.

2–59 Select the value of R_L in Figure P2–58 so that the voltage delivered to R_L is at least 2.5 V.

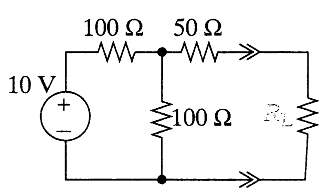


FIGURE P2–58

2–60 The box in the circuit in Figure P2–60 is a resistor whose value can be anywhere between 8 kΩ and 80 kΩ. Use circuit reduction to find the range of values of the outputs v_x and i_x.

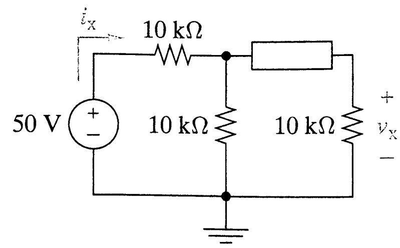


FIGURE P2–60

INTEGRATING PROBLEMS

2–61 Device Modeling

The circuit in Figure P2–61 consists of a 50-Ω linear resistor in parallel with a nonlinear varistor whose i–v characteristic is $i_V = 2.6 \times 10^{-5} v^3$.

(a) Plot the i–v characteristic of the parallel combination.

(b) State whether the parallel combination is linear or nonlinear, active or passive, and bilateral or nonbilateral.

(c) Identify a range of voltages over which the parallel combination can be modeled within ±10% by a linear resistor.

(d) Identify a range of voltages over which the parallel combination can be safely operated if both devices are rated at 50 W. Which device limits this range?

(e) The parallel combination is connected in series with a 50-Ω resistor and a 5-V voltage source. In this circuit, how would you model the parallel combination and why?

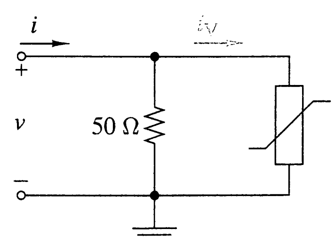


FIGURE P2–61

2–62 Wheatstone Bridge

The Wheatstone bridge circuit in Figure P2–62(a) is used in instrumentation systems. The resistance R_x is the equivalent resistance of a transducer (a device that converts energy from one form to another). The value of R_x varies in relation to an external physical phenomenon such as temperature, pressure, or light. The resistance R_M is the equivalent resistance of a measuring instrument such as a D'Arsonval meter. Prior to any measurements, one of the other resistors (usually R_3) is adjusted until the current i_M is zero. The resistance of the transducer changes when exposed to the physical phenomenon it is designed to measure. This change causes the bridge to become unbalanced, and the meter indicates the resulting current through R_M. The deflection of the meter is calibrated to indicate the value of the physical phenomenon measured by the transducer.

(a) Derive the relationship between R_1, R_2, R_3, and R_x when $i_M = 0$ A.

(b) Suppose the transducer resistance R_x varies with temperature, as shown in Figure P2–62(b). With $R_1 = R_2 = 2.2$ kΩ, find the value of R_3 that produces $i_M = 0$ at a temperature of 57.5° C.

(c) A current $i_M = -1.5$ mA is observed when $R_1 = R_2 = 2.2$ kΩ and R_3 is set to the value found in part (b). Is the temperature higher or lower than 57.5° C?

(d) For $R_1 = R_2 = 2.2$ kΩ and $R_3 = 2.4$ kΩ, find the temperature at which $i_M = 0$.

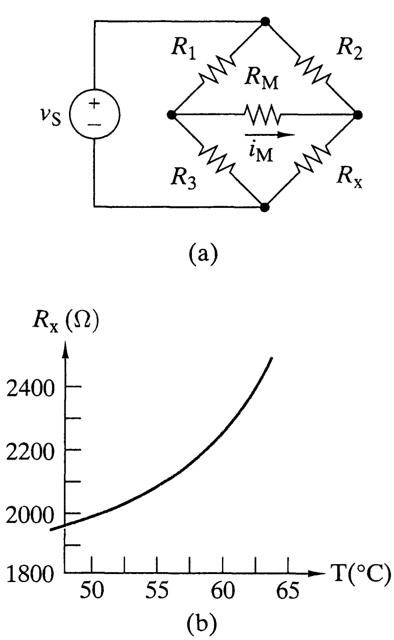


FIGURE P2–62

2–63 Three-Terminal Equivalence

Two circuits are said to be equivalent when they have the same i–v characteristics between specified terminal pairs. In this chapter we applied this definition to two-terminal circuits such as resistors in series or parallel and source transformations. The concept can be extended to the three-terminal circuits in Figure P2–63. These three- terminal circuits will be equivalent if the equivalent resistances seen between terminal pairs A and B, B and C, and C and A are the same.

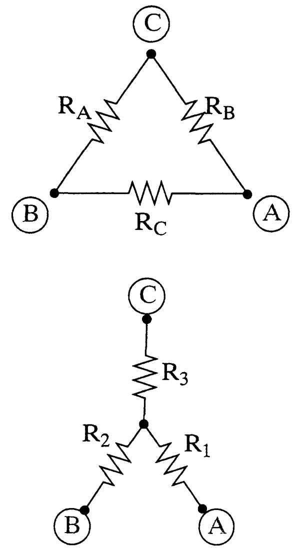


FIGURE P2–63

(a) Show that the two circuits are equivalent when

$$R_1 = \frac{R_B R_C}{R_A + R_B + R_C} \quad \text{and}$$

$$R_2 = \frac{R_C R_A}{R_A + R_B + R_C} \quad \text{and}$$

$$R_3 = \frac{R_A R_B}{R_A + R_B + R_C}$$

(b) Equivalence is useful because replacing one circuit by an equivalent circuit does not change the response of the rest of the circuit and may simplify an analysis problem. For example, the equations in (a) tell us how to create an equivalent Y-connected subcircuit like Figure P2–63(b) to replace the Δ-connected subcircuit in Figure P2–63(a). Such a replacement is called a Δ-to-Y transformation. Show that a Y-to- Δ transformation is also possible provided

$$G_A = \frac{G_2 G_3}{G_1 + G_2 + G_3} \quad \text{and}$$

$$G_B = \frac{G_1 G_3}{G_1 + G_2 + G_3} \quad \text{and}$$

$$G_C = \frac{G_1 G_2}{G_1 + G_2 + G_3}$$

-64 Digital-to-Analog Conversion

Digital-to-analog (D-to-A) conversion provides a link between the digital and analog worlds. A D-to-A converter produces a single analog output v_O from a multibit digital input $\{b_0, b_1, b_2, \ldots b_{N-1}\}$, where the bits b_j ($j = 0, 1, \ldots N-1$) are either 0 or 1. One method is to produce an analog output that is proportional to a fixed reference voltage V_{REF} and related to the digital inputs by the following algorithm

$$v_O = K V_{REF} \sum_{j=0}^{N-1} b_j 2^j$$

Figure P2–64 shows a programmable voltage divider in which two digital inputs control complementary analog switches connecting a multitap voltage divider to the output terminal. Show that the programmable voltage divider implements this D-to-A algorithm with $K = 0.25$ and $N = 2$.

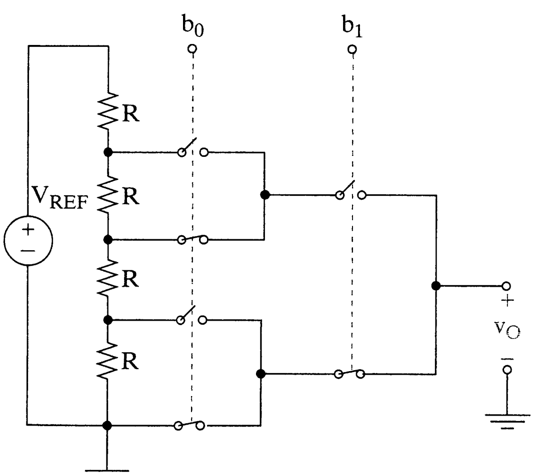


FIGURE P2–64

-65 Analog Voltmeter Design

A voltmeter can be made using a series resistor and a D'Arsonval meter. Figure P2–65(a) shows a voltmeter circuit consisting of a D'Arsonval meter, a two-position selector switch, and two series resistors. A current of 500 μA produces full-scale deflection of the D'Arsonval meter, whose internal resistance is $R_M = 50\ \Omega$.

(a) Select the series resistance R_1 and R_2 so a voltage $v_x = 50$ V produces full-scale deflection when the switch is in position A, and voltage $v_x = 10$ V produces full-scale deflection when the switch is in position B.

(b) By voltage division the voltage across the 20-kΩ resistor in Figure P2–65(b) is 20 V when the voltmeter is disconnected. What voltage reading is obtained when the voltmeter designed in part (a) is connected across the 20-kΩ resistor? What is the percentage error in the voltmeter reading?

(c) A D'Arsonval meter with an internal resistance of 200 Ω and a full-scale deflection current of 100 μA is available. If the voltmeter in part (a) is redesigned using this D'Arsonval meter, would the error found in part (b) be smaller or larger? Explain.

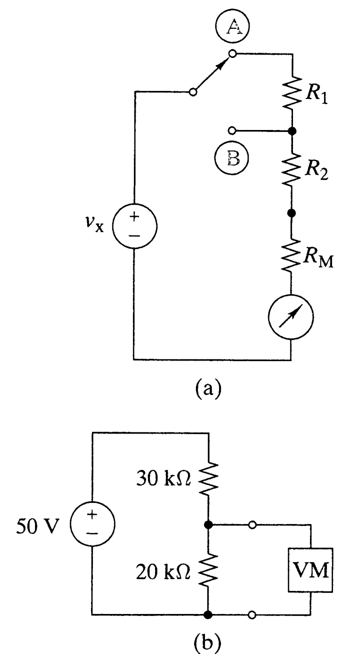


FIGURE 2–65

DISCUSSION: *(a) A standard 56-Ω resistor in series (ideally 58.1 Ω) yields 200 mW ±5% into the 50-Ω load. (b) No resistive interface will work since the maximum power available from the source is only 0.5 W. Delivering more power than the signal source can provide requires an active device, such as an OP AMP or transistor (treated in the next chapter).*

SUMMARY

- Node-voltage analysis involves identifying a reference node and the node to datum voltages at the remaining $N-1$ nodes. The KCL connection constraints at the $N-1$ nonreference nodes combined with the element constraints written in terms of the node voltages produce $N-1$ linear equations in the unknown node voltages.
- Mesh-current analysis involves identifying mesh currents that circulate around the perimeter of each mesh in a planar circuit. The KVL connection constraints around $E-N+1$ meshes combined with the element constraints written in terms of the mesh currents produce $E-N+1$ linear equations in the unknown mesh currents.
- Node and mesh analysis can be modified to handle both types of independent sources using a combination of three methods: (1) source transformations, (2) selecting circuit variables so independent sources specify the values of some of the unknowns, and (3) using supernodes or supermeshes.
- A circuit is linear if it contains only linear elements and independent sources. For single-input linear circuits, the proportionality property states that any output is proportional to the input. For multiple-input linear circuits, the superposition principle states that any output can be found by summing the output produced when each input acts alone.
- A Thévenin equivalent circuit consists of a voltage source in series with a resistance. A Norton equivalent circuit consists of a current source in parallel with a resistance. The Thévenin and Norton equivalent circuits are related by a source transformation.
- The parameters of the Thévenin and Norton equivalent circuits can be determined using any two of the following: (1) the open-circuit voltage at the interface, (2) the short-circuit current at the interface, and (3) the equivalent resistance of the source circuit with all sources turned off.
- The parameters of the Thévenin and Norton equivalent circuits can also be determined using circuit reduction methods or by directly solving for the source i–v relationship using node-voltage or mesh-current analysis.
- For a fixed source and an adjustable load, the maximum interface signal levels are $v_{MAX} = v_{OC}$ ($R_L = \infty$), $i_{MAX} = i_{SC}$ ($R_L = 0$), and $p_{MAX} = v_{OC}i_{SC}/4$ ($R_L = R_T$). When $R_L = R_T$, the source and load are said to be matched.
- Interface signal transfer conditions are specified in terms of the voltage, current, or power delivered to the load. The design constraints depend on the signal conditions specified and the circuit parameters that are adjustable. Some design requirements may require a two-port interface circuit. An interface design problem may have one, many, or no solutions.

PROBLEMS

ERO 3–1 General Circuit Analysis (Sect. 3–1 to 3–2)

Given a circuit consisting of linear resistors and independent sources,

(a) (Formulation) Write node-voltage or mesh-current equations for the circuit.
(b) (Solution) Solve the equations from (a) for selected signal variables or input-output relationships.

Node-voltage method:
See Examples 3–1, 3–2, 3–3, 3–4, 3–5, 3–6 and Exercises 3–2, 3–3, 3–4, 3–5, 3–6
Mesh-current method:
See Examples 3–7, 3–8, 3–9, and Exercises 3–8, 3–9, 3–10

3–1 **(a)** Formulate node-voltage equations for the circuit in Figure P3–1.
(b) Use these equations to find v_x and i_x.

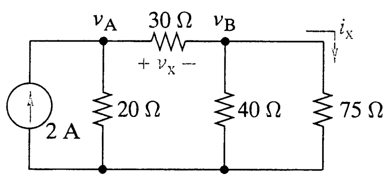


FIGURE P3–1

3–2 **(a)** Formulate node-voltage equations for the circuit in Figure P3–2.
(b) Use these equations to find v_x and i_x.

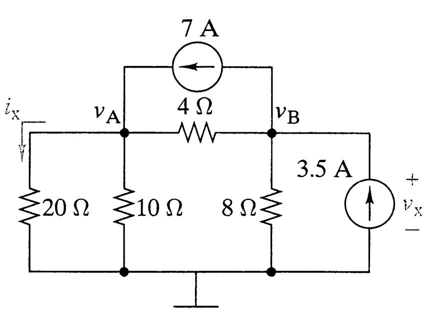


FIGURE P3–2

3–3 **(a)** Formulate node-voltage equations for the circuit in Figure P3–3.
(b) Use these equations to find v_x and i_x.

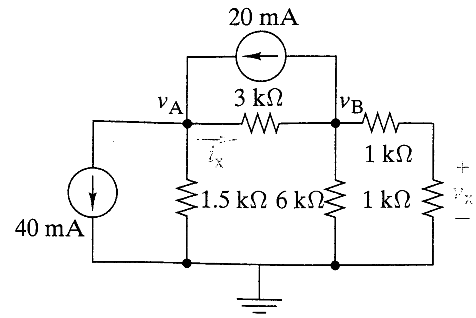


FIGURE P3–3

3–4 **(a)** Formulate a set of node-voltage equations for the circuit in Figure P3–4.
(b) Use these equations to find v_x and i_x.

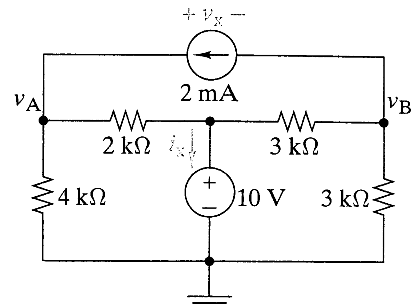


FIGURE P3–4

3–5 **(a)** Formulate node-voltage equations for the circuit in Figure P3–5.
(b) Solve for v_x and i_x when $v_S = 4$ V, $i_S = 2$ mA, $R_1 = R_2 = 10$ kΩ, and $R_3 = R_4 = 5$ kΩ.

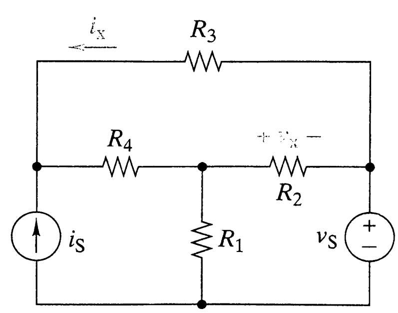


FIGURE P3–5

3–6 **(a)** Formulate node-voltage equations for the circuit in Figure P3–6.
(b) Solve for v_x and i_x using $R_1 = 10$ kΩ, $R_2 = 10$ kΩ, $R_3 = 40$ kΩ, $R_4 = 20$ kΩ, $v_1 = v_2 = 5$ V, and $v_3 = 15$ V.
(c) Find the power delivered to resistor R_1.

3–12 **(a)** Formulate mesh-current equations for the circuit in Figure P3–12.

(b) Solve for v_x and i_x using $R_1 = 200\ \Omega$, $R_2 = 500\ \Omega$, $R_3 = 60\ \Omega$, $R_4 = 240\ \Omega$, $R_5 = 200\ \Omega$, $i_S = 50$ mA, and $v_S = 15$ V.

(c) Find the total power dissipated in the circuit.

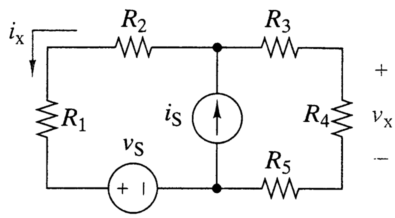


FIGURE P3–12

3–13 **(a)** Formulate mesh-current equations for the circuit in Figure P3–13.

(b) Solve for v_x and i_x using $R_1 = R_2 = 10$ kΩ, $R_3 = 2$ kΩ, $R_4 = 1$ kΩ, $i_S = 2.5$ mA, $v_{S1} = 12$ V, and $v_{S2} = 0.5$ V.

(c) Find the power supplied by v_{S1}.

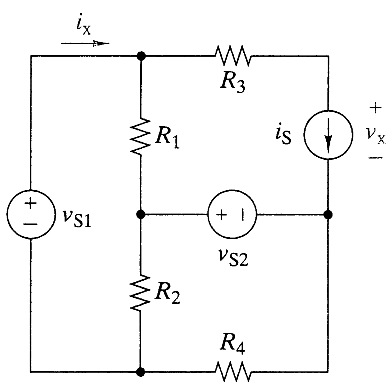


FIGURE P3–13

3–14 The circuit in Figure P3–14 seems to require two supermeshes since both current sources appear in two meshes. However, a circuit diagram can sometimes be rearranged to eliminate the need for supermesh equations.

(a) Show that supermeshes in Figure P3–14 can be avoided by connecting resistor R_6 between node A and node D via a different route.

(b) Formulate mesh-current equations for the modified circuit as redrawn in (a).

(c) Solve for v_x using $R_1 = R_2 = R_3 = R_4 = 2$ kΩ, $R_5 = R_6 = 1$ kΩ, $i_{S1} = 40$ mA, and $i_{S2} = 20$ mA.

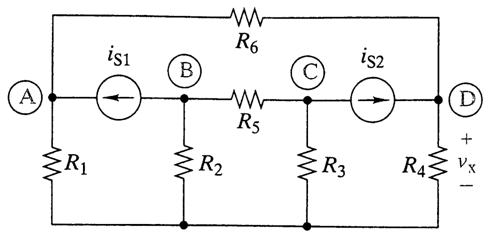


FIGURE P3–14

3–15 **(a)** Formulate mesh-current equations for the circuit in Figure P3–15.

(b) Use these equations to find v_x and i_x.

(c) Find the total power delivered to the resistors.

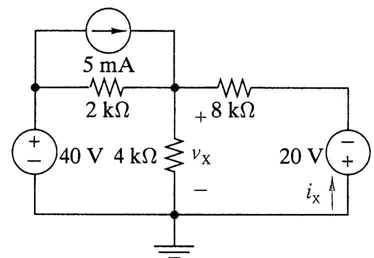


FIGURE P3–15

3–16 **(a)** Formulate mesh-current equations for the circuit in Figure P3–16.

(b) Use these equations to find the input resistance.

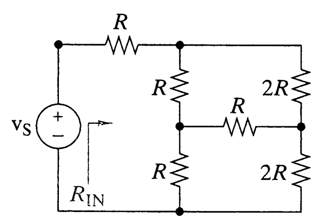


FIGURE P3–16

3–17 Use node-voltage or mesh-current analysis to find i_x in Figure P3–17.

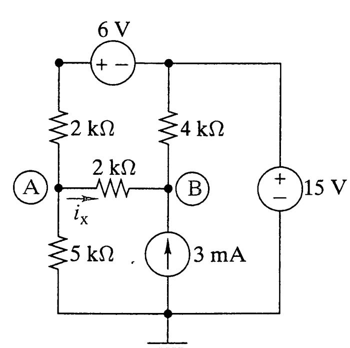


FIGURE P3–17

3–18 Use the node-voltage or mesh-current method in Figure P3–18 to find v_O in terms of v_1, v_2, and v_3.

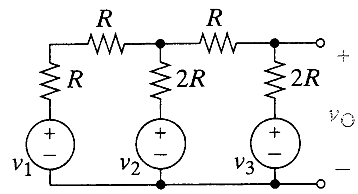


FIGURE P3–18

3–19 Find the node voltages v_A and v_B in Figure P3–19.

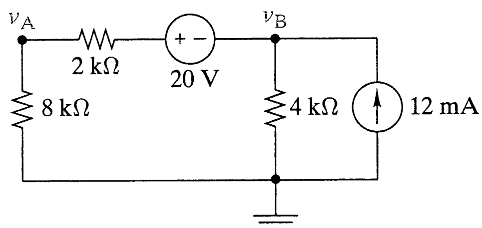


FIGURE P3–19

3–20 Find the mesh currents i_A, i_B, and i_C in Figure P3–20.

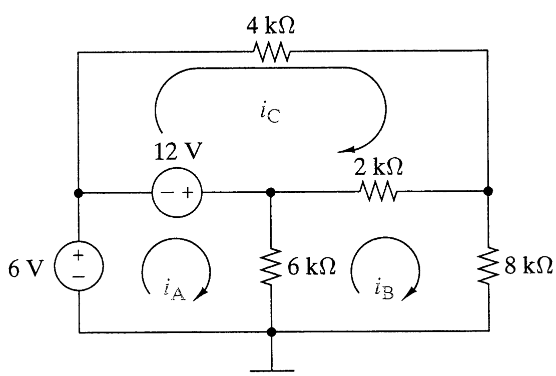


FIGURE P3–20

ERO 3–2 LINEARITY PROPERTIES (SECT. 3–3)

(a) Given a circuit containing linear resistors and one independent source, use the proportionality principle to find selected signal variables.
(b) Given a circuit containing linear resistors and two or more independent sources, use the superposition principle to find selected signal variables.

See Examples 3–10, 3–11, 3–12 and Exercises 3–11, 3–12, 3–13, 3–14, 3–15

3–21 Find the proportionality constant $K = v_O/i_S$ for the circuit in Figure P3–21.

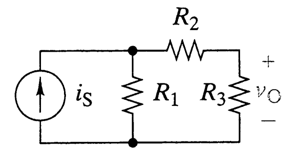


FIGURE P3–21

3–22 Find the proportionality constant $K = i_O/i_S$ for the circuit in Figure P3–22.

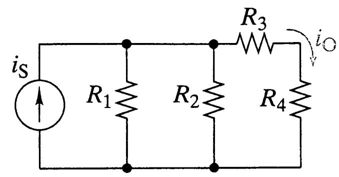


FIGURE P3–22

3–23 Find the proportionality constant $K = v_O/i_S$ for the circuit in Figure P3–23.

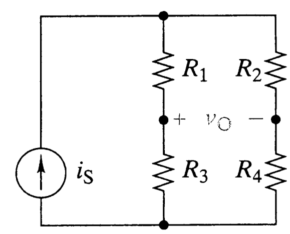


FIGURE P3–23

3–24 Use the unit output method to find v_O in the circuit in Figure P3–24.

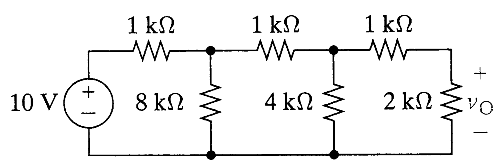


FIGURE P3–24

3–25 Use the unit output method to find i_O in the circuit in Figure P3–25.

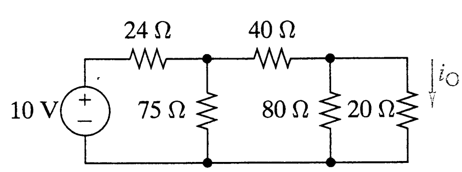


FIGURE P3–25

3–26 Use the unit output method to select R in the circuit in Figure P3–26 so that the proportionality constant $K = v_O/v_S = 1/4$.

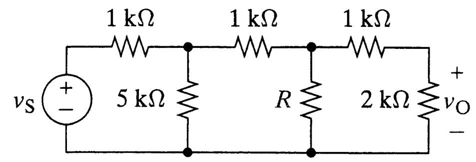


FIGURE P3–26

3–27 Find the proportionality constant $K = v_O/v_S$ for the circuit in Figure P3–27.

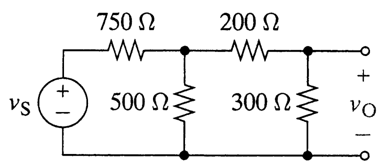


FIGURE P3–27

3–28 Use the superposition principle in the circuit of Figure P3–28 to find v_O.

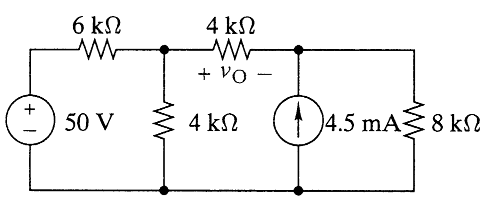


FIGURE P3–28

3–29 Use the superposition principle in the circuit of Figure P3–29 to find i_O.

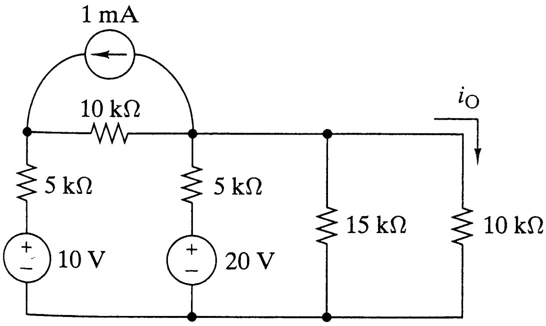


FIGURE P3–29

3–30 Use the superposition principle in the circuit of Figure P3–30 to find v_O in terms of v_1, v_2, and R.

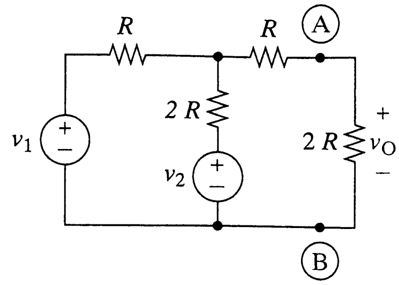


FIGURE P3–30

3–31 Use the superposition principle in the circuit of Figure P3–31 to find v_O in terms of i_1, i_2, and R.

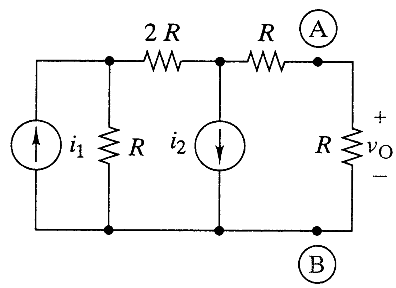


FIGURE P3–31

3–32 A linear circuit containing two sources drives a 100-Ω load resistor. Source number 1 delivers 250 mW to the load when source number 2 is off. Source number 2 delivers 4 W to the load when source number 1 is off. Find the power delivered to the load when both sources are on. *Hint*: The answer is not 4.25 W. Why?

3–33 A linear circuit is driven by an independent voltage source $v_S = 10$ V and an independent current source $i_S = 10$ mA. When the voltage source is on and the current source is off, the output voltage is $v_O = 2$ V. When both sources are on, the output is $v_O = 1$ V. Find the output when $v_S = 5$ V and $i_S = -10$ mA.

3–34 The following table lists test data of the output of a linear resistive circuit for different values of its three inputs. Find the input–output relationship for the circuit.

v_{S1}(V)	v_{S2}(V)	v_{S3}(V)	v_O(V)
0	4	−4	0
2	0	2	1.5
2	4	0	2

3–35 This problem involves designing a resistive circuit with two inputs v_{S1} and v_{S2} and a single output voltage v_O. Design the circuit so that $v_O = K(v_{S1} + 3v_{S2})$ is delivered across a 500-Ω load. The value of K is not specified but should be greater than 1/20.

ERO 3–3 THÉVENIN AND NORTON EQUIVALENT CIRCUITS (SECT. 3–4)

Given a circuit containing linear resistors and independent sources,

(a) Find the Thévenin or Norton equivalent at a specified pair of terminals.
(b) Use the Thévenin or Norton equivalent to find the signals delivered to linear or nonlinear loads.

See Examples 3–13, 3–14, 3–15, 3–16 and Exercises 3–16, 3–17, 3–18

3–36 **(a)** Find the Thévenin or Norton equivalent circuit seen by R_L in Figure P3–36.
(b) Use the equivalent circuit found in (a) to find i_L in terms of i_S, R_1, R_2, and R_L.
(c) Check your answer in (b) using current division.

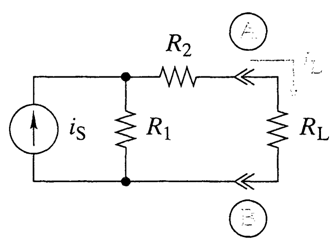


FIGURE P3–36

3–37 **(a)** Find the Thévenin or Norton equivalent circuit seen by R_L in Figure P3–37.
(b) Use the equivalent circuit found in (a) to find load power when R_L = 50 Ω, 100 Ω, and 500 Ω.

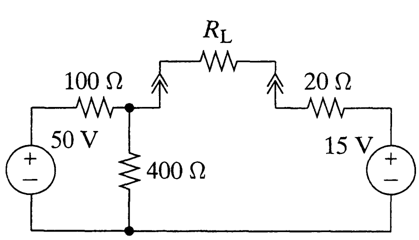


FIGURE P3–37

3–38 **(a)** Find the Thévenin or Norton equivalent seen by R_L in Figure P3–38.
(b) Use the equivalent circuit found in (a) to find load voltage when R_L = 10 kΩ, 25 kΩ, 50 kΩ, and 100 kΩ.

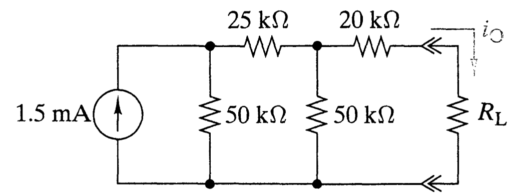


FIGURE P3–38

3–39 **(a)** Find the Thévenin or Norton equivalent seen by R_L in Figure P3–39.
(b) Use the equivalent circuit found in (a) to find i_O for R_L = 6 kΩ, R_L = 12 kΩ, 24 kΩ, and 48 kΩ.

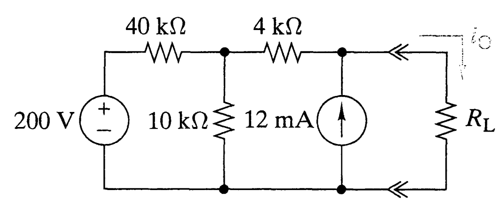


FIGURE P3–39

3–40 **(a)** Find the Thévenin or Norton equivalent at terminals A and B in Figure P3–40.
(b) Use the equivalent circuit to find interface power when a 10-Ω load is connected between terminals A and B.
(c) Repeat (b) when a 5-V source is connected between terminals A and B with the plus terminal at terminal A.

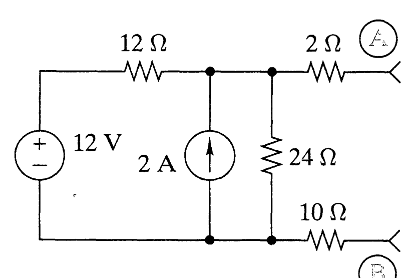


FIGURE P3–40

3–41 (a) Find the Thévenin or Norton equivalent seen to the left of terminals A and B in Figure P3–41. (*Hint*: Use source transformations and circuit reduction.)
(b) Use the equivalent found in (a) to find the output v_O in terms of v_1, v_2, and R.

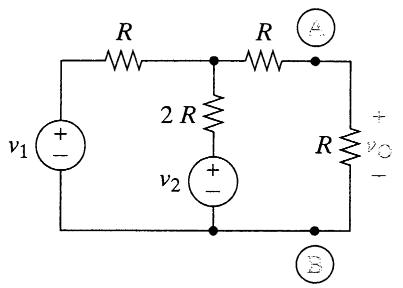


FIGURE P3–41

3–42 Figure P3–42 shows a source circuit with two accessible terminals. When $i = 0$ the output voltage is $v = 10$ V. When a 2.4-kΩ resistor is connected between the terminals the output drops to 6 V.
(a) Find the Thévenin equivalent of the source.
(b) Use the equivalent circuit to find the power the source would deliver to resistive loads of 500 Ω, 1 kΩ, and 2 kΩ.

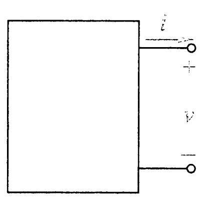


FIGURE P3–42

3–43 Figure P3–42 shows a source circuit with two accessible terminals. When a 300-Ω resistor is connected across the accessible terminals, the output current is i = 30 mA. When a 500-Ω resistor is connected, the output current is i = 20 mA. How much current would this source deliver to a 10-V source?

3–44 Figure P3–42 shows a source circuit with two accessible terminals. Some voltage and current measurements at the accessible terminals are

v (V)	−10	−5	0	+5	+10	12	13	14
i (mA)	+5	+4	+3	+2	+1	0	−1	−2

(a) Plot the source i–v characteristic using these data.
(b) Develop a Thévenin equivalent circuit valid on the range $|v| < 10$ V.
(c) Use the equivalent circuit to predict the source v_{OC} and i_{SC}.
(d) Compare your results in (c) with the given measurements and explain any differences.

3–45 The Thévenin equivalent parameters of a two-terminal source are $v_T = 5$ V and $R_T = 150$ Ω. Find the minimum allowable load resistance if the delivered load voltage must exceed 3.5 V.

3–46 Use a sequence of source transformations to find the Thévenin equivalent at terminals A and B in Figure P3–46.

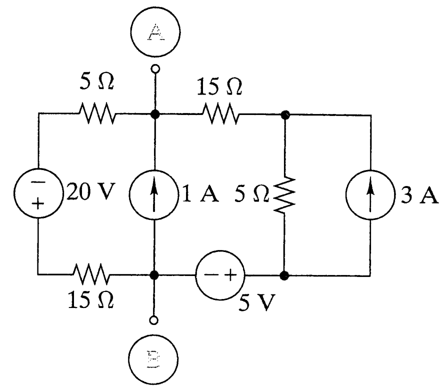


FIGURE P3–46

3–47 (a) Find the Thévenin or Norton equivalent seen by R_L in Figure P3–47.

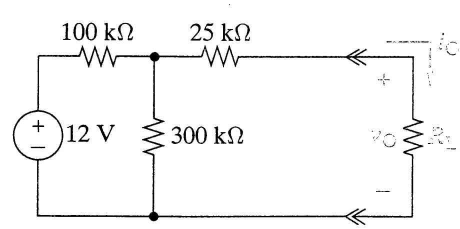


FIGURE P3–47

(b) Use the equivalent circuit to find the value of R_L that produces $v_O = 6$ V.

3–48 The current delivered to R_L in Figure P3–47 is observed to be $i_O = 36$ μA. Find the value of R_L.

3–49 A nonlinear resistor is connected across a two-terminal source whose Thévenin equivalent is $v_T = 5$ V and $R_T = 500$ Ω.

(a) Plot the i–v characteristic of the source in the first quadrant ($i \geq 0$, $v \geq 0$).

(b) The i–v characteristic of the resistor is $i = 10^{-4}(v + 2\,v^{3.3})$. Plot this characteristic on the source plot obtained in (a) and graphically determine the voltage across and current through the nonlinear resistor.

3–50 A nonlinear resistor is connected across a two-terminal source whose Thévenin equivalent is $v_T = 10$ V and $R_T = 200\ \Omega$.

(a) Plot the i–v characteristic of the source in the first quadrant ($i \geq 0$, $v \geq 0$).

(b) The i–v characteristic of the resistor is $v = 4000\,i^2$. Plot this characteristic on the source plot obtained in (a) and graphically determine the voltage across and current through the nonlinear resistor.

ERO 3–4 MAXIMUM SIGNAL TRANSFER (SECT. 3–5)

Given a circuit containing linear resistors and independent sources,

(a) Find the maximum voltage, current, and power available at a specified pair of terminals.

(b) Find the resistive loads required to obtain the maximum available signal levels.

See Example 3–17 and Exercise 3–19

3–51 **(a)** The load resistance in Figure P3–51 is adjusted until the maximum power is delivered. Find the power delivered and the value of R_L.

(b) The load resistance is adjusted until maximum voltage is delivered. Find the voltage delivered and the value of R_L.

(c) The load resistance is adjusted until maximum current is delivered. Find the current delivered and the value of R_L.

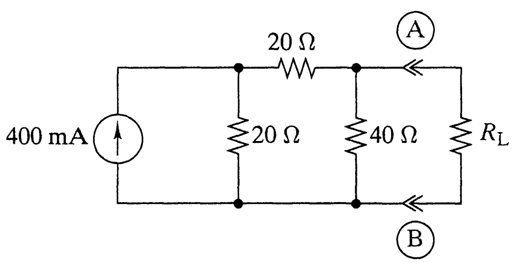


FIGURE P3–51

3–52 Find the maximum power available to the load resistance in Figure P3–52. What value of R_L will extract maximum power?

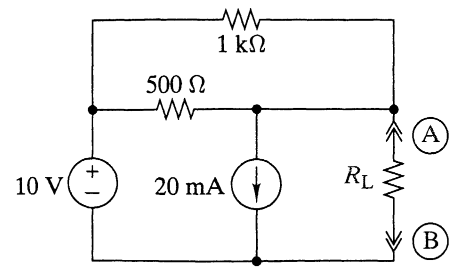


FIGURE P3–52

3–53 Find the maximum power available to the load resistance in Figure P3–53. What value of R_L will extract maximum power?

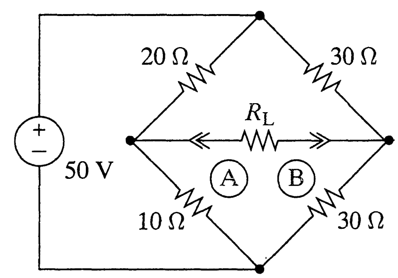


FIGURE P3–53

3–54 The resistance R in Figure P3–54 is adjusted until maximum power is delivered across the interface to the load consisting of R and the 6-kΩ resistor in parallel. Find the voltage and power delivered to the load and the value of R.

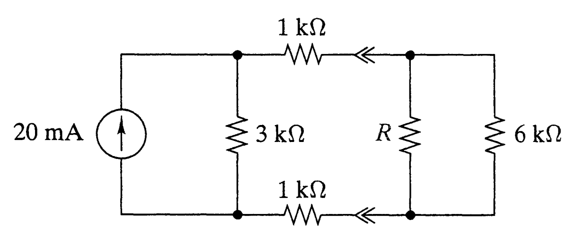


FIGURE P3–54

3–55 When a 2-kΩ resistor is connected across a two-terminal source, a current of 0.75 mA is delivered to the load. When a second 2-kΩ resistor is connected in parallel with the first, a total current of 1 mA is delivered. Find the maximum power available from the source and specify the load resistance required to extract maximum power from the source.

3–56 **(a)** The potentiometer in Figure P3–56 is adjusted until maximum power is delivered to the 2-kΩ load. Find the wiper position x. *Caution*: The load is fixed.

(b) The potentiometer in Figure P3–56 is adjusted until maximum voltage is delivered to the 2-kΩ load. Find the wiper position x.

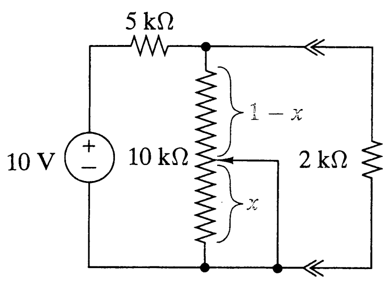


FIGURE P3–56

3–57 Find the value of R_L in Figure P3–57 such that i_L = 3 mA.

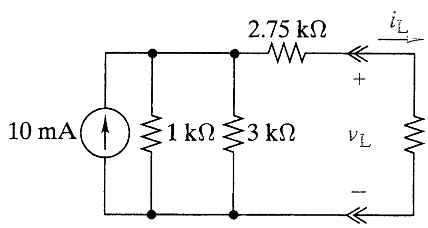


FIGURE P3–57

3–58 Find the value of R_L in Figure P3–57 such that v_L = 5 V.

3–59 A 15-V source with 100 Ω internal resistance is connected in series with a resistor R_S. Select the value of R_S so that outputs of the series combination are bounded by $i < 50$ mA and $p < 200$ mW for any load resistance.

3–60 A practical source delivers 50 mA to a 300-Ω load. The source delivers 12 V to a 120-Ω load. Find the maximum power available from the source.

ERO 3–5 INTERFACE CIRCUIT DESIGN (SECT. 3–6)

Given the signal transfer objectives at a source-load interface, adjust the circuit parameters or design one or more two-port interface circuits to achieve the specified objectives within stated constraints. See Examples 3–18, 3–19, 3–20, 3–21, 3–22 and Exercises 3–20, 3–21

3–61 Figure P3–61 shows a two-port interface circuit connecting source and load circuits. In this problem v_S = 10 V, R_S = 50 Ω, and the load is a 50-Ω resistor. To avoid damaging the source, its output current must be less than 100 mA. Design a resistive interface circuit so that the voltage delivered to the load is 4 V and the source current is less than 100 mA.

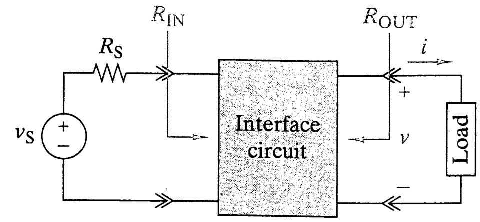


FIGURE P3–61

3–62 Figure P3–61 shows a two-port interface circuit connecting source and load circuits. In this problem v_S = 15 V, R_S = 1 kΩ, and the load is a diode whose i–v characteristic is

$$i = 10^{-15}(e^{40v} - 1)$$

Design an interface circuit that dissipates less than 50 mW and produces an interface voltage of v = 0.7 V.

3–63 Figure P3–61 shows a two-port interface circuit connecting source and load circuits. In this problem v_S = 15 V, R_S = 100 Ω, and the load is a 2-kΩ resistor. Design a resistive interface circuit so that the voltage delivered to the load is 10 V ±10% using one or more of the following standard resistors: 68 Ω, 100 Ω, 220 Ω, 330 Ω, 470 Ω, and 680 Ω. The resistors all have a tolerance of ±5%, which you must account for in your design.

3–64 In Figure P3–61 the load is a 500-Ω resistor and R_S = 75 Ω. Design an interface circuit so that the input resistance of the two-port is 75 Ω ±10% and the output resistance seen by the load is 500 Ω ±10%.

3–65 Use the resistor array in Figure P3–65 to design a two-port resistance circuit whose voltage gain $K = v_O/v_{IN}$ is at least 0.6 and whose input resistance is close to 100 Ω.

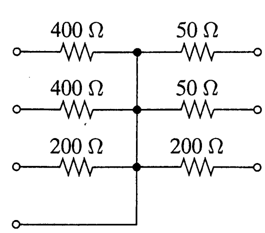


FIGURE P3–65

3–66 Figure P3–61 shows a two-port interface circuit connecting source and load circuits. In this problem $v_S = 12$ V, $R_S = 300\ \Omega$, and the load is a 50-Ω resistor. Design an interface circuit so that $v < 2$ V and $i > 40$ mA.

3–67 Figure P3–61 shows a two-port interface circuit connecting source and load circuits. In this problem $v_S = 10$ V, $R_S = 50\ \Omega$, and the load is a 50-Ω resistor. Design an interface so that 350 mW is delivered to the load.

3–68 Figure P3–61 shows a two-port interface circuit connecting a source and load. In this problem the source with $v_S = 5$ V and $R_S = 5\ \Omega$ is to be used in production testing of two-terminal semiconductor devices. The devices are to be connected as the load in Figure P3–61 and have highly nonlinear and variable i–v characteristics. The normal operating range for acceptable devices is $\{i > 10$ mA or $v > 0.7$ V$\}$ and $\{p < 10$ mW$\}$. Design an interface circuit so that the operating point always lies within the specified normal range regardless of the test article's i–v characteristic.

3–69 Figure P3–69 shows an interface circuit connecting a source circuit and a load. Design an interface circuit so that $v < 4$ V regardless of the load resistance.

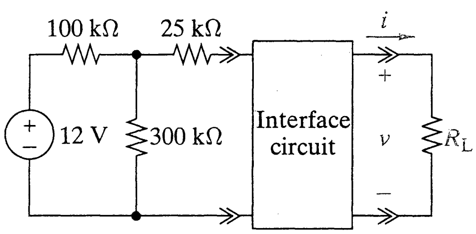


FIGURE P3–69

3–70 Design the interface circuit in Figure P3–69 so that the power delivered to the load never exceeds 1 mW regardless of the load resistance.

INTEGRATING PROBLEMS

3–71 COMPARISON OF ANALYSIS METHODS

The circuit in Figure P3–71 is called an R-2R ladder for obvious reasons. The additive property of linear circuits states that the output of the form

$$v_O = k_1 v_1 + k_2 v_2 + k_3 v_3$$

We could use superposition to find the gains k_1, k_2, and k_3. But applying the input sources one at a time may not be the best way to find these gains. The purpose of this problem is to compare two other methods.

(a) Write node-voltage equations for the circuit in Figure P3–71 using node B as the reference node. Solve these equations to show that $v_O = v_1/8 + v_2/4 + v_3/2$.

(b) We can also use circuit reduction techniques since the circuit is a ladder. Use successive source transformations and series/parallel equivalence to reduce the circuit between nodes A and B to a single equivalent voltage source connected in series with an equivalent resistor. Use this equivalent circuit to show that $v_O = v_1/8 + v_2/4 + v_3/2$.

(c) Which method do you think is easier and why?

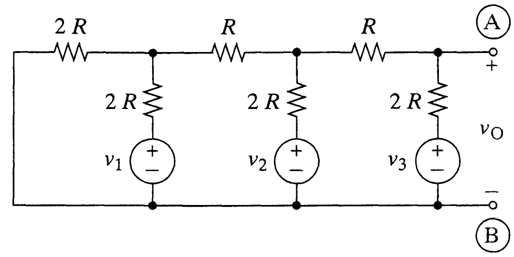


FIGURE P3–71

3–72 THREE-TERMINAL DEVICE MODELING

Figure P3–72 shows a three-terminal device with a voltage source v_S connected at the input and a 50-Ω load resistor connected at the output. The purpose of the problem is to develop an input–output relationship for the device using the following experimental data.

v_S(V)	−12	−9	−6	−3	0	+3	+6	+9	+12
v_O(V)	3	2.5	2	1	0	−1	−2	−2	−2

The device input resistance is $R_{IN} = 1$ kΩ when the 50-Ω load is connected at the output.

(a) Plot v_O versus v_S and state whether the graph is linear or nonlinear.

(b) Devise a linear model of the form $v_O = Kv_S$ that approximates the data for $|v_S| < 6$ V.

(c) Use your model from part (b) to predict the circuit output for $v_S = \pm 10$ V and explain why the predictions do not agree with the experimental results.

(d) For $v_S = 1$ V use your model from part (c) to find the circuit power gain = P_O/P_{IN}.

(e) In view of the result in (d), is the device active or passive?

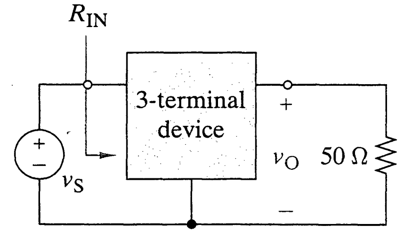


FIGURE P3–72

3–73 A ADJUSTABLE THÉVENIN EQUIVALENT

Figure P3–73 shows an ideal voltage source in parallel with an adjustable potentiometer. This problem concerns the effect of adjusting the potentiometer on the interface Thévenin equivalent circuit and the signals available at the interface.

(a) Find the parameters v_T and R_T of the Thévenin equivalent circuit at the interface in terms of circuit parameters k, v_S, and R.

(b) Find the value of R_T for $k = 0$, $k = 0.5$, and $k = 1$. Explain your results physically in terms of the position of the movable arm of the potentiometer.

(c) What is the power available at the interface for $k = 0$, $k = 0.5$, and $k = 1$? Justify your answers physically in terms of the position of the movable arm of the potentiometer.

(d) A load resistor $R_L = R/4$ is connected across the interface. Where should the potentiometer be positioned (k = ?) to transfer the maximum power to this load?

(e) A load resistor $R_L = R/4$ is connected across the interface. Where should the potentiometer be positioned (k = ?) to deliver an interface voltage $v = v_S/4$ to this load?

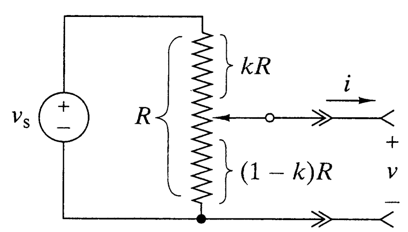


FIGURE P3–73

3–74 D BATTERY DESIGN

A satellite requires a battery with an open-circuit voltage $v_{OC} = 36$ V and a Thévenin resistance $R_T \le 10\ \Omega$. The battery is to be constructed using series and parallel combinations of one of two types of cells. The first type has $v_{OC} = 9$ V, $R_T = 4\ \Omega$, and a weight of 40 grams. The second type has $v_{OC} = 4$ V, $R_T = 0.5\ \Omega$, and a weight of 15 grams. Design a minimum weight battery to meet the open-circuit voltage and Thévenin resistance requirements.

3–75 E TTL TO ECL CONVERTER

It is claimed that the resistive circuit in Figure P3–75 converts transistor-transistor logic (TTL) input signals into output signals compatible with emitter coupled logic (ECL). Specifically, the claim is that for any output current in the range $-0.025\text{ mA} \le i \le 0.025$ mA, the circuit converts any input in the TTL low range ($0 \le v_S \le 0.4$ V) to an output in the ECL low range ($-1.7\text{ V} \le v \le -1.5$ V), and converts any input in the TTL high range ($3.0 \le v_S \le 3.8$ V) to an output in the ECL high range ($-0.9\text{ V} \le v \le -0.6$ V). The purpose of this problem is to verify this claim.

(a) The output voltage can be written in the form

$$v = k_1 v_S + k_2 i$$

Write a KCL equation at the output with the current i as an unknown and solve for the constants k_1 and k_2.

(b) Use the relationship found in (a) to verify that the output voltage falls in one of the allowed ECL ranges for every allowed combination of TTL inputs and load currents.

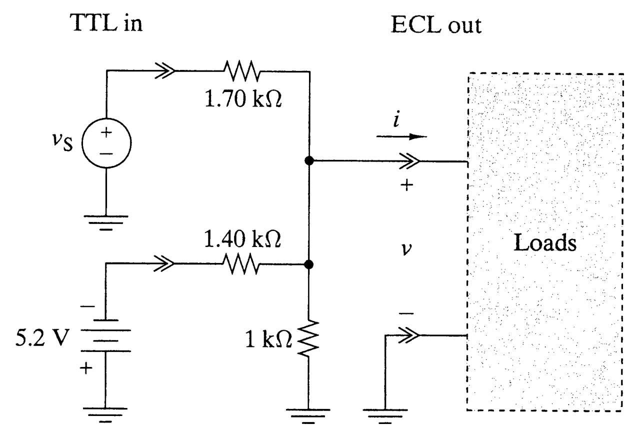


FIGURE P3–75

SUMMARY

- The output of a dependent source is controlled by a signal in a different part of the circuit. Linear dependent sources are circuit elements used to model active devices and are represented in this text by a diamond-shaped source symbol. Each type of controlled source is characterized by a single-gain parameter μ, β, r, or g.
- The Thévenin resistance of a circuit containing dependent sources can be found using the open-circuit voltage and the short-circuit current, or by directly solving for the interface i–v characteristic. The active Thévenin resistance may be significantly different from the passive lookback resistance.
- The large-signal model describes the BJT in terms of cutoff, active, and saturation modes. Each mode has a unique set of i–v characteristics. The operating mode must be determined to correctly analyze a transistor circuit. The operating mode can be determined by calculating the circuit responses assuming that the device is in the active mode and then comparing the calculated responses with known bounds.
- The OP AMP is an active device with at least five terminals: the inverting input, the noninverting input, the output, and two power supply terminals. The power supply terminals are not usually shown in circuit diagrams. The integrated circuit OP AMP is a differential amplifier with a very high voltage gain.
- The OP AMP can operate in a linear mode when there is a feedback path from the output to the inverting input. To remain in the linear mode, the output voltage is limited to the range $-V_{CC} \leq v_O \leq +V_{CC}$, where $\pm V_{CC}$ are the supply voltages.
- The i–v characteristics of the ideal model of an OP AMP are $i_P = i_N = 0$ and $v_P = v_N$. The ideal OP AMP has an infinite voltage gain, an infinite input resistance, and zero output resistance. The ideal model is a good approximation to real devices as long as the circuit gain is much smaller than the OP AMP gain.
- Four basic signal-processing functions performed by OP AMP circuits are the inverting amplifier, noninverting amplifier, inverting summer, and differential amplifier. These arithmetic operations can also be represented in block diagram form.
- OP AMP circuits can be connected in cascade to obtain more complicated signal-processing functions. The analysis and design of the individual stages in the cascade can be treated separately, provided the input resistance of the following stage is kept sufficiently high.
- OP AMP circuits are easily treated using node analysis. A node voltage is identified at each OP AMP output, but a node equation is not written at these nodes. Node equations are then written at the remaining nodes, and the ideal OP AMP input voltage constraint ($v_N = v_P$) is used to reduce the number of unknowns.
- The comparator is a nonlinear signal-processing device obtained by operating an OP AMP device without feedback. The comparator has two analog inputs and a two-state digital output.

PROBLEMS

ERO 4–1 Linear Active Circuits (Sects. 4–1, 4–2)

Given a circuit containing linear resistors, dependent sources, and independent sources, find selected output signal variables, input-output relationships, or input-output resistances.

See Examples 4–2, 4–3, 4–4, 4–5, 4–6, 4–7, 4–8 and Exercises 4–1, 4–2, 4–3, 4–5, 4–6

4–1 Find the voltage gain v_O/v_S and current gain i_O/i_x in Figure P4–1.

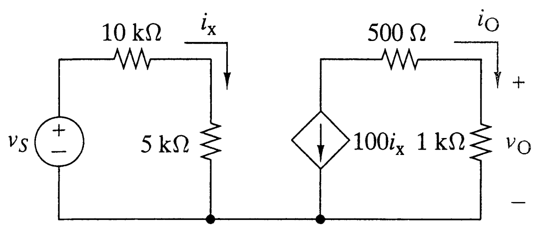


FIGURE P4–1

4–2 Find the voltage gain v_O/v_1 and the current gain i_O/i_S in Figure P4–2. For i_S = 2 mA, find the power supplied by the input source i_S and the power delivered to the 2-kΩ load resistor.

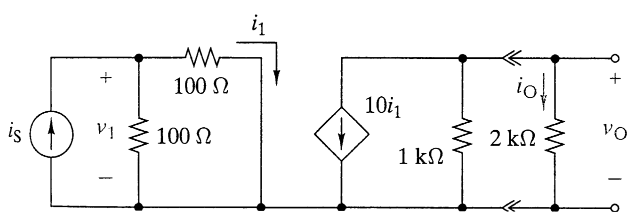


FIGURE P4–2

4–3 The circuit in Figure P4–3 is a dependent-source model of a two-stage amplifier.
Find the output voltage v_3 and the current gain i_3/i_1 when v_S = 1 mV.

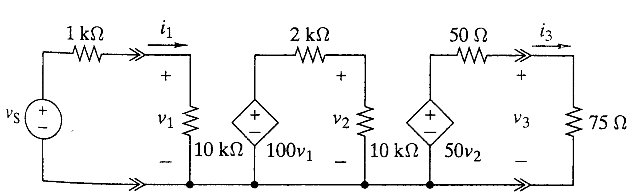


FIGURE P4–3

4–4 The circuit in Figure P4–4 is an ideal voltage amplifier with negative feedback provided via the resistor R_F.
(a) Find the output voltage v_2 and the current gain i_2/i_1 when v_S = 10 mV and R_F = 10 kΩ.
(b) Find the input resistance $R_{IN} = v_1/i_1$.

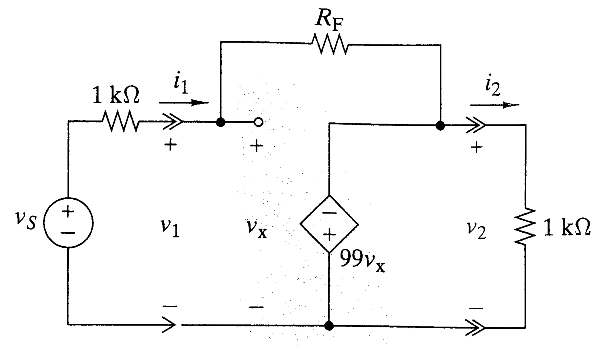


FIGURE P4–4

4–5 The circuit in Figure P4–5 is an ideal current amplifier with negative feedback via the resistor R_E.
(a) Find the output current i_2 and the voltage gain v_2/v_1 when i_S = 25 μA and R_E = 450 Ω.
(b) Find the input resistance $R_{IN} = v_1/i_1$.

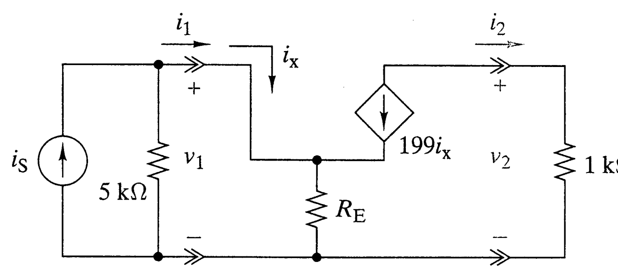


FIGURE P4–5

4–6 Find the voltage gain v_O/v_S and the current gain i_O/i_S in Figure P4–6.

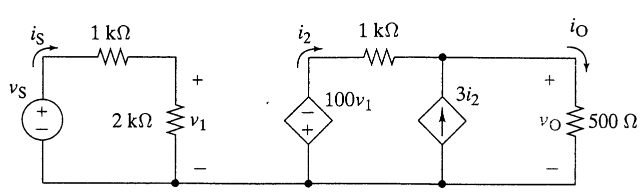


FIGURE P4–6

4–7 Find the voltage gain v_O/v_S in Figure P4–7.

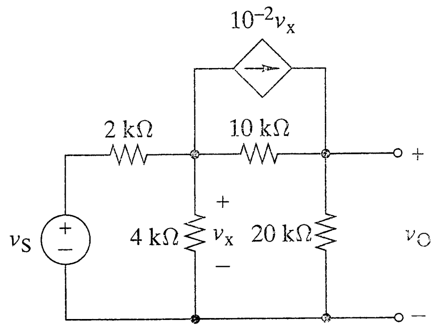


FIGURE P4–7

4–8 The circuit in Figure P4–8 is a model of a feedback amplifier using two identical transistors. Formulate either node-voltage or mesh-current equations for this circuit. Use these equations to solve for the input-output relationship $v_O = Kv_S$ using $r_\pi = 1$ kΩ, $R_E = 200$ Ω, $R_C = 10$ kΩ, $R_L = 5$ kΩ, $R_F = 5$ kΩ, and $\beta = 100$.

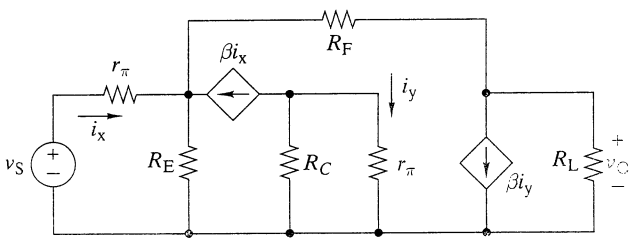


FIGURE P4–8

4–9 Find an expression for the voltage gain v_O/v_S in Figure P4–9.

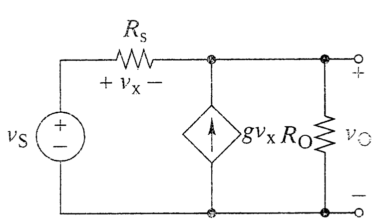


FIGURE P4–9

4–10 Find an expression for the current gain i_O/i_S in Figure P4–10.

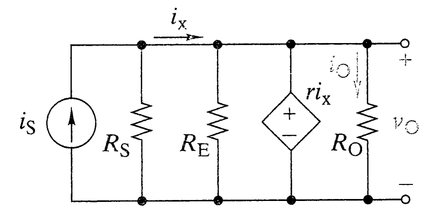


FIGURE P4–10

4–11 The circuit in Figure P4–11 is a model of a bipolar junction transistor operating in the active mode. The input signal is the current source i_S, and the voltage source V_{CC} supplies power. Find expressions for the base current i_B and the output voltage v_O in terms of V_{CC} and i_S.

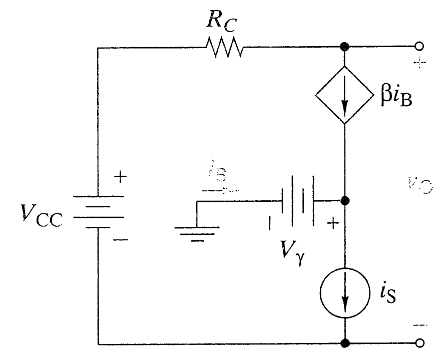


FIGURE P4–11

4–12 Find the Thévenin equivalent circuit seen by the resistor R_L in Figure P4–12.

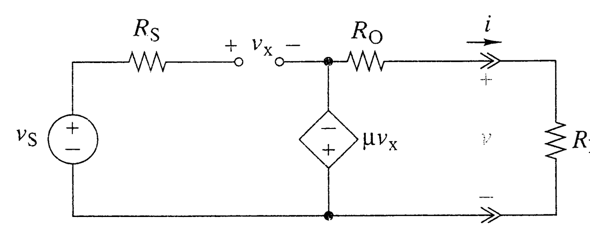


FIGURE P4–12

ERO 4–2 TRANSISTOR CIRCUITS (SECT. 4–3)

Given a linear resistive circuit with one transistor,

(a) Find the transistor operating mode and circuit responses.
(b) Select circuit parameters to obtain a specified operating mode.

See Examples 4–9, 4–10, 4–11 and Exercises 4–7, 4–8

4–13 In Figure P4–13 the circuit parameters are $R_B = 50$ kΩ, $R_C = 2$ kΩ, $\beta = 100$, $V_\gamma = 0.7$ V, and $V_{CC} = 10$ V. Find i_C and v_{CE} for $v_S = 2$ V. Repeat for $v_S = 5$ V.

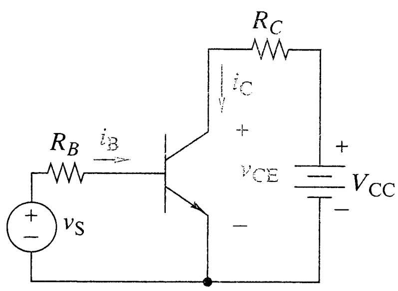


FIGURE P4–13

4–14 In Figure P4–13 the circuit parameters are $R_B = 50$ kΩ, $R_C = 5$ kΩ, $\beta = 50$, $V_\gamma = 0.6$ V, and $V_{CC} = 15$ V. Find the range of v_S for which the transistor operates in the active mode.

4–15 In Figure P4–13 the circuit parameters are $R_B = 20$ kΩ, $R_C = 470$ Ω, $\beta = 150$, $V_\gamma = 0.7$ V, and $V_{CC} = 15$ V. Find the range of v_S for which the transistor operates in the saturation mode.

4–16 In Figure P4–13 the circuit parameters are $R_C = 1$ kΩ, $\beta = 75$, $V_\gamma = 0.7$ V, $V_{CC} = 20$ V, and $v_S = 2.5$ V. Select a value of R_B so that the transistor is in the active mode with $v_{CE} = V_{CC}/2$.

4–17 In Figure P4–17 the transistor parameters are $\beta = 150$ and $V_\gamma = 0.7$ V. Find i_C and v_{CE} for $v_S = 0.5$ V. Repeat for $v_S = 1$ V.

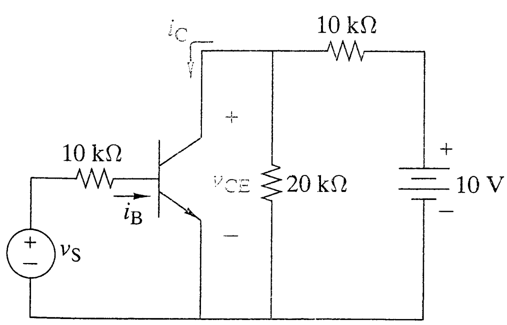


FIGURE P4–17

4–18 In Figure P4–18 the transistor parameters are $\beta = 80$ and $V_\gamma = 0.7$ V. Find i_C and v_{CE} for $v_S = 1$ V. Repeat for $v_S = 4$ V.

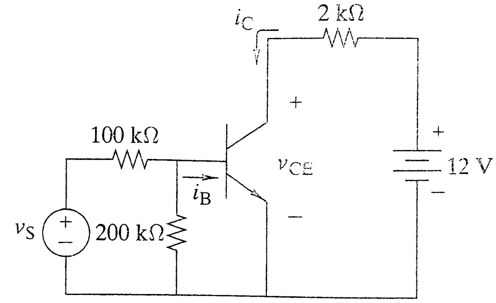


FIGURE P4–18

4–19 In Figure P4–19 the transistor parameters are $\beta = 100$ and $V_\gamma = 0.7$ V. Find i_C and v_{CE}.

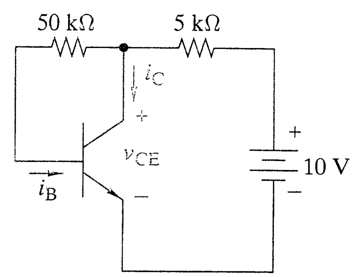


FIGURE P4–19

4–20 The input in Figure P4–20 is a series connection of a dc source V_{BB} and a signal source v_S. The circuit parameters are $R_B = 500$ kΩ, $R_C = 5$ kΩ, $\beta = 100$, $V_\gamma = 0.7$ V, and $V_{CC} = 15$ V.

(a) With $v_S = 0$, select the value of V_{BB} so that the transistor is in the active mode with $v_{CE} = V_{CC}/2$.

(b) Using the value of V_{BB} found in (a), find the range of values of the signal voltage v_S for which the transistor remains in the active mode.

(c) Plot the transfer characteristic v_{CE} versus v_S as the signal voltage sweeps across the range from −10 V to +10 V.

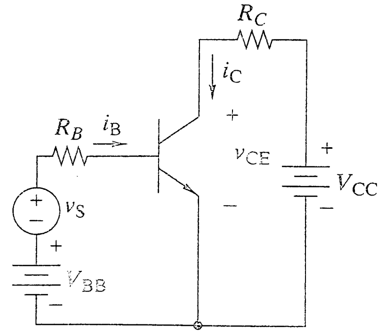


FIGURE P4–20

ERO 4–3 OP AMP CIRCUIT ANALYSIS (SECTS. 4–4, 4–5)

Given a circuit consisting of linear resistors, OP AMPs, and independent sources, find selected output signals or input-output relationships in equation or block diagram form.
See Examples 4–13, 4–14, 4–16, 4–17, 4–18, 4–19 and Exercises 4–10, 4–11, 4–12, 4–13, 4–15, 4–16

4–21 Find v_O in terms of v_S in Figure P4–21.

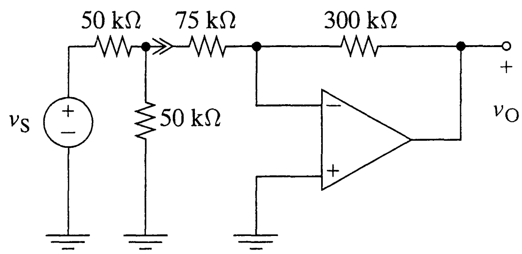


FIGURE P4–21

4–22 Find v_O in terms of v_S in Figure P4–22.

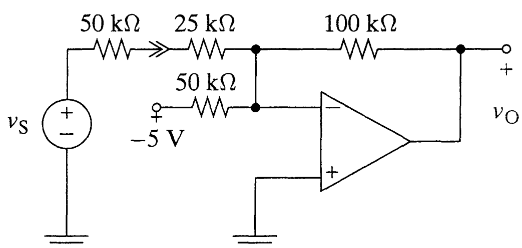


FIGURE P4–22

4–23 **(a)** Find v_O in terms v_S in Figure P4–23.
(b) Find i_O for v_S = 1.5 V.

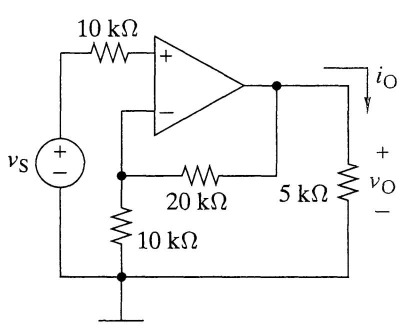


FIGURE P4–23

4–24 **(a)** Find v_O in terms of v_{S1} and v_{S2} in Figure P4–24.
(b) For V_{CC} = ±15 V and v_{S2} = 10 V, find the allowable range of v_{S1} for linear operation.

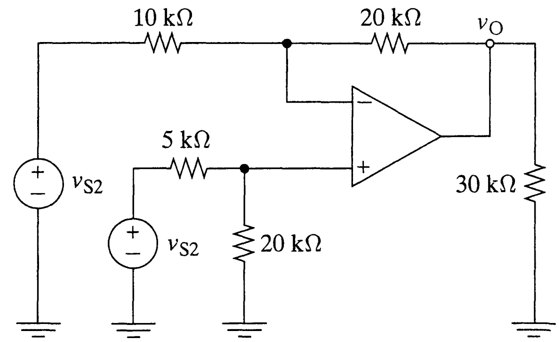


FIGURE P4–24

4–25 The input-output relationship for a three-input inverting summer is

$$v_O = -[v_1 + 3v_2 + 5v_3]$$

The resistance of the feedback resistor is 75 kΩ, and the supply voltages are V_{CC} = ±15 V.
(a) Find the values of the input resistors R_1, R_2, and R_3.
(b) For v_2 = 0.5 V and v_3 = –1 V, find the allowable range of v_1 for linear operation.

4–26 **(a)** Find v_O in terms v_S and V_{BB} in Figure P4–26.
(b) For V_{CC} = ±15 V, V_{BB} = 5 V, and R_1 = R_2, sketch the v_O versus v_S for v_S on the range from –15 V to +15 V.

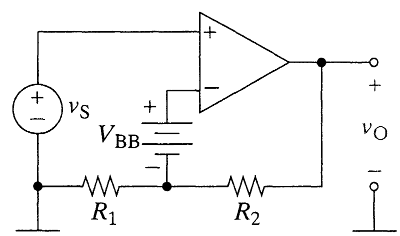


FIGURE P4–26

4–27 Find v_O in terms of v_{S1} and v_{S2} in Figure P4–27

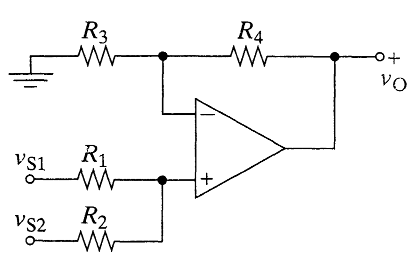


FIGURE P4–27

4–28 It is claimed that $v_O = v_S$ when the switch is closed in Figure P4–28 and that $v_O = -v_S$ when the switch is open. Prove or disprove this claim.

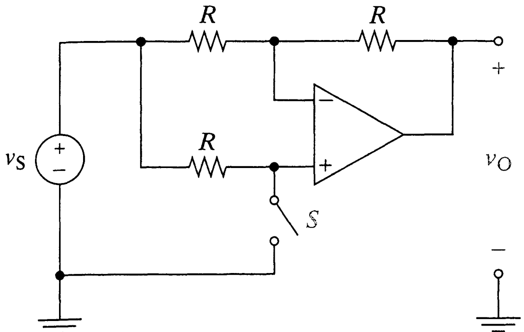


FIGURE P4–28

4–29 What range of gain is available from the circuit in Figure P4–29?

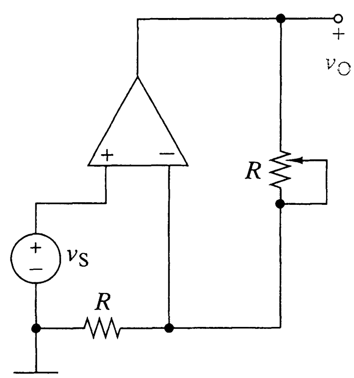


FIGURE P4–29

4–30 Find v_O in terms of v_{S1} and v_{S2} in Figure P4–30.

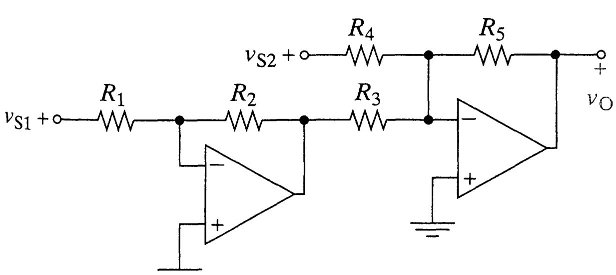


FIGURE P4–30

4–31 Find the output v_2 in terms of the input v_1 in Figure P4–31.

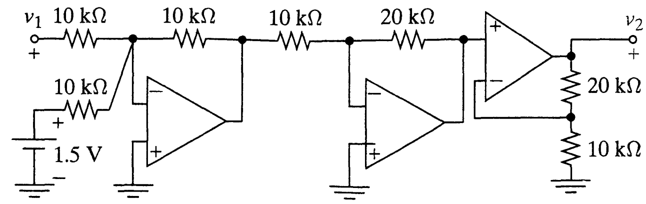


FIGURE P4–31

4–32 Find the output v_2 in terms of the input v_1 in Figure P4–32.

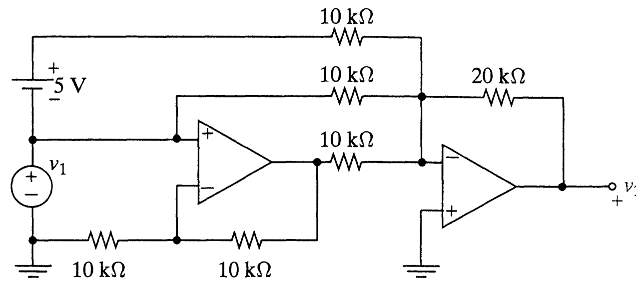


FIGURE P4–32

4–33 Find the output v_O in terms of the input v_S in Figure P4–33.

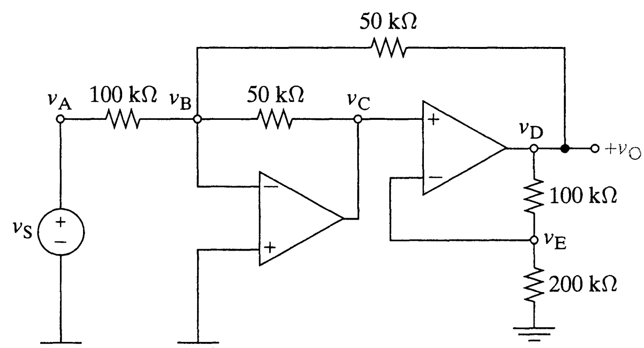


FIGURE P4–33

4–34 Find the output v_O in terms of v_1 and v_2 in Figure P4–34.

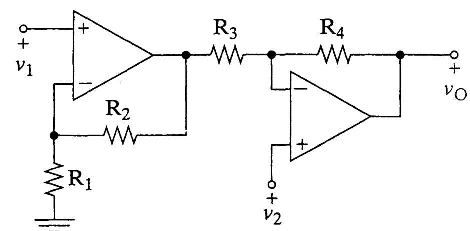


FIGURE P4–34

4–35 Find the output v_O in terms of v_1 and v_2 in Figure P4–35.

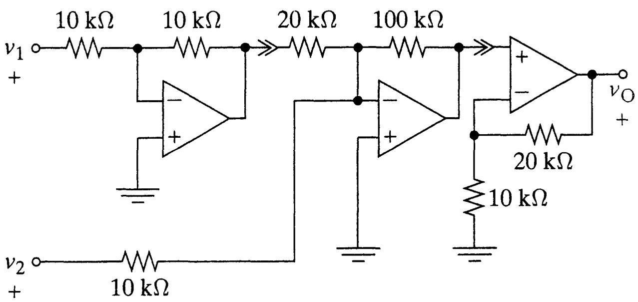


FIGURE P4–35

ERO 4–4 OP AMP CIRCUIT DESIGN (SECT. 4–6)

Given an input-output relationship, use resistors and OP AMPs to design one or more circuits that implement the relationship within stated constraints.
See Examples 4–15, 4–20, 4–21, 4–22, 4–23 and Exercise 4–16

4–36 Show how to interconnect a single OP AMP and the R-$2R$ resistor array shown in Figure P4–36 to obtain voltage gains of +1/4, +4, −1/3, and −3.

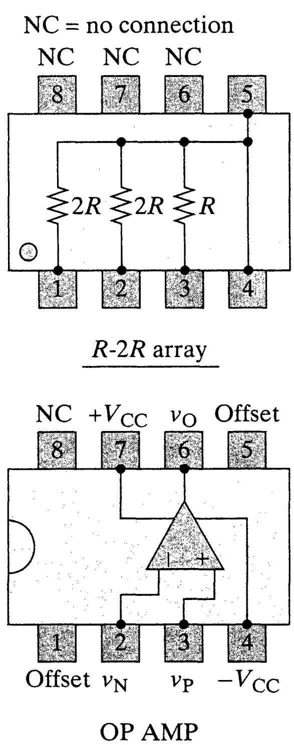


FIGURE P4–36

4–37 Design circuits using resistors and OP AMPs to implement each of the following input-output relationships:

(a) $v_O = 3v_1 - 2v_2$

(b) $v_O = 2v_1 + v_2$

4–38 Design a signal conditioning circuit for the temperature transducer whose characteristics are shown in Figure P4–38. The conditioning circuit must convert the transducer output for temperatures between −300 °C and −100 °C to a range of 0 to 5 V. The voltage gain for all stages must be less than 1000.

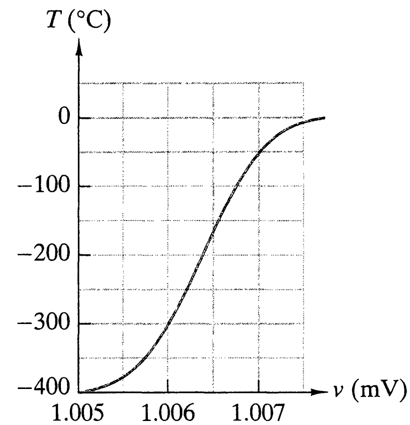


FIGURE P4–38

4–39 The resistance of a pressure transducer varies from 5 kΩ to 15 kΩ when the pressure varies over its specified operating range. Design a signal conditioning circuit to convert the sensor resistance variation to a voltage signal on the range from 0 to 5 V.

4–40 Design an OP AMP circuit that implements the block diagram in Figure P4–40 using only standard resistance values for ±5% tolerance (see Appendix A Table A–1).

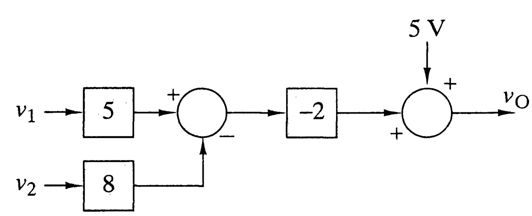


FIGURE P4–40

4–41 Design an OP AMP circuit summer that implements a 3-bit D/A converter defined by

$$v_O = K(4v_1 + 2v_2 + v_3)$$

The digital inputs (v_1, v_2, v_3) are either 0 V or 5 V. The analog output (v_O) must fall in the range of 0 V to 10 V for all possible inputs.

4–42 **D** An instrumentation system combines the outputs of three transducers into a single output using gains of -20, 3, and 18. Each transducer has a Thévenin resistance of 600 Ω and a Thévenin voltage in the range ±120 mV. Design an OP AMP circuit to meet these requirements.

4–43 **D** A requirement exists for an amplifier with a gain of –12,000 and an input resistance of at least 300 kΩ. Design an OP AMP circuit that meets the requirements using general-purpose OP AMPs with voltage gains of $A = 2 \times 10^5$, input resistances of $R_I = 4 \times 10^8$ Ω, and output resistances $R_O = 20$ Ω.

4–44 **D** The potentiometer in Figure P4–44 is used as a position sensor. The range of mechanical input moves the wiper between the bottom and the top of the potentiometer. An interface circuit is required to convert the v_P range (–15 to +15 V) to a v_O range (0 to 5 V) suitable for input to the analog-to-digital converter. Design a suitable interface circuit.

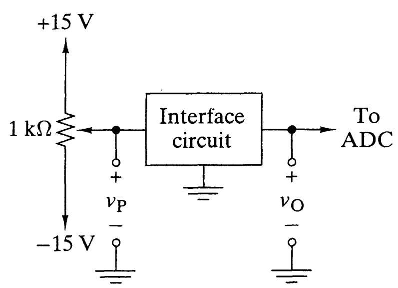


FIGURE P4–44

4–45 **D** Select the resistances in Figure P4–45 to produce the following gains.

S_1	S_1	K
open	open	10
open	closed	5
closed	x	2

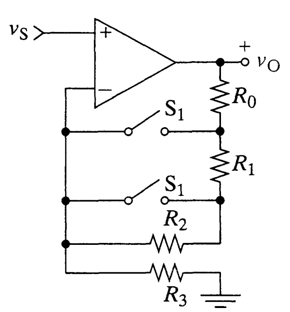


FIGURE P4–45

ERO 4–5 THE COMPARATOR (SECT. 4–7)

Given a circuit with one or more comparators, find the circuit input-output relationship.
See Examples 4–25, 4–26

4–46 The circuit in Figure P4–46 has V_{OH} = 15 V and V_{OL} = 0 V.

(a) Determine the input voltage ranges for which $v_O = V_{OH}$ and $v_O = V_{OL}$.

(b) Sketch the circuit transfer characteristics for v_S on the range from –15 V to +15 V.

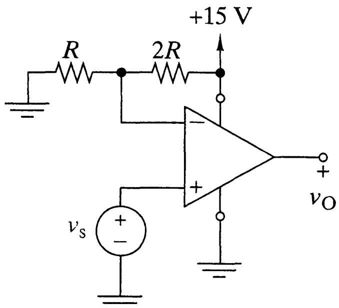


FIGURE P4–46

4–47 The circuit in Figure P4–47 has V_{OH} = 10 V and V_{OL} = 0 V.

(a) Determine the input voltage ranges for which $v_O = V_{OH}$ and $v_O = V_{OL}$.

(b) Sketch the circuit transfer characteristics for v_S on the range from –15 V to +15 V.

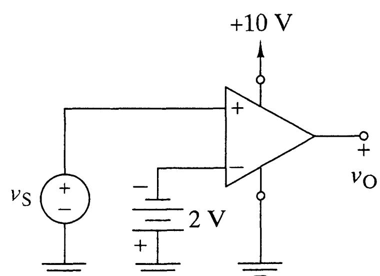


FIGURE P4–47

4–48 The circuit in Figure P4–48 is called a window detector. In this circuit the OP AMP saturation levels are $\pm V_{CC}$. For V_{CC} = 15 V, V_{AA} = 10 V, and V_{BB} = 5 V, show that output is determined by the following statement:

If $(-V_{BB} < v_S < V_{AA})$ then v_O = 15 V else v_O = 0.

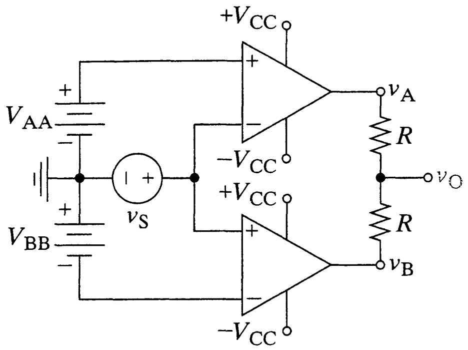


FIGURE P4–48

4–49 The circuit in Figure P4–49 has $V_{CC} = 15$ V and $V_{BB} = -5$ V.

(a) Determine the input voltage ranges for which $v_O = V_{OH}$ and $v_O = V_{OL}$.

(b) Sketch the circuit transfer characteristics for v_S on the range from −10 V to +10 V.

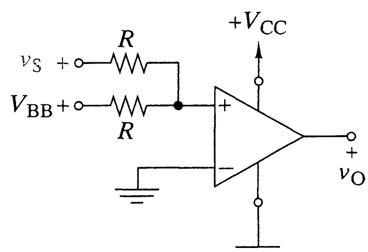


FIGURE P4–49

4–50 Repeat Problem 4–49 with $V_{BB} = 5$ V.

4–51 The circuit in Figure P4–51 has $V_{CC} = 15$ V and $V_{BB} = 5$ V. Sketch the output voltage v_O on the range $0 \leq t \leq 2$ s for $v_S = 10\sin(2\pi t)$ V.

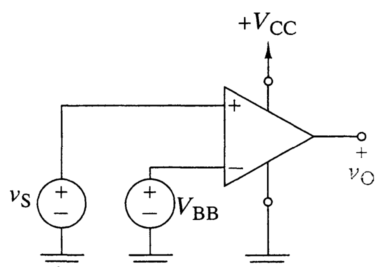


FIGURE P4–51

4–52 Repeat Problem 4–51 with $V_{BB}(t) = 10t$ V.

INTEGRATING PROBLEMS

4–53 BRIDGED-T INVERTING AMPLIFIER

Using the basic inverting OP AMP configuration to obtain a large voltage gain requires a small input resistor, a large feedback resistor, or both. Small input resistors load the input source, and large ($R > 1$ MΩ) feedback resistors have more noise and exhibit greater life-cycle variations. The circuit in Figure P4–53 circumvents these problems by using a bridged-T circuit in the feedback path. Note that R_3 occurs twice in this diagram.

(a) Show that the gain of the circuit in Figure P4–53 can be written as $K = -R_{FDBK}/R_1$, where R_{FDBK} is the effective feedback resistance defined as:

$$R_{FDBK} = R_3\left(2 + \frac{R_3}{R_2}\right)$$

(b) Design a basic inverting amplifier to achieve $K = -400$ and $R_{IN} \geq 20$ kΩ.

(c) Design a bridged-T inverting amplifier to achieve $K = -400$ and $R_{IN} \geq 20$ kΩ.

(d) Evaluate the two designs by comparing their element counts, element spreads (ratio of largest over smallest resistance), and total resistances (sum of all resistances).

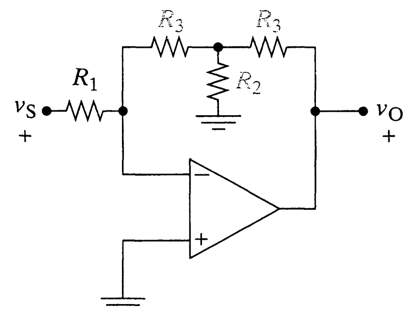


FIGURE P4–53

4–54 HYBRID CIRCUIT ANALYSIS

The two-port interface circuit in Figure P4–54 is a small-signal model of a bipolar junction transistor using what are called hybrid parameters. The analysis of this circuit illustrates that it can be useful to use a mixture (or hybrid) of mesh-current and node-voltage equations.

(a) Using the symbolic notation in the figure, write a mesh-current equation for the input circuit and a node-voltage equation for the output circuit.

(b) Using $R_S = 2$ kΩ, $R_1 = 5$ kΩ, $R_2 = 50$ kΩ, $R_L = 150$ kΩ, $\mu = 10^{-3}$, and $\beta = 50$, solve the equations from (a) for the input current i_1 and the output voltage v_2 in terms of the input v_S.

(c) Using the results from (b), solve for the input resistance and the voltage gain of the circuit.

(d) Calculate the power gain defined as the ratio of the power delivered to R_L divided by the power supplied by v_S.

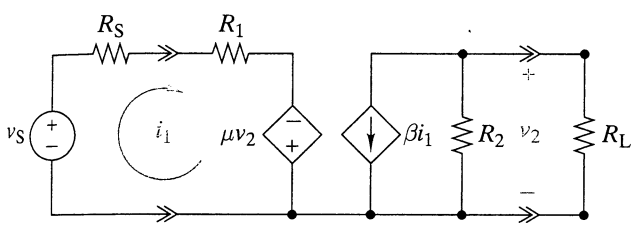


FIGURE P4–54

4–55 WHEATSTONE BRIDGE AMPLIFIER

The circuit in Figure P4–55 shows a Wheatstone bridge consisting of three equal resistors and a fourth resistor that is a transducer whose resistance is $R + \Delta R$, where $\Delta R << R$. The bridge is excited by a constant reference voltage source V_{REF} and is connected to the inputs of an OP AMP. For $\Delta R << R$ the OP AMP output voltage can be expressed in the form

$$v_O = K\left[\frac{\Delta R}{R}\right] V_{REF}$$

(a) Verify that this expression is correct and express K in terms of circuit parameters.

(b) For $V_{REF} = 15$ V, $R = 100$ Ω and $\Delta R/R$ in the range ±0.04%, select value R_F so that the output voltage v_O falls in the range ±3 V.

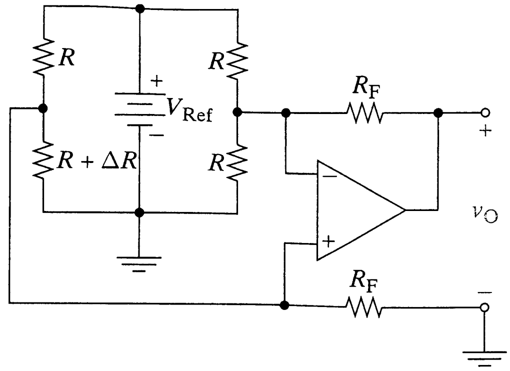


FIGURE P4–55

4–56 TEMPERATURE SENSOR DESIGN

Figure P4–56 shows a circuit with a semiconductor temperature sensor modeled as a temperature-controlled current source. The device senses absolute temperature T_A (°K) and delivers a current kT_A, where $k = 1$ μA/°K. The purpose of the OP AMP circuit is to make the output voltage proportional to °C. For $V_{CC} = 10$ V, select values for R_1 and R_2 so that output voltage sensitivity is 100 mV/°C.

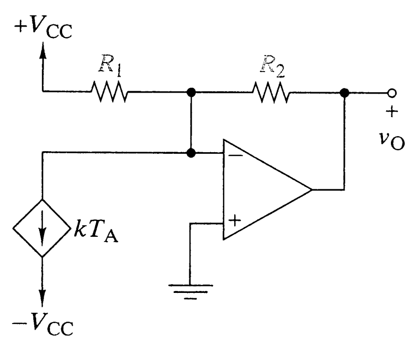


FIGURE P4–56

4–57 SUBTRACTOR CIRCUITS

The input-output relationship for both circuits in Figure P4–57 are of the form $v_O = K_2v_2 + K_1v_1$.

(a) For circuits C1 and C2, determine the constants K_1 and K_2 in terms of circuit parameters.

(b) In circuit C1 with $R_1 = R_2 = 1$ kΩ and $R_3 = R_5 = 10$ kΩ, select the values R_4 and R_6 that produce $v_O = 5(v_2 - v_1)$.

(c) Repeat part (b) for circuit C2.

(d) Evaluate the two designs by comparing the number of devices required and the load they impose on the input signal sources.

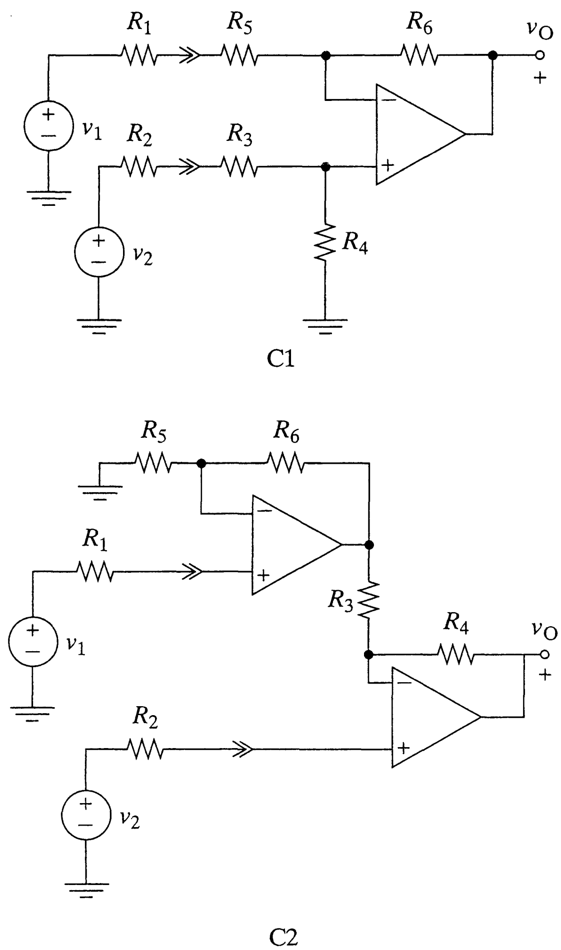


FIGURE P4-57

4-58 PHOTORESISTOR INSTRUMENTATION

Both circuits in Figure P4–58 contain a photoresistor R_X whose resistance varies inversely with the intensity of the incident light. In complete darkness its resistance is 10 kΩ. In bright sunlight its resistance is 2 kΩ. At any given light level the circuit is linear, so its input-output relationship is of the form $v_O = Kv_1$.

(a) For circuits C1 and C2, determine the constant K in terms of circuit resistances.

(b) For circuit C1 with $v_1 = +15$ V, select the values of R and R_F so that $v_O = -10$ V in bright sunlight and +10 V in complete darkness.

(c) Repeat part (b) for circuit C2.

(d) Evaluate the two designs by comparing the number of devices required and the total power dissipated.

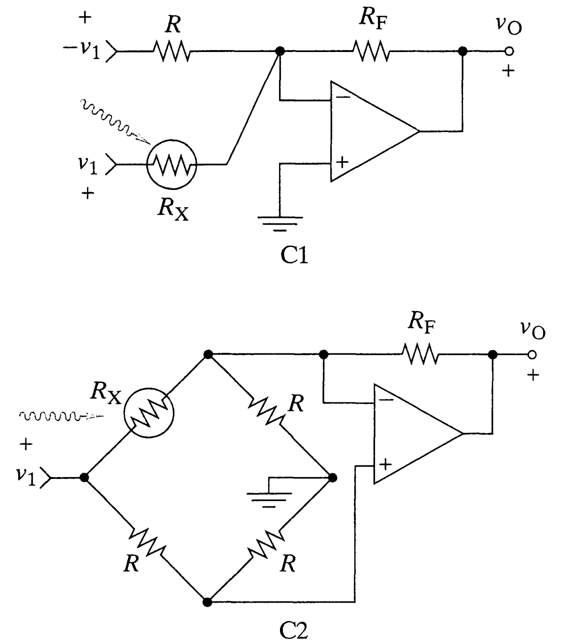


FIGURE P4-58

4-59 DESIGN EVALUATION

As chief engineer of a small electronics company, you find yourself with a dilemma. Your two engineering interns have worked independently and have produced different solutions for the design problem you gave them. Their proposed solutions are shown in Figure 4–59.

You asked them to design a circuit with three inputs v_1, v_2, v_3, and an output v_O. The output is to be proportional to $v_1/16 + v_2/8 + v_3/4$. The output can be either positive or negative, but must be able to drive a 500-Ω load. A ±15 V dc power supply is available within the system without added cost. You need to manufacture 2 million of these circuits, so part costs are a concern, but performance is the top priority. Electrical characteristics and cost data for available parts are as follows.

PART TYPE	PART CHARACTERISTICS	RELATIVE COST
Standard resistors	1.0, 1.5, 2.2, 3.3, 4.7, 6.8 Ω and multiples of 10 thereof	$4000 per 100,000
Custom resistors	Values to three significant figures from 100 Ω to 200 kΩ	$4500 per 100,000
OP AMPs	Minimum voltage gain 100,000 Output voltage range ±15 V Maximum output current 10 mA	$11,500 per 100,000

(a) Verify whether both circuits comply with the performance requirements. If not, explain how one or both can be modified to comply.

(b) Which of the two circuits would you select for production and why?

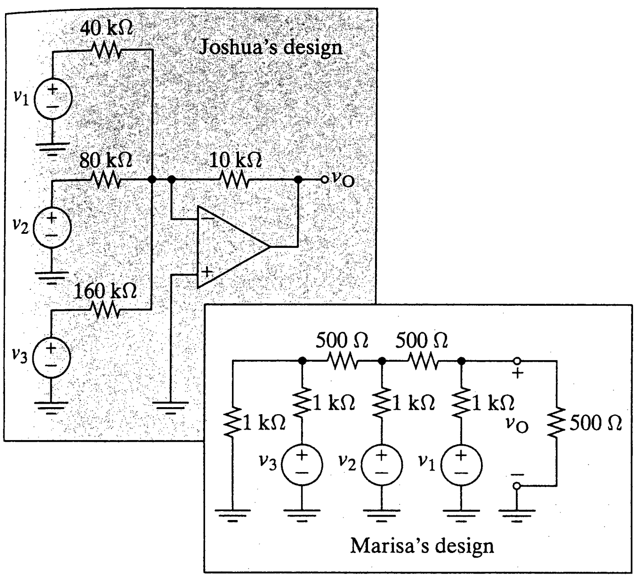


FIGURE P4–59

4–60 COMPUTER-AIDED CIRCUIT DESIGN

Use computer-aided circuit analysis to find the value of R_F in Figure P4–60 that causes the input resistance seen by i_S to be 50 Ω. Find the current gain i_O/i_S for this value of R_F. Use $\beta = 100$, $r_\pi = 1.1$ kΩ, $R_C = 10$ kΩ, $R_E = 100$ Ω, and $R_L = 100$ Ω.

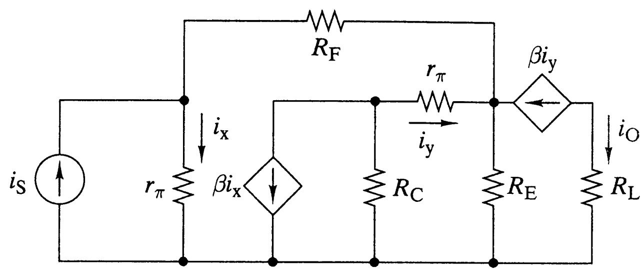
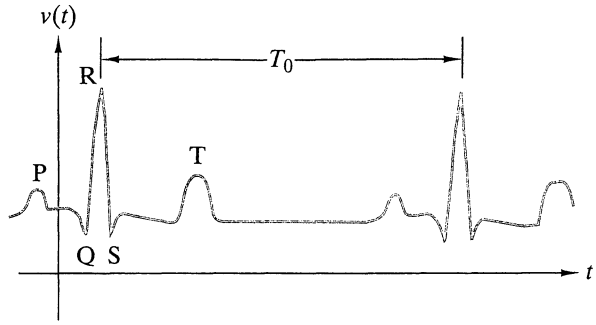


FIGURE P4–60

conditions allow the trained clinician to diagnose the situation, especially when abnormal features occur in certain combinations. However, it is not our purpose to discuss the medical interpretation of ECG waveform abnormalities. Rather, this examples illustrates that bioelectric signals carry information and that the information is decoded by analyzing the signal's partial waveform descriptors.

FIGURE 5-28



SUMMARY

- A waveform is an equation or graph that describes a voltage or current as a function of time. Most signals of interest in electrical engineering can be derived using three basic waveforms: the step, exponential, and sinusoid.
- The step function is defined by its amplitude and time-shift parameters. The impulse, step, and ramp are called singularity functions and are often used as test inputs for circuit analysis purposes.
- The exponential waveform is defined by its amplitude, time constant, and time-shift parameter. For practical purposes, the duration of the exponential waveform is five time constants.
- A sinusoid can be defined in terms of three types of parameters: *amplitude* (either V_A or the Fourier coefficients a and b), *time shift* (either T_S or the phase angle ϕ), and *time/frequency* (either T_0 or f_0 or ω_0).
- Many composite waveforms can be derived using the three basic waveforms. Some examples are the impulse, ramp, damped ramp, damped sinusoid, exponential rise, and double exponential.
- Partial descriptors are used to classify or describe important signal attributes. Two important temporal attributes are periodicity and causality. Periodic waveforms repeat themselves every T_0 seconds. Causal signals are zero for $t < 0$. Some important amplitude descriptors are peak value V_p, peak-to-peak value V_{pp}, average value V_{avg}, and root-mean-square value V_{rms}.
- A spectrum is an equation or graph that defines the amplitudes and phase angles of sinusoidal components contained in a signal. The signal bandwidth (B) is a partial descriptor that defines the range of frequencies outside of which the component amplitudes are less than a specified value. Periodic signals can be resolved into a dc component and a sum of ac components at harmonic frequencies.

PROBLEMS

ERO 5–1 BASIC WAVEFORMS (SECTS. 5–2, 5–3, 5–4)

Given an equation, graph, or word description of a step, exponential, or sinusoid waveform,

(a) Construct an alternative description of the waveform.
(b) Find the parameters or properties of the waveform.
(c) Find new waveforms by summing, integrating, or differentiating the given waveform.

See Examples 5–1, 5–2, 5–3, 5–5, 5–6, 5–7, 5–8, 5–9 and Exercises 5–1, 5–2, 5–3, 5–4, 5–5, 5–6, 5–7

5–1 Graph the following step function waveforms:
(a) $v_1(t) = 5u(t)$ V
(b) $v_2(t) = -5u(t-2)$ V
(c) $v_3(t) = v_1(t) + v_2(t)$ V
(d) $v_4(t) = v_1(t) - v_2(t)$ V

5–2 Graph the waveforms obtained by integrating the waveforms in Problem 5-1.

5–3 Use step functions to write an expression for a rectangular pulse with amplitude V_A, duration T, and centered at $t = 0$.

5–4 A waveform $v(t)$ is –5 V for t in the range 5 ms $\leq t \leq$ 3 ms and +5 V elsewhere. Write an equation for the waveform using step functions.

5–5 A waveform $v(t)$ is zero for $t = 0$, rises linearly to 5 V at $t = 2$ ms, and abruptly drops to zero thereafter. Write an equation for the waveform using singularity functions.

5–6 Find the amplitude and time constant of each of the following exponential waveforms. Graph each of the waveforms.
(a) $v_1(t) = [10\, e^{-2t}]u(t)$ V
(b) $v_2(t) = [10\, e^{-t/2}]u(t)$ V
(c) $v_3(t) = [-10\, e^{-20t}]u(t)$ V
(d) $v_4(t) = [-10\, e^{-t/20}]u(t)$ V

5–7 Graph the waveforms obtained by differentiating the first two waveforms in Problem 5-6.

5–8 An exponential waveform starts at $t = 0$ and decays to 4 V at $t = 5$ ms and 2 V at $t = 6$ ms. Find the amplitude and time constant of the waveform.

5–9 The value of an exponential waveform is 5 V at $t =$ 5 ms and 3.5 V at $t = 7$ ms. What is its value at $t = 2$ ms?

5–10 By direct substitution show that the exponential function $v(t) = V_A e^{-\alpha t}$ satisfies the following first-order differential equation:

$$\frac{dv(t)}{dt} + \alpha v(t) = 0$$

5–11 Find the period, frequency, amplitude, time shift, and phase angle of the following sinusoids:
(a) $v_1(t) = 10\cos(2000\pi t) + 10\sin(2000\pi t)$ V
(b) $v_2(t) = -30\cos(2000\pi t) - 20\sin(2000\pi t)$ V
(c) $v_3(t) = 10\cos(2\pi t/10) - 10\sin(2\pi t/10)$ V
(d) $v_4(t) = -20\cos(800\pi t) + 30\sin(800\pi t)$ V

5–12 Find the period, frequency, amplitude, time shift, and phase angle of the sum of the first two sinusoids in Problem 5–11.

5–13 A sinusoid has an amplitude of 15 V. At $t = 0$ the value of a sinusoid is 10 V and its slope is positive. Find the Fourier coefficients of the waveform.

5–14 A sinusoid has a frequency of 5 MHz, a value of –10 V at $t = 0$, and reaches its first positive peak at $t = 125$ ns. Find its amplitude, phase angle, and Fourier coefficients.

5–15 Find the frequency, period, and Fourier coefficients of the following sinusoids:
(a) $v_1(t) = 20\cos(4000\pi t - 180°)$ V
(b) $v_2(t) = 20\cos(4000\pi t - 90°)$ V
(c) $v_3(t) = 30\cos(2\pi t/400 - 45°)$ V
(d) $v_4(t) = 60\sin(2000\pi t + 45°)$ V

5–16 Find the frequency, period, phase angle, and amplitude of the sum of the first two sinusoids in Problem 5-15.

5–17 A 100 kHz sinusoid has an amplitude of 75 V and passes through 0 V with a positive slope at $t = 5$ μs. Find the Fourier coefficients, phase angle, and time shift of the waveform.

ERO 5–2 COMPOSITE WAVEFORMS (SECT. 5–5)

Given an equation, graph, or word description of a composite waveform,

(a) Construct an alternative description of the waveform.
(b) Find the parameters or properties of the waveform.
(c) Find new waveforms by integrating, or differentiating the given waveform.

See Examples 5–10, 5–11, 5–12, 5–13, 5–14, 5–15 and Exercises 5–8, 5–9

5–18 Graph the following waveforms:
(a) $v_1(t) = 10\,[1 - 2e^{-200t}\sin(1000\pi t)]u(t)$ V
(b) $v_2(t) = [20 - 10e^{-1000t}]u(t)$ V
(c) $v_3(t) = 10\,[2 - \sin(1000\pi t)]u(t)$ V
(d) $v_4(t) = 10\,[4 - 2e^{-1000t}]u(t)$ V

5–19 The damped ramp waveform can be written as $v(t) = V_A \alpha t e^{-\alpha t} u(t)$. Find the maximum value of the waveform and the time at which the maximum occurs.

5–20 A waveform is known to be of the form $v(t) = V_A - V_B\, e^{-\alpha t}$. At $t = 0$ the value of the waveform is 8 V, at $t = 5$ μs its value is 9 V, and it approaches 10 V for large values of t. Find the values of V_A, V_B, and α.

5–21 A waveform is known to be of the form $v(t) = V_A e^{-\alpha t} \sin \beta t$. The waveform periodically passes through zero every 2.5 ms. At $t = 1$ ms its value is 3.5 V and at $t = 2$ ms it is 0.8 V. Find the values of V_A, α, and β, and then graph the waveform.

5–22 Write an expression for the first cycle of the periodic waveform in Figure P5–22.

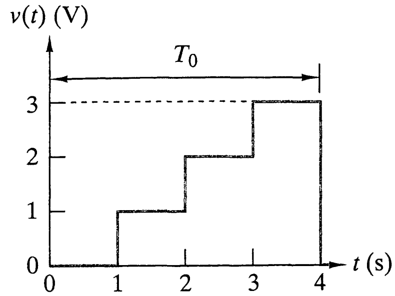


FIGURE P5–22

5–23 Write an expression for the first cycle of the periodic waveform in Figure P5–23.

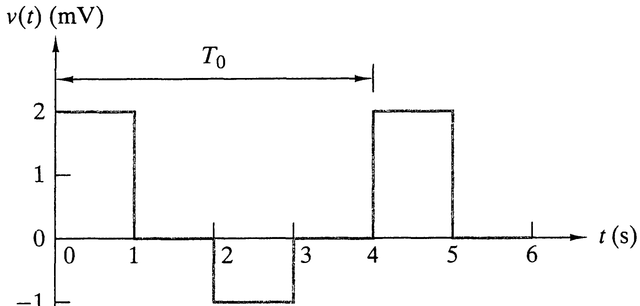


FIGURE P5–23

5–24 A waveform is known to be of the form $v(t) = V_A - V_B \sin \beta t$. At $t = 0$ the value of the waveform is 5 V, and it periodically reaches a minimum value of −2 V every 5 μs. Find the values of V_A, V_B, and β, and then graph the waveform.

5–25 Write an equation for the periodic waveform in Figure P5–25.

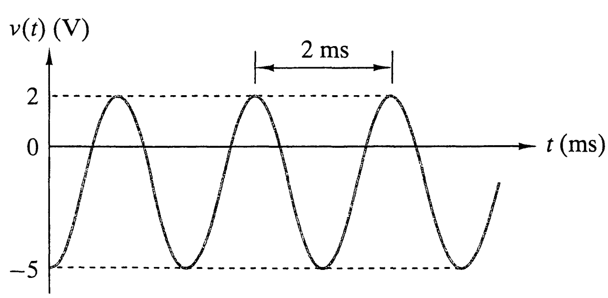


FIGURE P5–25

5–26 Write an expression for the derivative of the periodic waveform in Figure P5–25.

5–27 Write an equation for the first cycle of the periodic waveform in Figure P5–27 and then graph the waveform obtained by differentiating the signal.

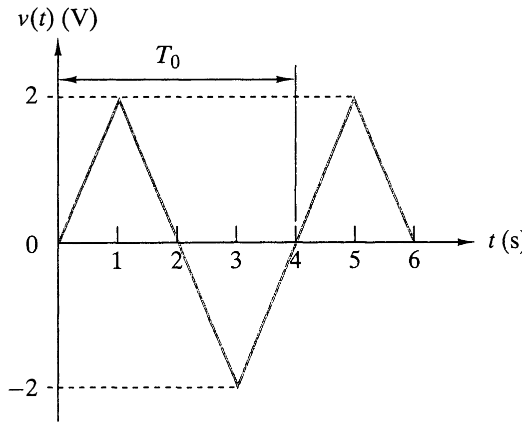


FIGURE P5–27

5–28 The exponential rise waveform $v(t) = V_A(1 - e^{-\alpha t})\,u(t)$ is zero at $t = 0$ and monotonically approaches a final value as $t \to \infty$. What is the final value and for what value of t does the waveform reach 50% of this value?

5–29 Figure P5–29 shows a plot of the waveform $v(t) = V_A[e^{-\alpha t} \sin \beta t]u(t)$. Find the values of V_A, α, and β.

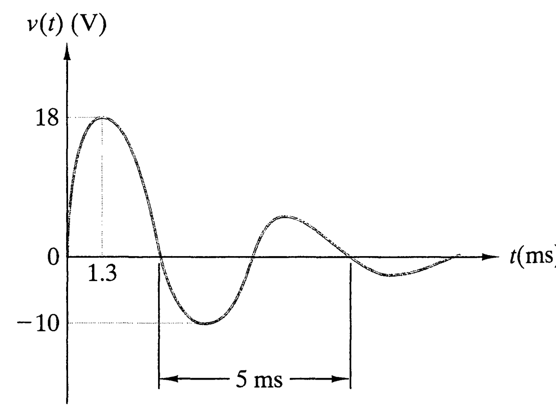


FIGURE P5–29

5–30 The basic waveform $u(x)$ is zero for all $x < 0$. The function $f(t) = u(\cos t)$ defines a periodic waveform. Sketch the waveform of cos t and then sketch $f(t)$. Is the $f(t)$ zero for all $t < 0$? If not, why not? How would you describe $f(t)$? Is it periodic? If so, what is the period of $f(t)$? How would you modify the function to change its period and peak amplitude?

ERO 5–3 WAVEFORM PARTIAL DESCRIPTORS (SECT. 5–6)

Given a complete description of a basic or composite waveform,

(a) Classify the waveform as periodic or aperiodic and causal or noncausal.
(b) Find the applicable partial waveform descriptors.
(c) Find the parameters of a waveform given its partial descriptors.

See Examples 5–16, 5–17 and Exercises 5–10, 5–11, and 5–12

5–31 Classify the following waveforms as periodic or aperiodic and causal or noncausal. Find V_p and V_{pp} for all of the waveforms. Find V_{rms} and V_{avg} for those waveforms that are periodic.

(a) $v_1(t) = [150 - 80\sin(2000\pi t)]u(t)$ V
(b) $v_2(t) = 40[\sin(2000\pi t)][u(t) - u(t-1)]$ V
(c) $v_3(t) = 15\cos(2000\pi t) + 10\sin(2000\pi t)$ V
(d) $v_4(t) = [10 - 5e^{-400t}]u(t)$ V

5–32 Find V_p, V_{pp}, V_{rms}, and V_{avg} for each of the sinusoids in Problem 5-11.

5–33 Find V_p, V_{pp}, V_{rms}, and V_{avg} for each of the sinusoids in Problem 5-15.

5–34 Find V_p, V_{pp}, V_{rms}, and V_{avg} for the periodic waveform Figure P5-22.

5–35 Find V_p, V_{pp}, V_{rms}, and V_{avg} for the periodic waveform Figure P5-23.

5–36 In digital data communications the *time constant of fall* is defined as the time required for a pulse to fall from 70.7% to 26.0% of its maximum value. Assuming that the pulse decay is exponential, find the relationship between the time constant of fall and the time constant of the exponential decay.

5–37 The waveform $v(t) = V_0 + 10\cos(200\pi t)$ is applied at the input of an OP AMP voltage follower with $V_{CC} = \pm 15$ V. What range of values of the dc component V_0 ensures that the OP AMP does not saturate?

5–38 The first cycle ($t > 0$) of a periodic waveform with $T_0 = 70$ ms can be expressed as

$$v(t) = 2u(t) - 3u(t - 0.01) + 5u(t - 0.06) \quad \text{V}$$

Sketch the waveform and find V_{max}, V_{min}, V_p, V_{pp}, and V_{avg}.

5–39 A periodic waveform can be expressed as

$$v(t) = 100 - 200\cos 2000\,\pi t - 75\sin 40000\,\pi t + 35\cos 80000\,\pi t \quad \text{mV}$$

What is the period of the waveform? What is the average value of the waveform? What is the amplitude of the fundamental component? What is the highest frequency in the waveform?

5–40 The first cycle ($0 \le t < T_0$) of a periodic clock pulse train is

$$v(t) = V_A[u(t) - u(t - T)] \quad \text{V}$$

The duty cycle of the clock pulse is defined as the fraction of the period during which the pulse is not zero. Derive an expression for the average value of the clock pulse train in terms of V_A and the duty cycle $D = T/T_0$.

INTEGRATING PROBLEMS

5–41 THE SPICE EXPONENTIAL SIGNAL

The SPICE circuit simulation language defines a composite exponential waveform as

$$v(t) = \begin{cases} V_0 + (V_1 - V_0)\,(1 - e^{-t/T_{C1}}) & 0 \le t \le T_D \\ V_0 + (V_1 - V_0)\,(1 - e^{-T_D/T_{C1}})\, e^{-(t-T_D)/T_{C2}} & T_D < t \end{cases}$$

What is the value of the waveform at $t = 0$? At $t = T_D$? What is the value of the waveform as t approaches infinity? What is the maximum amplitude of the waveform? Sketch the waveform on the range from $t = 0$ to $t = T_D + 2T_{C2}$. What is the practical duration of the waveform?

5–42 ANALOG-TO-DIGITAL CONVERSION

Figure P5–42 shows a circuit diagram of an analog-to-digital converter based on a voltage divider and OP AMPs operating without feedback. Each OP AMP operates as a comparator whose output is $V_{OH} = 10$ V when $v_P > v_N$ and $V_{OL} = 0$ V when $v_P < v_N$. The input signal $v_S(t)$ is applied to all of the noninverting inputs simultaneously. The voltages applied to the inverting inputs come from the four-resistor voltage divider shown. For an input voltage of $v_S(t) = 25e^{-2000t}$ V, express the output voltages $v_A(t)$, $v_B(t)$, $v_C(t)$, and $v_D(t)$ in terms of step functions.

5–43 DIGITAL-TO-ANALOG CONVERSION

Figure P5–43 shows a 3-bit digital-to-analog converter of the type discussed in Sect. 4–6. The circuit consists of an R-$2R$ ladder connected to the inverting input to the OP AMP. The ladder circuit is driven by three digital input signals $v_1(t)$, $v_2(t)$, and $v_3(t)$.

(a) Show that the input-output relationship for the OP AMP circuit is

$$v_O(t) = -\frac{R_F}{8R}[4v_1 + 2v_2 + v_3]$$

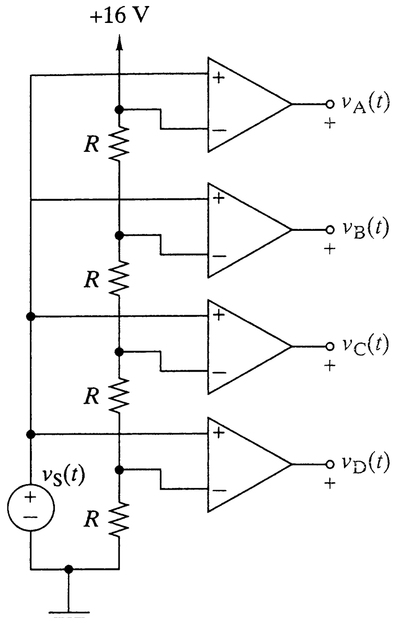


FIGURE P5–42

(b) The digital input signals can be expressed in terms of step functions as follows:

$$v_1(t) = 5u(t-1) - 5u(t-5) \text{ V}$$

$$v_2(t) = 5u(t-3) - 5u(t-4) + 5u(t-6) - 5u(t-10) \text{ V}$$

$$v_3(t) = 5u(t) - 5u(t-4) + 5u(t-8) \text{ V}$$

Plot each digital waveform separately and stack the plots on top of each other with $v_1(t)$ at the bottom and $v_3(t)$ at the top. A stacked plot of digital signals is called a *timing diagram*.

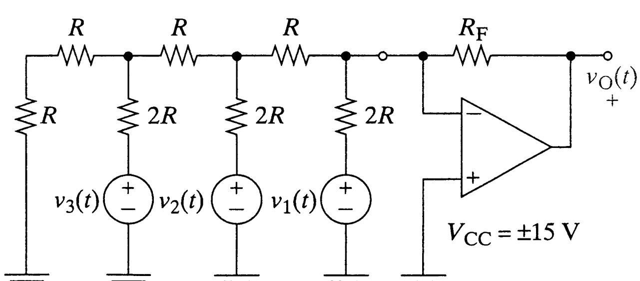


FIGURE P5–43

(c) For $R_F = R$, use the input-output relationship in (a) and the input timing diagram in (b) to obtain a plot of the output voltage in the range $0 < t < 10$ s.

5–44 TIMING DIAGRAMS

Timing diagrams are separate plots of digital waveforms that are stacked on top of each other to show how signals change over time and to reveal temporal relationships between signals. Timing diagrams are widely used to analyze, design, and evaluate digital circuits and systems. Timing diagrams waveforms can take on only two states: 0 (low) and 1 (high). The temporal points at which waveforms transition from one state to another are called **edges**. Thus, waveforms are described by the temporal location of their edges and the state of the signals following each edge.

A 3-bit binary counter has outputs $(D_2\ D_1\ D_0)$. At $t = 0$ the outputs are in the zero state, that is, $(D_2\ D_1\ D_0) = (0\ 0\ 0)$. Thereafter, the outputs undergo the following state transitions.

000--->001--->010--->011--->100--->
101--->110--->111--->000

The first transition occurs at $t = 50$ ns and subsequent transitions occur every 50 ns.

(a) Sketch a timing diagram for these signals with D_2 at the bottom and D_0 at the top.

(b) A digital signal D_4 is 1 (high) when D_2 AND D_0 are high and is 0 (low) otherwise. Add D_4 at the bottom of the timing diagram in (a).

(c) The outputs feed a digital-to-analog converter whose output is

$$v_O(t) = D_0 + 2D_1 + 4D_2$$

Add the analog waveform $v_O(t)$ at the bottom of the timing diagram in (b).

5–45 FOURIER SERIES

Reasonably well behaved periodic waveforms can be expressed as a sum of sinusoidal components called a Fourier series. For example, the sum

$$v(t) = \frac{V_A}{2} - \sum_{n=1}^{n=\infty} \frac{V_A}{n\pi} \sin(2\pi n f_0 t)$$

is the Fourier series of one of the periodic waveforms in Figure 5–2. Use a spreadsheet or math solver to plot the sum of the first 10 terms of this series for $V_A = 10$ V and $f_0 = 50$ kHz. Use a time interval $0 \leq t \leq 2T_0$. Can you identify this waveform in Figure 5–2?

5–46 A VOLTMETER CALIBRATION

Most dc voltmeters measure the average value of the applied signal. A dc meter that measures the average value can be adapted to indicate the rms value of an ac signal. The input is passed through a rectifier circuit. The rectifier output is the absolute value of the input and is applied to a dc meter whose deflection is proportional to the average value of the rectified signal. The meter scale is calibrated to indicate the rms value of the input signal. A calibration factor is needed to convert the average absolute value into the rms value of the ac signal. What is the required calibration factor for a sinusoid? Would the same calibration factor apply to a square wave?

To determine dc responses, we replace capacitors by open circuits and inductors by short circuits and analyze the resulting resistance circuit using any of the methods in Chapters 2 through 4. The circuit analysis involves only resistance circuits and yields capacitor voltages and inductor currents along with any other variables of interest. Computer programs like SPICE use this type of dc analysis to find the initial operating point of a circuit to be analyzed. The dc capacitor voltages and inductor currents become initial conditions for a transient response that begins at $t = 0$ when something in the circuit changes, such as the position of a switch.

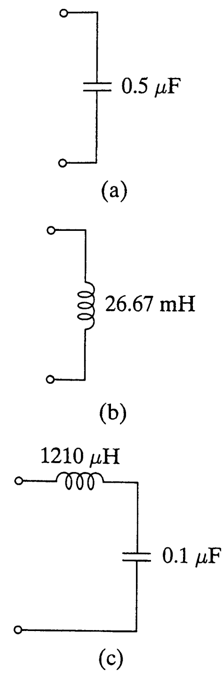


FIGURE 6–28

EXAMPLE 6–15

Determine the voltage across the capacitors and current through the inductors in Figure 6–29(a).

SOLUTION:

The circuit is driven by a 5-V dc source. Figure 6–29(b) shows the equivalent circuit under dc conditions. The current in the resulting series circuit is $5/(50 + 50) = 50$ mA. This dc current exists in both inductors, so $i_{L1} = i_{L2} =$ 50 mA. By voltage division the voltage across the 50-Ω output resistor is $v = 5 \times 50/(50 + 50) = 2.5$ V; therefore, $v_{C1}(0) = 2.5$ V. The voltage across C_2 is zero because of the short circuits produced by the two inductors.

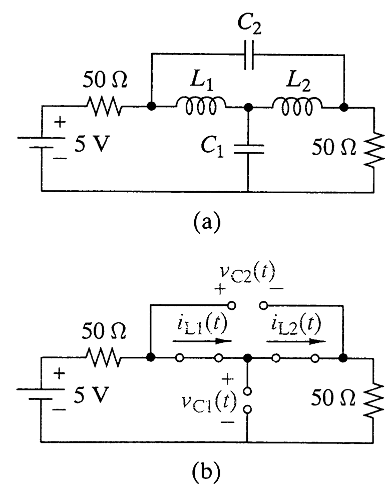


FIGURE 6–29

Exercise 6–11

Find the OP AMP output voltage in Figure 6–30.

Answer:

$$v_O = \frac{R_2 + R_1}{R_1} V_{dc}$$

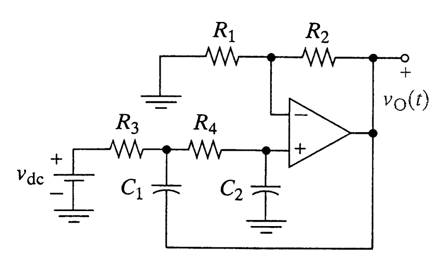


FIGURE 6–30

SUMMARY

- The linear capacitor and inductor are dynamic circuit elements that can store energy. The instantaneous element power is positive when they are storing energy and negative when they are delivering previously stored energy. The net energy transfer is never negative because inductors and capacitors are passive elements.
- The current through a capacitor is zero unless the voltage is changing. A capacitor acts like an open circuit to dc excitations.
- The voltage across an inductor is zero unless the current is changing. An inductor acts like a short circuit to dc excitations.
- Capacitor voltage and inductor current are called state variables because they define the energy state of a circuit. Circuit state variables are continuous functions of time as long as the circuit driving forces are finite.
- OP AMP capacitor circuits perform signal integration or differentiation. These operations, together with the summer and gain functions, provide the building blocks for designing dynamic input-output characteristics.

- Capacitors or inductors in series or parallel can be replaced with an equivalent element found by adding the individual capacitances or inductances or their reciprocals. The dc response of a dynamic circuit can be found by replacing all capacitors with open circuits and all inductors with short circuits.

PROBLEMS

ERO 6–1 CAPACITOR AND INDUCTOR RESPONSES (SECTS. 6–1, 6–2)

(a) Given the current through a capacitor or an inductor, find the voltage across the element.
(b) Given the voltage across a capacitor or an inductor, find the current through the element.
(c) Find the power and energy associated with a capacitor or inductor.

See Examples 6–1, 6–2, 6–3, 6–4, 6–6, 6–7, 6–8 and Exercises 6–1, 6–2, 6–3, 6–4, 6–5, 6–6

6–1 For $t \geq 0$ the voltage across a 2-μF capacitor is $v_C(t) = 3\,e^{-4000t}$ V. Derive expressions for $i_C(t)$, $p_C(t)$, and $w_C(t)$. Is the capacitor absorbing power, delivering power, or both?

6–2 A voltage of $15 \cos(2\pi 1000t)$ appears across a 3.3-μF capacitor. Find the energy stored on the capacitor at $t =$ 0.5, 0.75, and 1 ms.

6–3 For $t \geq 0$ the current through a 100-mH inductor is $i_L(t) = 30\,e^{-4000t}$ mA. Derive expressions for $v_L(t)$, $p_L(t)$, and $w_L(t)$. Is the inductor absorbing power, delivering power, or both?

6–4 For $t \geq 0$ the current through a 25-μF capacitor is $i_C(t) = 50[u(t) - u(t - 5\times10^{-3})]$ mA. Prepare sketches of $v_C(t)$ and $p_C(t)$. Is the capacitor absorbing power, delivering power, or both?

6–5 At $t = 0$ the voltage across a 200-nF capacitor is $v_C(0) = 30$ V. For $t > 0$, the current through the capacitor is $i_C(t) = 0.4 \cos 10^5 t$ A. Derive an expression for $v_C(t)$.

6–6 The voltage across a 0.5-μF capacitor is shown in Figure P6–6. Prepare sketches of $i_C(t)$, $p_C(t)$, and $w_C(t)$. Is the capacitor absorbing power, delivering power, or both?

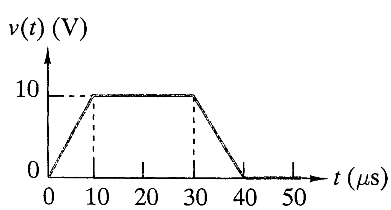


FIGURE P6–6

6–7 The current through a 10-nF capacitor is shown in Figure P6–7. Given that $v_C(0) = -5$ V, find the value of $v_C(t)$ at $t = 5$, 10, and 20 μs.

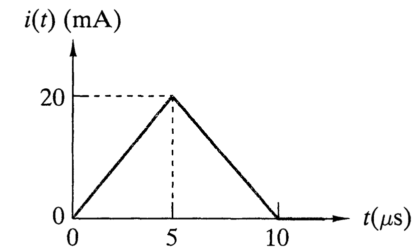


FIGURE P6–7

6–8 At $t = 0$ the current through a 10-mH inductor is $i_L(0) = 1$ mA. For $t \geq 0$ the voltage across the inductor is $v_L(t) = 50e^{-5000t}$ mV. Derive an expression for $i_L(t)$. Is the inductor absorbing power, delivering power, or both?

6–9 For t > 0 the current through a 500-mH inductor is $i_L(t) = 10\,e^{-2000t} \sin 1000t$ mA. Derive expressions for $v_L(t)$, $p_L(t)$, and $w_L(t)$. Is the inductor absorbing power, delivering power, or both?

6–10 A voltage $v_L(t) = 5 \cos(1000t) - 2 \sin(3000t)$ V appears across a 50-mH inductor. Derive an expression for $i_L(t)$. Assume $i_L(0) = 0$. Discuss the effect of frequency on the relative amplitudes of the sinusoidal components in $v_L(t)$ and $i_L(t)$.

6–11 For t > 0 the voltage across a 50-nF capacitor is $v_C(t) = -100e^{-1000t}$ V. Derive an expression for $i_C(t)$. Is the capacitor absorbing power, delivering power, or both?

6–12 The current through a 25-mH inductor is shown in Figure P6–7. Prepare sketches of $v_L(t)$, $p_L(t)$, and $w_L(t)$.

6–13 The voltage across a 100-μH inductor is shown in Figure P6–6. The inductor current is observed to be zero at $t = 5$ μs. What is the value of $i_L(0)$?

6–14 The capacitor in Figure P6–14 carries an initial voltage $v_C(0) = 25$ V. At $t = 0$, the switch is closed, and thereafter the voltage across the capacitor is $v_C(t) = 50 - 25\,e^{-5000t}$ V. Derive expressions for $i_C(t)$ and $p_C(t)$ for $t > 0$. Is the capacitor absorbing power, delivering power, or both?

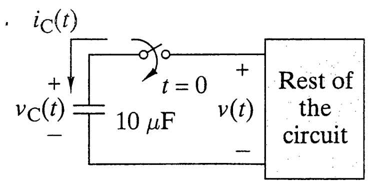


FIGURE P6–14

6–15 The capacitor in Figure P6–14 carries an initial voltage $v_C(0) = 0$ V. At $t = 0$, the switch is closed, and thereafter the voltage across the capacitor is $v_C(t) = 10(1 - e^{-1000t})$ V. Derive expressions for $i_C(t)$ and $p_C(t)$ for $t > 0$. Is the capacitor absorbing or delivering power?

6–16 The inductor in Figure P6–16 carries an initial current of $i_L(0) = 20$ mA. At $t = 0$, the switch opens, and thereafter the current into the rest of the circuit is $i(t) = -20\,e^{-500t}$ mA. Derive expressions for $v_L(t)$ and $p_L(t)$ for $t > 0$. Is the inductor absorbing or delivering power?

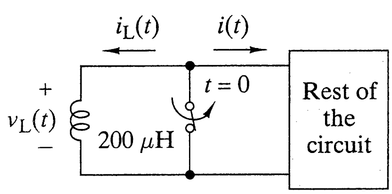


FIGURE P6–16

6–17 The inductor in Figure P6–16 carries an initial current of $i_L(0) = -20$ mA. At $t = 0$, the switch opens, and thereafter the current into the rest of the circuit is $i(t) = 40 - 20\,e^{-500t}$ mA. Derive expressions for $v_L(t)$ and $p_L(t)$ for $t > 0$. Is the inductor absorbing or delivering power?

6–18 A 2.2-μF capacitor is connected in series with a 200-Ω resistor. The voltage across the capacitor is $v_C(t) = 10\cos(2000t)$ V. What is the voltage across the resistor?

6–19 A 300-mH inductor is connected in parallel with a 10-kΩ resistor. The current through the inductor is $i_L(t) = 10\,e^{-1000t}$ mA. What is the current through the resistor?

6–20 For t > 0 the current through a 2-mH inductor is $i_L(t) = 100te^{-1000t}$ A. Derive an expression for v_L(t). Is the inductor absorbing power or delivering power at $t = 0.5$, 1, and 2 ms?

ERO 6–2 Dynamic OP AMP Circuits (Sect. 6–3)

(a) Given a circuit consisting of resistors, capacitors, and OP AMPs, determine its input–output relationship and use the relationship to find the output for specified inputs.

(b) Design an OP AMP circuit to implement a given input–output relationship or a block diagram.

See Examples 6–9, 6–10, 6–11, 6–12 and Exercises 6–7, 6–8, 6–9

6–21 Find the input–output relationship of the OP AMP circuit in Figure P6–21. *Hint*: the voltage at the inverting input is $v_N(t) = v_S(t)$.

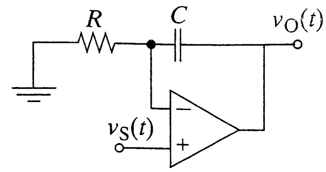


FIGURE P6–21

6–22 Show that the OP AMP capacitor circuit in Figure P6–22 is a noninverting integrator whose input–output relationship is

$$v_O(t) = \frac{1}{RC}\int_0^t v_S(x)dx$$

Hint: By voltage division the voltage at the inverting input is $v_N(t) = v_O(t)/2$.

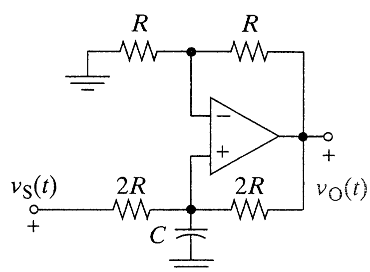


FIGURE P6–22

6–23 Find the input–output relationship of the OP AMP circuit in Figure P6–23. *Hint*: the circuit has two inputs.

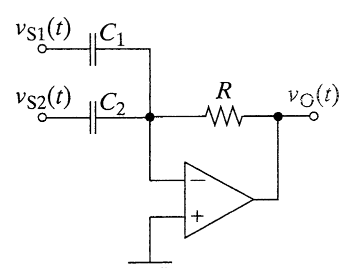


FIGURE P6–23

6–24 In Figure P6–24 the voltage across the capacitor at $t = 0$ is such that $v_O(0) = -10$ V. The input signal is $v_S(t) = 5u(t)$ V. Derive an equation for the output voltage for the OP AMP in its linear range. If the OP AMP saturates at ±15 V, find the time when the OP AMP saturates.

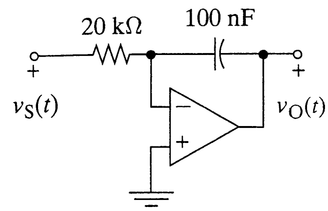


FIGURE P6–24

6–25 In Figure P6–24 the voltage across the capacitor at $t = 0$ is 0 V. The input signal is a rectangular pulse $v_S(t) = 5[u(t) - u(t - T)]$ V. The OP AMP saturates at ±15 V. What is the maximum pulse duration for linear operation?

6–26 At $t = 0$ the voltage across the capacitor in Figure P6–24 is zero. The OP AMP saturates at ±15 V. For $v_S(t) = 5[\sin \omega t]u(t)$ V, derive an expression for the output voltage for the OP AMP in its linear range. What is the minimum value of ω for linear operation?

6–27 The input to the circuit in Figure P6–27 is $v_S(t) = V_A[\sin 10^6 t]u(t)$ V. Derive an expression for the output voltage for the OP AMP in its linear range. The OP AMP saturates at ±15 V. What is the maximum value of V_A for linear operation?

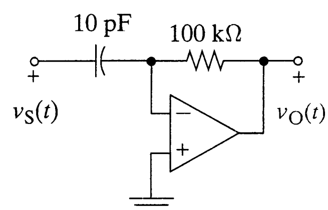


FIGURE P6–27

6–28 The input to the circuit in Figure P6–27 is $v_S(t) = 5[\sin \omega t]u(t)$ V. Derive an expression for the output voltage for the OP AMP in its linear range. The OP AMP saturates at ±15 V. What is the maximum value of ω for linear operation?

6–29 The input to the circuit in Figure P6–27 is $v_S(t) = 5[e^{-\alpha t}]u(t)$ V. Derive an expression for the output voltage for the OP AMP in its linear range. If the OP AMP saturates at ±15 V, what is the maximum value of α for linear operation?

6–30 Construct a block diagram for the following input–output relationship:

$$v_O(t) = -5v_S(t) - 20\int_0^t v_S(x)dx$$

6–31 Construct a block diagram for the following input–output relationship:

$$v_O(t) = 5v_S(t) + \frac{1}{20}\frac{dv_S(t)}{dt}$$

6–32 What is the input–output relationship of the block diagram in Figure P6–32.

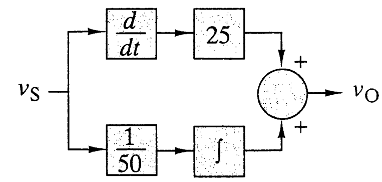


FIGURE P6–32

6–33 **D** Design an OP AMP circuit to implement the input–output relationship in Problem 6–30.

6–34 **D** Design an OP AMP circuit to implement the input–output relationship in Problem 6–31.

6–35 **D** Design OP AMP *RC* circuits to implement the input–output relationship of the block diagram in Figure P6–32.

ERO 6–3 EQUIVALENT INDUCTANCE AND CAPACITANCE (SECT. 6–4)

(a) Derive equivalence properties of inductors and capacitors or use equivalence properties to simplify *LC* circuits.
(b) Solve for currents and voltages in *RLC* circuits with dc input signals.

See Examples 6–14, 6–15, and Exercise 6–10, 6–11

6–36 Find a single equivalent element for each circuit in Figure P6–36.

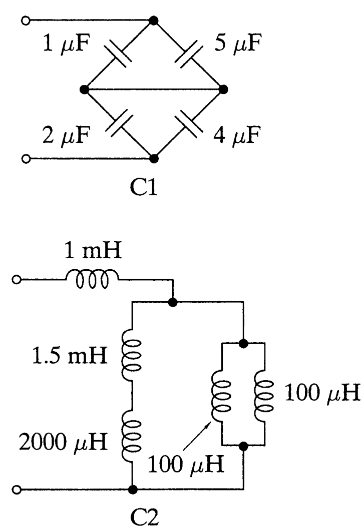


FIGURE P6–36

6–37 Verify Eqs. (6–30) and (6–31).

6–38 A 3-mH inductor is connected in series with a 100-μH inductor and the combination connected in parallel with a 12-mH inductor. Find the equivalent inductance of the connection.

6–39 A series connection of a 3.3-μF capacitor and a 4.7-μF capacitor is connected in parallel with a series connection of two 6.8-μF capacitors. Find the equivalent capacitance of the connection.

6–40 Find the equivalent capacitance between terminals A and B in Figure P6–40.

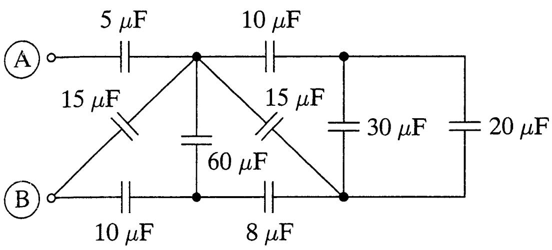


FIGURE P6–40

6–41 Figure P6–41 is the equivalent circuit of a two-wire feed through capacitor.

(a) What is the capacitance between terminal 1 and ground?

(b) What is the capacitance between terminal 1 and ground when terminal 2 is grounded?

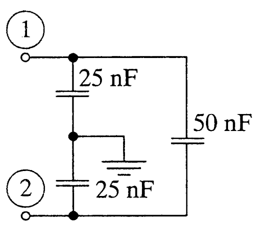


FIGURE P6–41

6–42 **D** A capacitor bank is required that can be charged to 5 kV and store at least 250 J of energy. Design a series/parallel combination that meets the voltage and energy requirements using 20-μF capacitors each rated at 1.5 kV max.

6–43 Figure P6–43 shows a power inductor package containing two identical inductors. When terminal 2 is connected to terminal 4 the inductance between terminals 1 and 3 is 260-μH.

(a) What is the inductance between terminals 1 and 3 when terminal 1 is connected to terminal 4?

(b) What is the inductance between terminals 1 and 3 when terminal 1 is connected to terminal 4 and terminal 2 is connected to terminal 3?

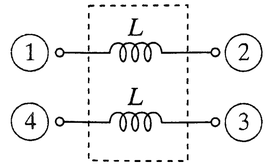


FIGURE P6–43

6–44 The circuits in Figure P6–44 are driven by dc sources. Find the voltage across capacitors and the current through inductors.

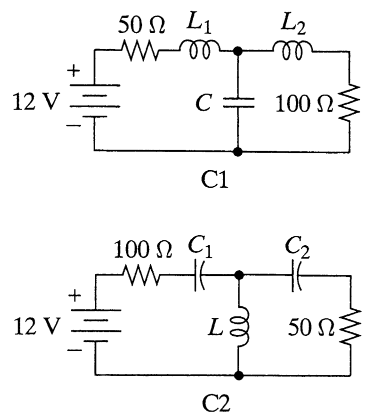


FIGURE P6–44

6–45 The OP AMP circuits in Figure P6–45 are driven by dc sources. Find the output voltage v_O.

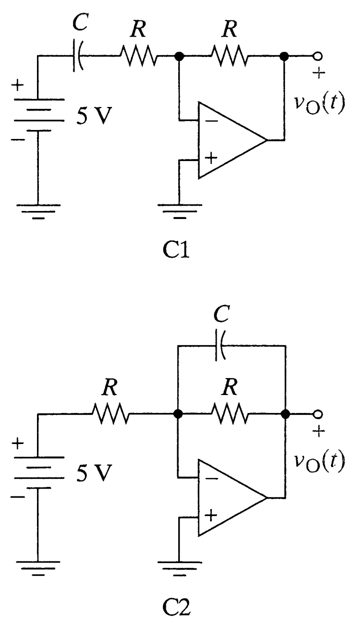


FIGURE P6–45

INTEGRATING PROBLEMS

6–46 A CAPACITIVE DISCHARGE PULSER

A capacitor bank for a large pulse generator consists of 11 capacitor strings connected in parallel. Each string consists of 16 1.5-mF capacitors connected in series. The purpose of this problem is to calculate important characteristics of the pulser.

(a) What is the total equivalent capacitance of the bank?

(b) If each capacitor in a series string is charged to 300 V, what is the total energy stored in the bank?

(c) In the discharge mode the voltage across the capacitor bank is $v(t) = 4.8[e^{-500t}]u(t)$ kV. What is the peak power delivered by the capacitor bank?

(d) For practical purposes the capacitor bank is completely discharged after about five time constants. What is the average power delivered during that interval?

6–47 A LC CIRCUIT RESPONSE

In the circuit shown in Figure P6–47 the initial capacitor voltage is $v_C(0) = 30$ V. At $t = 0$ the switch is closed, and thereafter the current into the rest of the circuit is

$$i(t) = 2(e^{-2000t} - e^{-8000t}) \quad \text{A}$$

The purpose of this problem is to find the voltage $v(t)$ and the equivalent resistance looking into the rest of the circuit.

(a) Use the inductor's i–v characteristic to find $v_L(t)$ for $t \geq 0$. Find the value of $v_L(t)$ at $t = 0$.

(b) Use the capacitor's i–v characteristic to find $v_C(t)$ for $t \geq 0$. Find the value of $v_C(t)$ at $t = 0$. Does this value agree with the initial condition given in the problem statement? If not, you need to review your work to find the error.

(c) Use KVL and the results from (a) and (b) to find the voltage $v(t)$ delivered to the rest of the circuit. What is the value of $v(t)$ at $t = 0$?

(d) The $v(t)$ found in (c) should be proportional to the $i(t)$ given in the problem statement. If so, what is the equivalent resistance looking into the rest of the circuit?

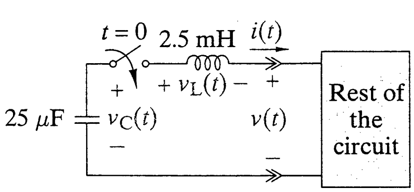


FIGURE P6–47

6–48 A CAPACITOR MULTIPLIER

It is claimed that the i–v characteristic at the input interface in Figure P6–48 is

$$i(t) = C_{EQ}\frac{dv(t)}{dt}$$

where $C_{EQ} = (1 + R_2/R_1)C$. Since $C_{EQ} > C$ the circuit is called a capacitor multiplier.

(a) Prove or disprove this claim.

(b) If the initial capacitor voltage $v_C(0) = V_0$, what is the initial value of the input voltage $v(0)$?

(c) If the initial energy stored in the capacitor is $w_C(0) = W_0$, what is the initial energy stored in equivalent capacitor C_{EQ}?

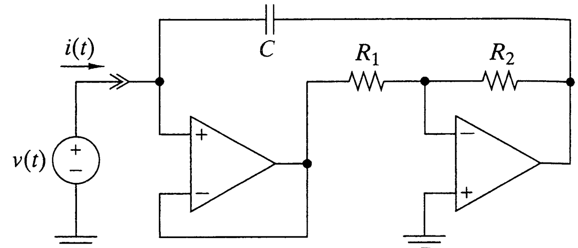


FIGURE P6–48

6–49 A INDUCTOR SIMULATION CIRCUIT

Circuits that simulate an inductor can be produced using resistors, OP AMPs, and a capacitor. It is claimed that the i–v characteristic at the input interface in Figure P6–49 is

$$i(t) = \frac{1}{L_{EQ}}\int_0^t v(x)\,dx$$

where $L_{EQ} = R_1R_2C$.

(a) Prove or disprove this claim.

(b) If the initial capacitor voltage $v_C(0) = V_0$, what is the initial value of the input current $i(0)$?

(c) If the initial energy stored in the capacitor is $w_C(0) = W_0$, what is the initial energy stored in equivalent inductor L_{EQ}?

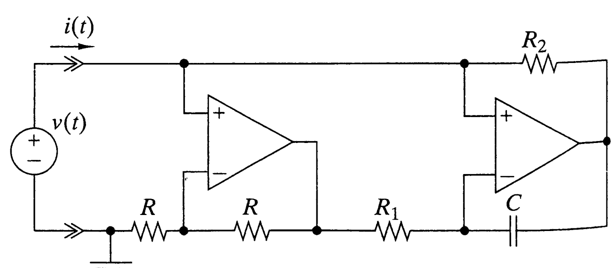


FIGURE P6–49

6–50 A D E RC OP AMP CIRCUIT DESIGN

An upgrade to one of your company's robotics products requires a proportional plus integral compensator that implements the input–output relationship

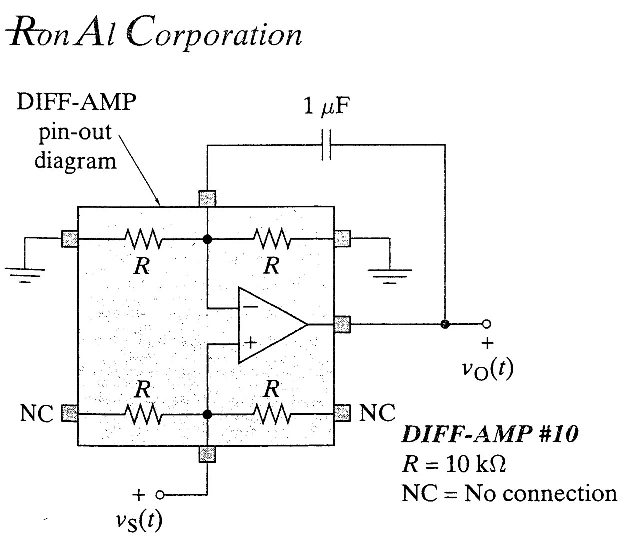
$$v_O(t) = v_S(t) + 50 \int_0^t v_S(x)\, dx$$

The input voltage $v_S(t)$ comes from an OP AMP, and the output voltage $v_O(t)$ drives a 10-kΩ resistive load. As the junior engineer in the company, you have been given the responsibility of developing a preliminary design.

(a) D Design a circuit that implements the relationship using the standard OP AMP building blocks in Figure 6–17. Minimize the parts count in your design.

(b) A The RonAl Corporation (founded by two well-known authors) has given you an unsolicited proposal claiming that their standard DIFF AMP-10 product can realize the required relationship. Their proposal is shown in Figure P6-50. Verify their claim.

(c) E Compare your design in part (a) with the RonAl proposal in part (b) in terms of the total part costs. Part costs in your company are as follows: resistors, \$400 per 10,000, capacitors, \$1,500 per 10,000; and OP AMPs, \$2500 per 10,000. RonAl's proposal offers to provide the company's standard DIFF AMP product for \$5000 per 10,000. Note that for the RonAl product you must supply the capacitor shown in Figure P6–50.



Note: External connections shown in color

FIGURE P6–50

6–51 A SUPER CAPACITOR

Super capacitors have very large capacitance (typically from 0.1 to 50 F) , very long charge holding times, and small sizes making them useful in nonbattery backup power applications. The circuit in Figure P6–51 is a standard method of measuring the capacitance of such a device. Initially the switch is held in Position A until the unknown capacitance is charged to a specified voltage $v_C = V_0$. At $t = 0$ the switch is moved to Position B and thereafter the load resistor R_L is continuously adjusted to maintain a constant discharge current $i_D = I_0 > 0$. The capacitor voltage is monitored until at time $t = T_1$ it decreases to a prescribed level $v_C = V_1$. For $V_0 = 5.5$ V, $V_1 = 3$ V, $I_0 = 1$ mA, and $T_1 = 3000$ s,

(a) Find the time derivative of the capacitor voltage for $0 < t < T_1$.

(b) Use the result in (a) to find the capacitance.

(c) Using the result in (b) calculate the amount of energy dissipated in R_L between $t = 0$ and $t = 3000$ s. *Caution*: R_L is not constant.

(d) Suppose the 1 mA constant current discharge continues after $t = 3000$ s. At $t = 4200$ s the capacitor voltage decreases to $v_C = 2$ V. Are these results consistent with the capacitance found in part (b)?

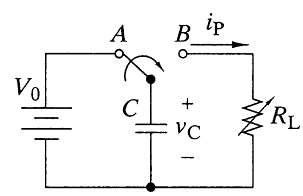


FIGURE P6–51

6–52 D DIFFERENTIATOR DESIGN

The input to the OP AMP differentiator in Figure 6–17 is a sinusoid with a peak-to-peak amplitude of 10 V. Select the values of R and C so that the OP AMP operates in its linear mode for all input frequencies less than 1 kHz. Assume the OP AMP saturates at ±15 V.

(a) $v_{2N}(t) = K_1 e^{-10t} \cos 10t + K_2 e^{-10t} \sin 10t$
(b) $C_1 = 20\ \mu F$

SUMMARY

- Circuits containing linear resistors and the equivalent of one capacitor or one inductor are described by first-order differential equations in which the unknown is the circuit state variable.
- The zero-input response in a first-order circuit is an exponential whose time constant depends on circuit parameters. The amplitude of the exponential is equal to the initial value of the state variable.
- For linear circuits the total response is the sum of the forced and natural responses. The natural response is the general solution of the homogeneous differential equation obtained by setting the input to zero. The forced response is a particular solution of the differential equation for the given input.
- For linear circuits the total response is the sum of the zero-input and zero-state responses. The zero-input response is caused by the initial energy stored in capacitors or inductors. The zero-state response results from the input driving forces.
- The initial and final values of the step response of a first- and second-order circuit can be found by replacing capacitors by open circuits and inductors by short circuits and then using resistance circuit analysis methods.
- For a sinusoidal input the forced response is called the sinusoidal steady-state response, or the ac response. The ac response is a sinusoid with the same frequency as the input but with a different amplitude and phase angle. The ac response can be found from the circuit differential equation using the method of undetermined coefficients.
- Circuits containing linear resistors and the equivalent of two energy storage elements are described by second-order differential equations in which the dependent variable is one of the state variables. The initial conditions are the values of the two state variables at $t = 0$.
- The zero-input response of a second-order circuit takes different forms depending on the roots of the characteristic equation. Unequal real roots produce the overdamped response, equal real roots produce the critically damped response, and complex conjugate roots produce underdamped responses.
- The circuit damping ratio ζ and undamped natural frequency ω_0 determine the form of the zero-input and natural responses of any second-order circuit. The response is overdamped if $\zeta > 1$, critically damped if $\zeta = 1$, and underdamped if $\zeta < 1$. Active circuits can produce undamped ($\zeta = 0$) and unstable ($\zeta < 0$) responses.
- Computer-aided circuit analysis programs can generate numerical solutions for circuit transient responses. Some knowledge of analytical methods and an estimate of the general form of the expected response are necessary to use these analysis tools.

PROBLEMS

ERO 7–1 FIRST-ORDER CIRCUIT ANALYSIS (SECTS. 7–1, 7–2, 7–3, 7–4)

Given a first-order *RC* or *RL* circuit,

(a) Find the circuit differential equation, the circuit characteristic equation, the circuit time constant, and the initial conditions (if not given).
(b) Find the zero-input response.
(c) Find the complete response for step function and sinusoidal inputs.

See Examples 7–1, 7–2, 7–3, 7–4, 7–5, 7–7, 7–8, 7–9, 7–12, 7–13 and Exercises 7–1, 7–2, 7–5, 7–6

7–1 Find the function that satisfies the following differential equation and the initial condition.

$$\frac{dv(t)}{dt} + 1500\,v(t) = 0, \quad v(0) = -15 \quad \text{V}$$

7–2 Find the function that satisfies the following differential equation and initial condition.

$$10^{-4}\frac{di(t)}{dt} + 10^{-1}i(t) = 0, \quad i(0) = -20 \quad \text{mA}$$

7–3 Find the time constants of the circuits in Figure P7–3.

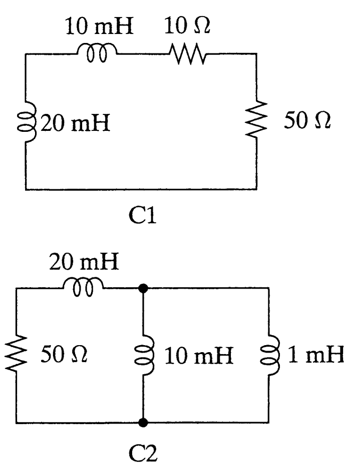


FIGURE P7–3

7–4 Find the time constants of the circuits in Figure P7–4.

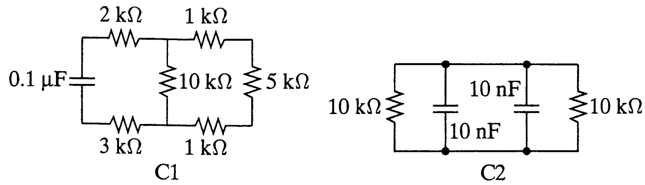


FIGURE P7–4

7–5 The switch in Figure P7–5 is closed at $t = 0$. The initial voltage on the capacitor is $v_C(0) = 15$ V. Find $v_C(t)$ and $i_O(t)$ for $t \geq 0$.

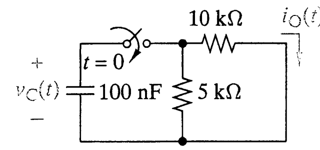


FIGURE P7–5

7–6 In Figure P7–6 the initial current through the inductor is $i_L(0) = 25$ mA. Find $i_L(t)$ and $v_O(t)$ for $t \geq 0$.

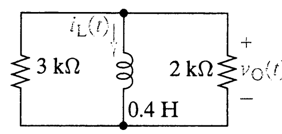


FIGURE P7–6

7–7 The switch in each circuit in Figure P7–7 has been in position A for a long time and is moved to position B at $t = 0$. For each circuit, develop an expression for the state variable for $t \geq 0$.

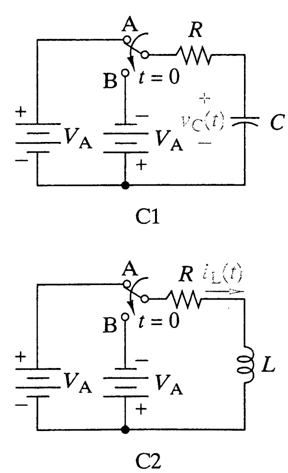


FIGURE P7–7

7–8 Repeat Problem 7–7 when the switch in each circuit has been in position B for a long time and is moved to position A at $t = 0$.

7–9 The circuit in Figure P7–9 is in the zero state when the input $i_S(t) = I_A u(t)$ is applied. Find the voltage $v_O(t)$ for $t \geq 0$. Identify the forced and natural components.

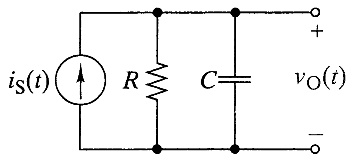


FIGURE P7–9

7–10 The circuit in Figure P7–10 is in the zero state when the input $v_S(t) = V_A u(t)$ is applied. Find $v_O(t)$ for $t \geq 0$. Identify the forced and natural components.

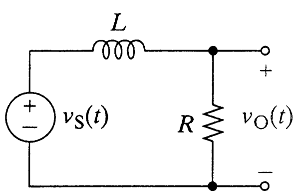


FIGURE P7–10

7–11 The switch in Figure P7–11 has been in position A for a long time and is moved to position B at $t = 0$. Find $v_C(t)$ for $t \geq 0$. Identify the forced and natural components.

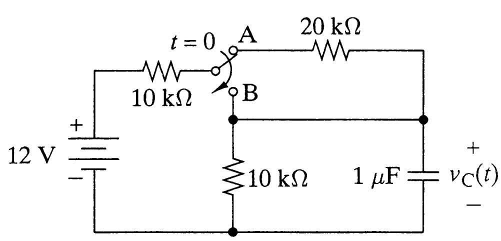


FIGURE P7–11

7–12 Repeat Problem 7–11 when the switch has been in position B for a long time and is moved to position A at $t = 0$.

7–13 The input in Figure P7–13 is $v_S(t) = 15$ V. The switch has been open for a long time and is closed at $t = 0$. Find $v_C(t)$ for $t \geq 0$. Identify the forced and natural components, and sketch their waveforms.

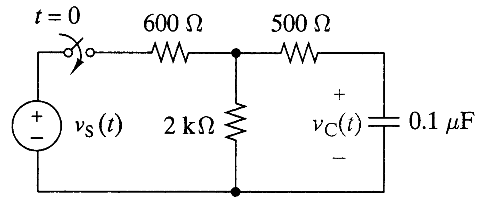


FIGURE P7–13

7–14 The input in Figure P7–13 is $v_S(t) = 15$ V. The switch has been open for a long time and is closed at $t = 0$. The switch is reopened at $t = 200$ μs. Find $v_C(t)$ for $t \geq 0$ and sketch its waveform.

7–15 Find the function that satisfies the following differential equation and the initial condition for an input $v_S(t) = 25\cos(100t)$ V.

$$\frac{dv(t)}{dt} + 200\,v(t) = v_S(t) \quad v(0) = 0 \quad \text{V}$$

7–16 Repeat Problem 7–15 for $v_S(t) = 25\sin(100t)$ V.

7–17 The input in Figure P7–17 is $v_S(t) = 20\cos 5t$ V. The switch has been open for a long time and is closed at $t = 0$. Find $i_L(t)$ for $t \geq 0$.

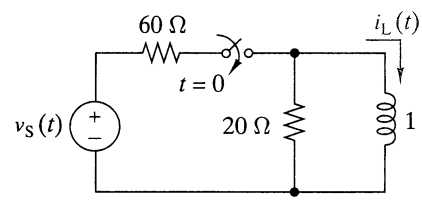


FIGURE P7–17

7–18 The switch in Figure P7–18 has been in position A for a long time and is moved to position B at $t = 0$. Find $i_L(t)$ for $t \geq 0$ and sketch its waveform.

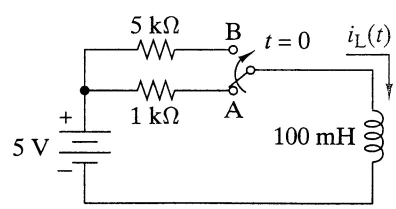


FIGURE P7–18

7–19 The switch in Figure P7–19 has been in position A for a long time and is moved to position B at $t = 0$. Find $v_C(t)$ for $t \geq 0$ and sketch its waveform.

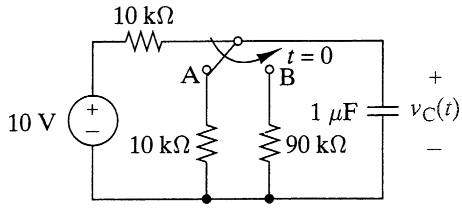


FIGURE P7–19

7–20 Switches 1 and 2 in Figure P7–20 have both been in position A for a long time. Switch 1 is moved to position B at $t = 0$ and Switch 2 is moved to position B at $t = 20$ ms. Find the voltage across the 0.1-μF capacitor for $t > 0$ and sketch its waveform.

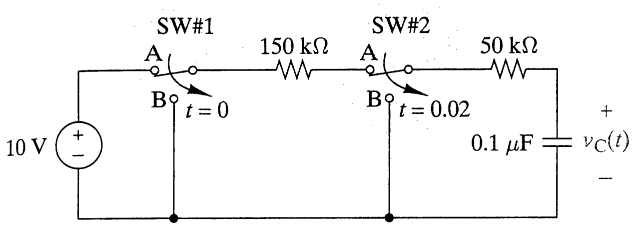


FIGURE P7–20

7–21 The switch in Figure P7–21 has been open for a long time and is closed at $t = 0$. The switch is reopened at $t = 2$ ms. Find $v_C(t)$ for $t \geq 2$ ms.

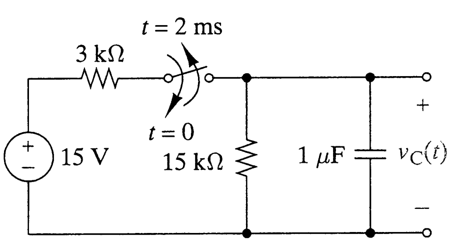


FIGURE P7–21

7–22 The input in Figure P7–22 is a rectangular pulse of the form

$$v_S(t) = V_A[u(t) - u(t - T)]$$

where $V_A = 5$ V and T is the pulse duration. A digital device with $RC = 20$ ns can detect a pulse input only if $v_C(t)$ exceeds 4 V. Find the minimum detectable pulse duration. Assume that $v_C(0) = 0$.

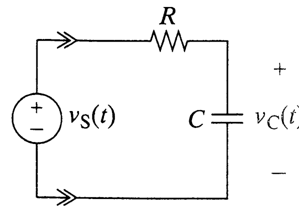


FIGURE P7–22

ERO 7–2 First-Order Circuit Responses (Sects. 7–1, 7–2, 7–3)

Given responses in a first-order *RC* or *RL* circuit,

(a) Find the circuit parameters or other responses.
(b) Select element values to produce a given response.

See Examples 7–6, 7–10 and Exercises 7–2, 7–3, 7–4, 7–12

7–23 For $t \geq 0$, the zero-input responses of the circuit in Figure P7–23 are

$$v_C(t) = 10e^{-1000t} \text{ V and } i_C(t) = -20e^{-1000t} \text{ mA}$$

(a) Find the circuit time constant.
(b) Find the initial value of the state variable.
(c) Find *R* and *C*.
(d) Find the energy stored in the capacitor at $t = 1$ ms.

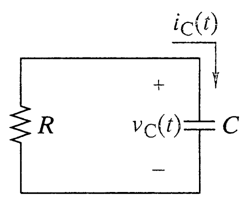


FIGURE P7–23

7–24 For $t \geq 0$ the zero-input responses of the circuit in Figure P7–24 are

$$i_L(t) = 5e^{-5000t} \text{ mA and } v_L(t) = -10e^{-5000t} \text{ V} \quad t \geq 0$$

(a) Find the circuit time constant.
(b) Find the initial value of the state variable.
(c) Find *R* and *L*.
(d) Find the energy stored in the inductor at $t = 0$.

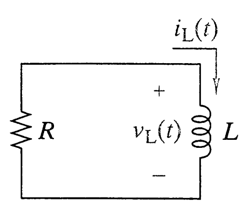


FIGURE P7–24

7–25 For $t \geq 0$ the voltage across and current though the capacitor in Figure P7–25 are

$$v_C(t) = 15 - 10e^{-2000t}\text{ V and } i_C(t) = 10e^{-2000t}\text{ mA}$$

(a) Find the circuit time constant.
(b) Find the initial value of the state variable.
(c) Find v_S, R, and C.
(d) Find the energy stored in the capacitor at $t = 1$ ms.

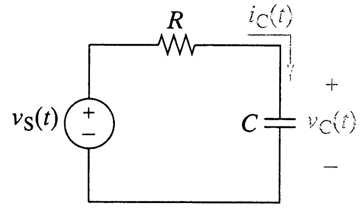


FIGURE P7–25

7–26 For $t \geq 0$ the voltage across the 100-nF capacitor in Figure P7–25 is

$$v_C(t) = 10 - 10e^{-500t} + [15e^{-500(t-0.005)} - 15]u(t - 0.005)\text{ V}$$

(a) Find the circuit time constant.
(b) Find the initial and final value of the state variable.
(c) Find v_S and R.

7–27 For $t \geq 0$ the current through and voltage across the inductor in Figure P7–27 is

$$i_L(t) = 5 - 10e^{-1000t}\text{ mA} \quad\text{and}\quad v_L(t) = e^{-1000t}\text{ V}$$

(a) Find the circuit time constant.
(b) Find the initial and final value of the state variable.
(c) Find v_S, R, and L.
(d) Find the energy stored in the inductor at $t = 0$ and $t = \infty$.

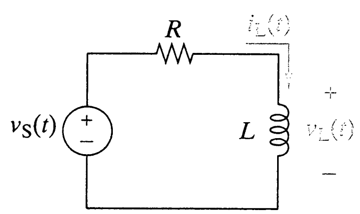


FIGURE P7–27

7–28 For $t \geq 0$ the zero-input voltage across the inductor in Figure P7–27 is

$$v_L(t) = -10e^{-500t}\text{ V}$$

(a) Find the circuit time constant.
(b) The initial value of the state variable is $i_L(0) = 10$ mA. Find R and L.

7–29 Select values for v_S, R, and C in Figure P7–25 to produce the following zero-state response:

$$v_C(t) = 10 - 10e^{-100t}\text{ V} \quad t \geq 0$$

7–30 The RC circuit in Figure P7–25 is in the zero state and $v_S(t) = 5u(t)$. Select values of R and C such that $v_C(t) = 2.5$ V at $t = 5$ ms.

ERO 7–3 SECOND-ORDER CIRCUIT ANALYSIS (SECTS. 7–5, 7–6, 7–7, 7–8)

Given a second-order circuit,

(a) Find the circuit differential equation, the circuit characteristic equation, and the initial conditions (if not given).
(b) Find the zero-input response.
(c) Find the complete response for a step function input.

See Examples 7–14, 7–15, 7–17, 7–18, 7–19, 7–20 and Exercises 7–14, 7–17

7–31 Find the response $v(t)$ that satisfies the following differential equation and meets the initial conditions.

$$\frac{d^2v}{dt^2} + 16\frac{dv}{dt} + 64v = 0,\ v(0) = 0\text{ V},\ \frac{dv}{dt}(0) = 12\text{ V/s}$$

7–32 Find the function that satisfies the following differential equation and the initial conditions.

$$\frac{d^2v}{dt^2} + 20\frac{dv}{dt} + 500v = 0,\ v(0) = 5\text{ V},\ \frac{dv}{dt}(0) = 30\text{ V/s}$$

7–33 Find the roots of the characteristic equation for each circuit in Figure P7–33. Specify whether the circuits are overdamped, underdamped, or critically damped.

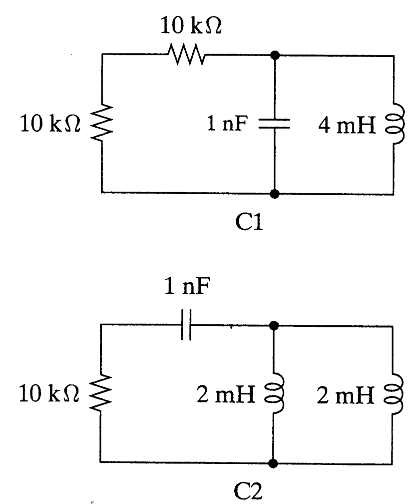


FIGURE P7–33

7–34 The switch in Figure P7–34 has been open for a long time and is closed at $t = 0$. The circuit parameters are

$L = 1$ H, $C = 0.5$ μF, $R_1 = 2$ kΩ, $R_2 = 3$ kΩ, and $V_A = 10$ V. Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Is the circuit overdamped or underdamped?

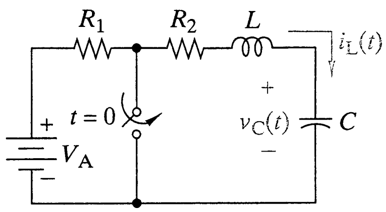


FIGURE P7–34

7–35 The switch in Figure P7–34 has been open for a long time and is closed at $t = 0$. The circuit parameters are $L = 1$ H, $C = 0.2$ μF, $R_1 = 3$ kΩ, $R_2 = 2$ kΩ, and $V_A = 10$ V. Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Is the circuit overdamped or underdamped?

7–36 The switch in Figure P7–36 has been open for a long time and is closed at $t = 0$. The circuit parameters are $L = 0.5$ H, $C = 25$ nF, $R_1 = 5$ kΩ, $R_2 = 12$ kΩ, and $V_A = 10$ V.

(a) Find the initial values of v_C and i_L at $t = 0$ and the final values of v_C and i_L as $t \to \infty$.

(b) Find the differential equation for $v_C(t)$ and the circuit characteristic equation.

(c) Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Is the circuit overdamped or underdamped?

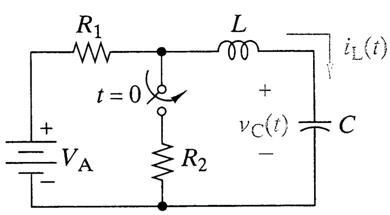


FIGURE P7–36

7–37 The switch in Figure P7–36 has been closed for a long time and is opened at $t = 0$. The circuit parameters are $L = 0.5$ H, $C = 0.4$ μF, $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, and $V_A = 15$ V.

(a) Find the initial values of v_C and i_L at $t = 0$ and the final values of v_C and i_L as $t \to \infty$.

(b) Find the differential equation for $v_C(t)$ and the circuit characteristic equation.

(c) Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Identify the forced and natural components of the responses and plot $v_C(t)$ and $i_L(t)$. Is the circuit overdamped or underdamped?

7–38 The switch in Figure P7–38 has been open for a long time and is closed at $t = 0$. The circuit parameters are $L = 0.4$ H, $C = 0.25$ μF, $R_1 = 3$ kΩ, $R_2 = 2$ kΩ, and $V_A = 15$ V. Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Is the circuit overdamped or underdamped?

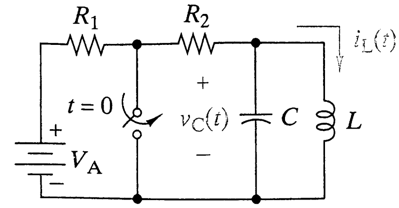


FIGURE P7–38

7–39 Repeat Problem 7–38 with $L = 80$ mH.

7–40 The switch in Figure P7–40 has been open for a long time and is closed at $t = 0$. The circuit parameters are $L = 0.8$ H, $C = 50$ nF, $R_1 = 4$ kΩ, $R_2 = 4$ kΩ, and $V_A = 20$ V. Find $v_C(t)$ and $i_L(t)$ for $t \geq 0$. Is the circuit overdamped or underdamped?

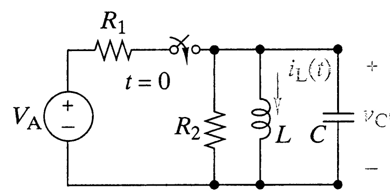


FIGURE P7–40

7–41 Repeat Problem 7–40 with $L = 1.25$ H.

7–42 The switch in Figure P7–42 has been in position A for a long time. At $t = 0$ it is moved to position B. The circuit parameters are $R_1 = 1$ kΩ, $R_2 = 4$ kΩ, $L = 0.625$ H, $C = 6.25$ nF, and $V_A = 15$ V. Find $v_C(t)$ and $i_L(t)$ for $t > 0$. Identify the forced and natural components of the responses and plot $v_C(t)$ and $i_L(t)$. Is the circuit overdamped or underdamped?

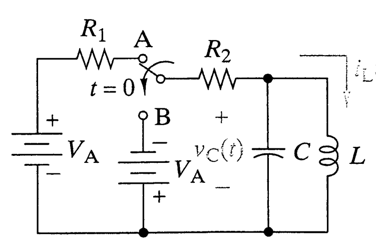


FIGURE P7–42

7–43 The switch in Figure P7–42 has been in position B for a long time. At $t = 0$ it is moved to position A. The circuit parameters are $R_1 = 10\ \Omega$, $R_2 = 40\ \Omega$, $L = 1$ H, $C = 100\ \mu$F, and $V_A = 12$ V. Find $v_C(t)$ and $i_L(t)$ for $t > 0$. Is the circuit overdamped or underdamped?

7–44 The switch in Figure P7–44 has been in position A for a long time and is moved to position B at $t = 0$. The circuit parameters are $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $L = 250$ mH, $C = 3.2\ \mu$F, and $V_A = 5$ V. Find $v_C(t)$ and $i_L(t)$ for $t > 0$. Is the circuit overdamped or underdamped?

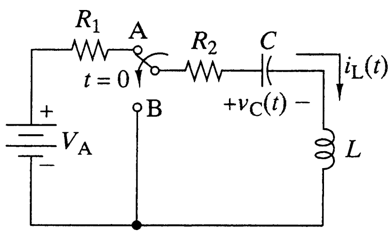


FIGURE P7–44

7–45 The switch in Figure P7–44 has been in position B for a long time and is moved to position A at $t = 0$. The circuit parameters are $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $L = 250$ mH, $C = 1\ \mu$F, and $V_A = 5$ V. Find $v_C(t)$ and $i_L(t)$ for $t > 0$. Is the circuit overdamped or underdamped?

7–46 The circuit in Figure P7–46 is in the zero state when the step function input is applied. The element values are $L = 2.5$ H, $C = 2\ \mu$F, $R = 3$ kΩ, and $V_A = 100$ V. Find the output $v_O(t)$.

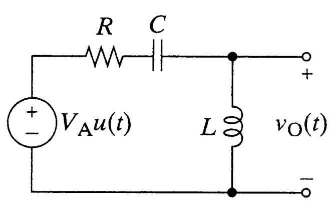


FIGURE P7–46

7–47 The circuit in Figure P7–47 is in the zero state when the step function input is applied. The element values are $R = 4$ kΩ, $L = 160$ mH, $C = 25$ nF, and $V_A = 100$ V. Find the output $v_O(t)$.

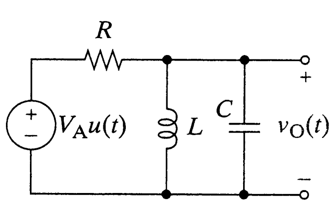


FIGURE P7–47

7–48 The circuit in Figure P7–48 is in the zero state when the step function input is applied. The element values are $R = 4$ kΩ, $L = 400$ mH, $C = 12.5$ nF, and $V_A = 100$ V. Find the output $v_O(t)$.

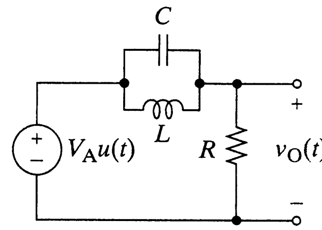


FIGURE P7–48

7–49 Find the differential equation relating v_O and v_S in Figure P7–49. Find the damping ratio and undamped natural frequency of the circuit.

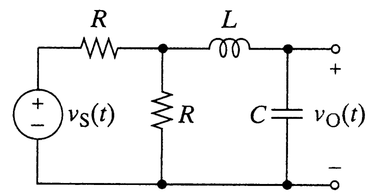


FIGURE P7–49

7–50 Find the differential equation relating v_O and v_S in Figure P7–50. Find the damping ratio and undamped natural frequency of the circuit.

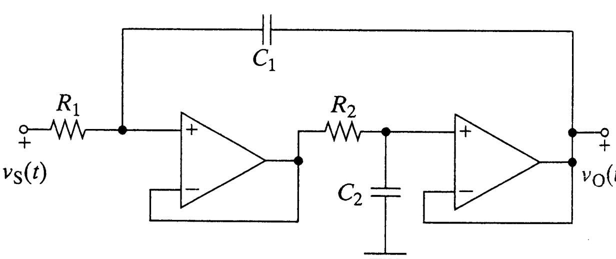


FIGURE P7–50

ERO 7–4 SECOND-ORDER CIRCUIT RESPONSES (SECTS. 7–5, 7–6, 7–7, 7–8)

Given the response of a second-order *RLC* circuit,

(a) Find the circuit parameters or other responses.

(b) Select element values to produce a given response.

See Example 7–16 and Exercises 7–13, 7–15, 7–16, 7–18

7–51 In a series *RLC* circuit the zero-state step response across the 1-μF capacitor is

$$v_C(t) = 10 - 50e^{-4000t} + 40e^{-5000t}\ \text{V} \qquad t \geq 0$$

(a) Find v_T, R, L.
(b) Find $i_L(t)$ for $t \geq 0$.

7–52 In a series RLC circuit the zero-input response in the 100-mH inductor is

$$i_L(t) = 5e^{-2000t}(\sin 1000t - \cos 1000t) \text{ mA} \quad t \geq 0.$$

(a) Find R, C.
(b) Find $v_C(t)$ for $t \geq 0$.

7–53 In a parallel RLC circuit the step responses are

$$v_C(t) = e^{-100t}(5 \cos 500t + 25 \sin 500t) \text{ V} \quad t \geq 0$$

$$i_L(t) = 20 - 25e^{-100t} \cos 500t \text{ mA} \quad t \geq 0$$

Find R, L, and C.

7–54 The zero-input responses of an RLC circuit are

$$v_C(t) = 2e^{-2000t} \cos 1000t - 4e^{-2000t} \sin 1000t \text{ V} \quad t \geq 0$$

$$i_L(t) = -80e^{-2000t} \cos 1000t + 60e^{-2000t} \sin 1000t \text{ mA} \quad t \geq 0$$

(a) Is this a series or a parallel RLC circuit?
(b) Find R, L, and C.

7–55 In a parallel RLC circuit with $v_C(0) = -10$ V the inductor current is observed to be

$$i_L(t) = 10e^{-10t} \cos(20\,t) \text{ mA} \quad t \geq 0$$

Find $v_C(t)$.

7–56 A series RLC circuit has $L = 400$ mH. What value of R and C will produce a zero-input response of the form

$$v_L(t) = K_1 e^{-5000t} + K_2 e^{-10000t} \text{ V} \quad t \geq 0$$

7–57 Select values for R, L, and C in a series circuit so that $\zeta = 0.5$ and $\omega_0 = 4$ Mrad/s.

7–58 Select values for R, L, and C in a series circuit so that its step response has the form

$$v_C(t) = V_A - 2V_Ae^{-200t} + V_Ae^{-800t} \text{ V} \quad t > 0$$

where V_A is the amplitude of the input.

7–59 Select values for R, L, and C in a parallel RLC circuit so that its zero-input response has the form

$$i_L(t) = K_1 e^{-500t} + K_2 t\, e^{-500t} \text{ V} \quad t > 0$$

7–60 What range of damping ratios is available in the circuit in Figure P7–60?

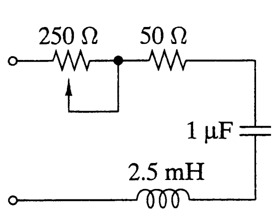


FIGURE P7–60

INTEGRATING PROBLEMS

7–61 D RC CIRCUIT DESIGN

Design an RC circuit whose step response fits neatly in the unshaded region in Figure P7–61. The source you must use is a 1.5-V battery. Your design must include a method of generating the required step function and can use resistors in the range from 1 kΩ to 100 kΩ. Test your design by finding its step response and calculating its value at $t = 1$ ms, 2 ms, and 10 ms.

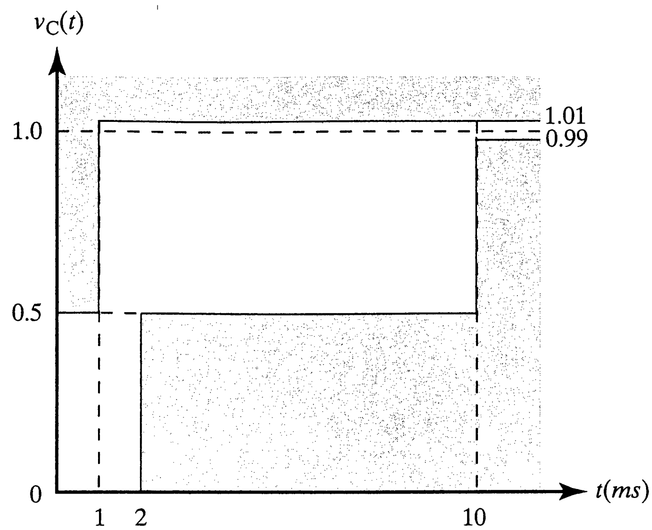


FIGURE P7–61

7–62 D LIGHTNING PULSER DESIGN

The circuit in Figure P7–62 is a simplified diagram of a pulser that delivers simulated lightning transients to the test article at the output interface. The pulser performance specification states that when the switch closes the short-circuit current delivered by the pulser must be of the form $i_{SC}(t) = I_Ae^{-\alpha t} \cos \beta t$, with $\alpha = 200$ krad/s, $\beta = 10$ Mrad/s, and $I_A = 2$ kA. Select the values of L, C, and the initial charge on the capacitor.

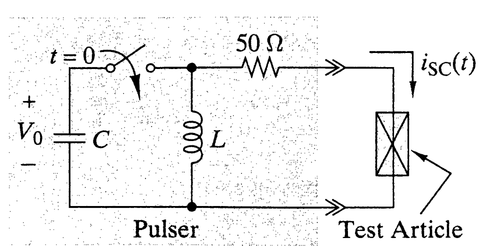


FIGURE P7–62

7–63 EXPERIMENTAL SECOND-ORDER RESPONSE

Figure P7–63 shows an oscilloscope display of the voltage across the resistor in a series *RLC* circuit.

(a) Estimate the values of α and β of the damped sine signal.

(b) Use the values of α and β from (a) to write the characteristic equation of the circuit.

(c) The resistor is known to be 2.2 kΩ. Use the characteristic equation from (b) to determine the values of L and C.

(d) If the display shows the zero-input response of the circuit, what are the values of the initial conditions $v_C(0)$ and $i_L(0)$?

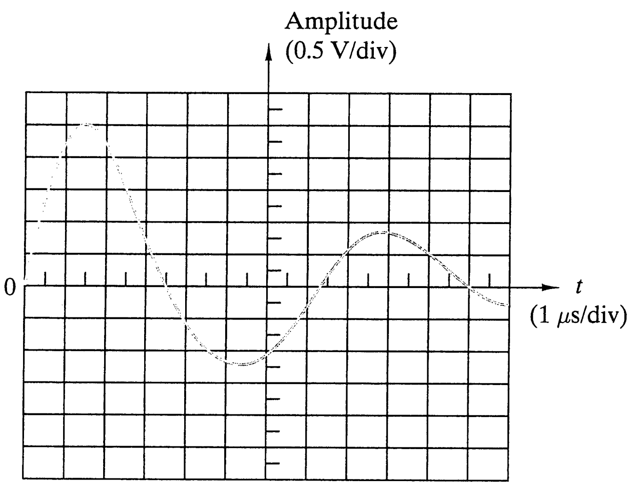


FIGURE P7–63

7–64 SAMPLE HOLD CIRCUIT

Figure P7–64 shows a sample-hold circuit at the input of an analog-to-digital converter. In the sample mode the converter commands the analog switch to close (ON) and the capacitor charges up to the value of the input signal. In the hold mode the converter commands the analog switch to open (OFF), and the capacitor holds and feeds the input signal value to the converter via the OP AMP voltage follower. When conversion is completed, the analog switch is turned ON again and the sample-hold cycle repeats.

(a) The series resistances of the analog switch are $R_{ON} = 50\ \Omega$ and $R_{OFF} = 100\ \text{M}\Omega$. When $C = 20$ pF, what is the time constant in the sample mode and the time constant in the hold mode?

(b) The number of sample-hold cycles per second must be at least twice the highest frequency in the analog input signal. What is the minimum number of sample-hold cycles per second for an input $v_S(t) = 5 + 5\sin 2\pi 1000t$?

(c) Sampling at 10 times the minimum number of sample-hold cycles per second, what is the duration of the sample mode if the hold mode lasts nine times as long as the sample mode?

(d) For the input in (b), will the capacitor voltage reach a steady-state condition during the sample mode?

(e) What fraction of the capacitor voltage will be lost during the hold mode?

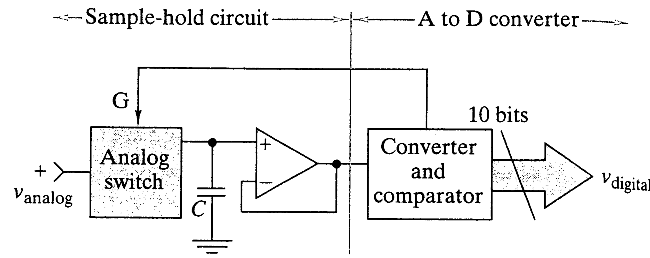


FIGURE P7–64

7–65 SUPER CAPACITOR SPECIFICATION

Super capacitors have very large capacitance (0.1 to 50 F), very long charge holding times (several days), and are several thousand times smaller than conventional capacitors with the same energy storage capacity. These attributes make them useful in nonbattery backup power applications such as VCRs, cash registers, computer terminals, and programmable consumer products. Because of their unique capabilities special parameters are used to characterize these devices. One of the standard parameters is the so-called 30-minute current. The circuit in Figure P7–65 is the industry standard method of measuring this parameter. With the capacitor completely discharged (shorted for at least 24 hours), the switch is closed and the capacitor current measured by observing the voltage across the resistor. As the name suggests, the 30-minute current is the charging current observed 30 minutes after the switch is closed.

The following data are specification values for a certain super capacitor.

$C = 1.4$ F +80%, −20%
Max rated voltage = 11 V
Max current at 30 minutes = 1.5 mA
Test circuit conditions $V_{test} = 10$ V (dc) and $R_{test} = 200\ \Omega$

Are these values internally consistent?

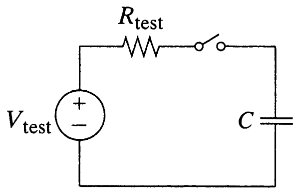


FIGURE P7–65

7–66 SECOND-ORDER OP AMP CIRCUIT

The circuit in Figure P7–66 is a second-order circuit consisting of a cascade connection of a first-order *RC* circuit and a first-order *RL* circuit.

(a) Find the second-order differential equation relating the output voltage $v_2(t)$ to the input $v_S(t)$.

(b) Show that the roots of the characteristic equation are $-1/R_1C_1$ and $-R_2/L$. That is, show that the natural frequencies of the second-order circuit are the natural frequencies of the two first-order circuits.

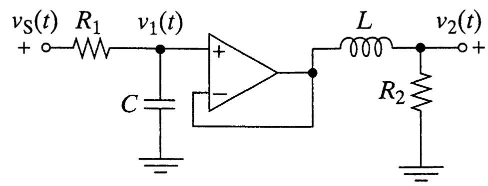


FIGURE P7–66

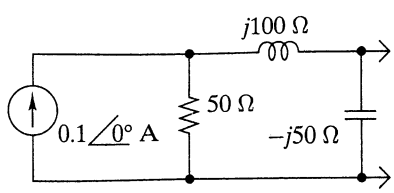


FIGURE 8–58

Exercise 8–20

Calculate the maximum average power available at the interface in Figure 8–58.

Answer: 125 mW.

SUMMARY

- A phasor is a complex number representing a sinusoidal waveform. The magnitude and angle of the phasor correspond to the amplitude and phase angle of the sinusoid. The phasor does not provide frequency information.
- The additive property states that adding phasors is equivalent to adding sinusoids of the same frequency. The derivative property states that multiplying a phasor by $j\omega$ is equivalent to differentiating the corresponding sinusoid.
- In the sinusoidal steady state, phasor currents and voltages obey Kirchhoff's laws and the element i–v relationships are written in terms of impedances. Impedance can be defined as the ratio of phasor voltage over phasor current. The device and connection constraints for phasor circuit analysis have the same form as resistance circuits.
- Phasor circuit analysis techniques include series equivalence, parallel equivalence, circuit reduction, Thévenin's and Norton's theorems, unit output method, superposition, node-voltage analysis, and mesh-current analysis.
- In the sinusoidal steady state the equivalent impedance at a pair of terminals is $Z(j\omega) = R(\omega) + jX(\omega)$, where $R(\omega)$ is called resistance and $X(\omega)$ is called reactance. A frequency at which an equivalent impedance is purely real is called a resonant frequency. Admittance is the reciprocal of impedance.
- In the sinusoidal steady state the instantaneous power to a passive element is a periodic function at twice the frequency of the driving force. The average power delivered to an inductor or capacitor is zero. The average power delivered to a resistor is ½ $R|\mathbf{I}_R|^2$. The maximum average power is delivered by a fixed source to an adjustable load when the source and load impedances are conjugates.

PROBLEMS

ERO 8–1 SINUSOIDS AND PHASORS (SECT. 8–1)

Use the additive and derivative properties of phasors to convert sinusoidal waveforms into phasors and vice versa.
See Examples 8–1, 8–2, 8–3, 8–4 and Exercises 8–1, 8–2, 8–3, 8–4

8–1 Transform the following sinusoids into phasor form and draw a phasor diagram. Use the additive property of phasors to find $v_1(t) + v_2(t)$.

(a) $v_1(t) = 250\cos(\omega t + 45°)$

(b) $v_2(t) = 150\cos\omega t + 100\sin\omega t$

8–2 Transform the following sinusoids into phasor form and draw a phasor diagram. Use the additive property of phasors to find $i_1(t) + i_2(t)$.

(a) $i_1(t) = 6\cos\omega t$

(b) $i_2(t) = 3\cos(\omega t - 90°)$

8–3 Convert the following phasors into sinusoidal waveforms.

(a) $\mathbf{V}_1 = 10\, e^{-j30°}$, $\omega = 10^4$

(b) $\mathbf{V}_2 = 60\, e^{-j220°}$, $\omega = 10^4$

(c) $\mathbf{I}_1 = 5\, e^{j90°}$, $\omega = 200$

(d) $\mathbf{I}_2 = 2\, e^{j270°}$, $\omega = 200$

8–4 Use the phasors in Problem 8–3 and the additive property to find $2v_1(t) + v_2(t)$ and $i_1(t) + 3i_2(t)$.

8–5 Use the phasor derivative property to find the time derivative of the waveform $v(t)$ when

$$\mathbf{V} = 20 + j5 \text{ V and } \omega = 20 \text{ rad/s.}$$

8–6 Convert the following phasors into sinusoids:

(a) $\mathbf{V}_1 = 10 + j40$, $\omega = 10$

(b) $\mathbf{V}_2 = (8 - j3)5\, e^{-j60°}$, $\omega = 20$

(c) $\mathbf{I}_1 = 8 - j3 + \dfrac{3}{j}$, $\omega = 300$

(d) $\mathbf{I}_2 = \dfrac{3 + j1}{1 - j3}$, $\omega = 50$

8–7 The input–output relationship of a signal processor is

$$v_2(t) = \frac{1}{200}\frac{dv_1(t)}{dt} + v_1(t)$$

Use phasors to find the output $v_2(t)$ when the input is $v_1(t) = 10 \cos(500t + 45°)$.

8–8 Given the sinusoids

$$v_1(t) = 50 \cos(\omega t - 45°) \quad \text{and} \quad v_2(t) = 25 \sin \omega t$$

use the additive property of phasors to find $v_3(t)$ such that $v_1 + v_2 + v_3 = 0$.

8–9 Find the phasor corresponding to $v(t) = 12\sqrt{2} \cos [1000\pi(t - 2.5 \times 10^{-4})]$.

8–10 Given a phasor $\mathbf{V}_1 = -3 + j4$, use phasor methods to find a voltage $v_2(t)$ that leads $v_1(t)$ by 90° and has an amplitude of 10 V.

ERO 8–2 EQUIVALENT IMPEDANCE (SECTS. 8–2, 8–3)

Given a linear circuit, use series and parallel equivalence to find the equivalent impedance at a specified pair of terminals.

See Examples 8–5, 8–6, 8–9, 8–10, 8–12 and Exercises 8–8, 8–10, 8–11

8–11 Express the equivalent impedance of the following circuits in rectangular and polar form:

(a) A 25-Ω resistor in series with a 20-mH inductor at ω = 1000 rad/s.

(b) A 25-Ω resistor in parallel with a 20-μF capacitor at ω = 1000 rad/s.

(c) The circuit formed by connecting the circuits in (a) and (b) in parallel.

(d) Repeat (c) at ω = 4000 rad/s.

8–12 Find the equivalent impedance Z in Figure P8–12. Express the result in both polar and rectangular form.

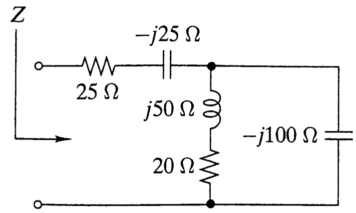


FIGURE P8–12

8–13 Express the equivalent impedance of the following circuits in rectangular and polar form:

(a) A 100-mH inductor in series with a 10-μF capacitor at ω = 2000 rad/s.

(b) A 30-mH inductor in parallel with 60-Ω resistor at ω = 2000 rad/s.

(c) The circuit formed by connecting the circuits in (a) and (b) in series.

(d) Repeat (c) at ω = 1000 rad/s.

8–14 Find the equivalent impedance Z in Figure P8–14. Express the result in both polar and rectangular form.

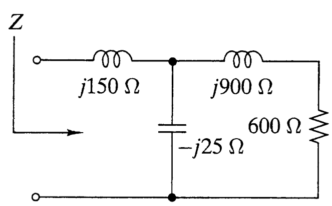


FIGURE P8–14

8–15 The voltage applied at the input to a linear circuit is $v(t) = 200 \cos(1000t - 60°)$ V. In the sinusoidal steady state the input current is observed to be $i(t) = 20 \cos 1000t$ mA.

(a) Find the equivalent impedance at the input.

(b) Find the steady-state current $i(t)$ for $v(t) = 150 \cos(1000t - 270°)$ V.

8–16 The circuit in Figure P8–16 is operating in the sinusoidal steady state with ω = 20 krad/s. Find the equivalent impedance Z.

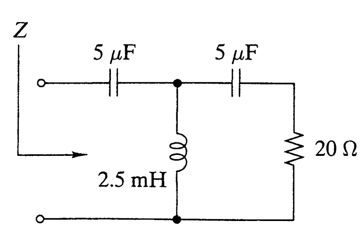


FIGURE P8–16

8–17 **D** An inductor L is connected in parallel with a 600-Ω resistor. The parallel combination is then connected in series with a capacitor C. Select the values of L and C so that the equivalent impedance of the combination is $100 + j0\ \Omega$ at $\omega = 100$ krad/s.

8–18 A 200-Ω resistor is connected in series with a capacitor. When the current through the series combination is $i(t) = 20\cos(1000t)$ mA, the voltage is $v(t) = 2\sqrt{2}\cos(1000\,t - 45°)$. Find the value of C.

8–19 **D** A capacitor C is connected in parallel with a resistor R. Select values of R and C so that the equivalent impedance of the combination is $600 - j600\ \Omega$ at $\omega = 1$ Mrad/s.

8–20 A relay coil can be modeled as a resistor and inductor in series. When a certain coil is connected across a 110-V, 60-Hz source, the amplitude of the relay current is observed to be 0.25 A. When the frequency of the 110-V source is increased to 400 Hz, the amplitude drops to 0.12 A. Find the resistance and inductance of the coil.

ERO 8–3 BASIC PHASOR CIRCUIT ANALYSIS (SECTS. 8–3, 8–4)

Given a linear circuit operating in the sinusoidal steady state, find phasor responses using basic analysis methods such as series and parallel equivalence, voltage and current division, circuit reduction, Thévenin or Norton equivalent circuits, and proportionality or superposition.
See Examples 8–6, 8–8, 8–9, 8–10, 8–13, 8–14, 8–15, 8–17, 8–18, 8–19 and Exercises 8–9, 8–13, 8–14, 8–15

8–21 A voltage $v(t) = 10\cos 500t$ V is applied across a series connection of a 100-Ω resistor and 40-mH inductor. Find the steady-state current $i(t)$ through the series connection.

8–22 The circuit in Figure P8–22 is operating in the sinusoidal steady state with $v_S(t) = V_A \cos \omega t$ V. Use circuit reduction to derive a general expression for the phasor response $\mathbf{I}_L$.

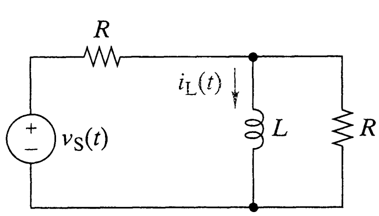


FIGURE P8–22

8–23 A current source delivering $i(t) = 300\cos 2000t$ mA is connected across a parallel combination of a 10-kΩ resistor and a 50-nF capacitor. Find the steady-state current $i_R(t)$ through the resistor and the steady-state current $i_C(t)$ through the capacitor. Draw a phasor diagram showing $\mathbf{I}$, $\mathbf{I}_C$, and $\mathbf{I}_R$.

8–24 The circuit in Figure P8–24 is operating in the sinusoidal steady state with $i_S(t) = I_A \cos \omega t$ A. Use phasor circuit reduction to derive a general expression for the steady-state response $\mathbf{V}_R$.

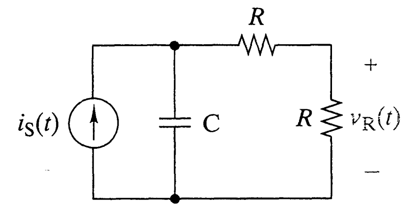


FIGURE P8–24

8–25 A voltage $v(t) = 50\cos(1000t + 45°)$ V is applied across a parallel connection of a 5-kΩ resistor and a 200-nF capacitor. Find the steady-state current $i_C(t)$ through the capacitor and the steady-state current $i_R(t)$ through the resistor. Draw a phasor diagram showing $\mathbf{V}$, $\mathbf{I}_C$, and $\mathbf{I}_R$.

8–26 The circuit in Figure P8–26 is operating in the sinusoidal steady state. Use circuit reduction to find the input impedance seen by the voltage source and the steady-state response $v_x(t)$.

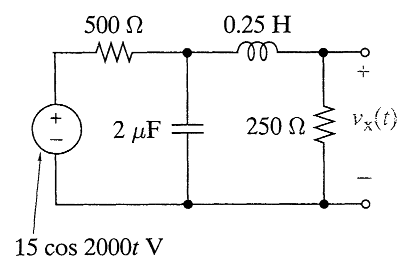


FIGURE P8–26

8–27 The circuit in Figure P8–27 is operating in the sinusoidal steady state. Use circuit reduction to find the input impedance seen by the current source and steady-state response $v_x(t)$.

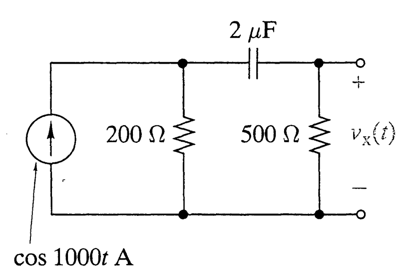


FIGURE P8–27

8–28 The circuit in Figure P8–28 is operating in the sinusoidal steady state. Use circuit reduction to find the input impedance seen by the voltage source and the steady-state phasor response $\mathbf{V}_x$.

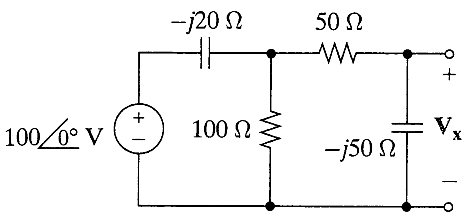


FIGURE P8–28

8–29 The circuit in Figure P8–29 is operating in the sinusoidal steady state. Use superposition to find the phasor response $\mathbf{I}_x$.

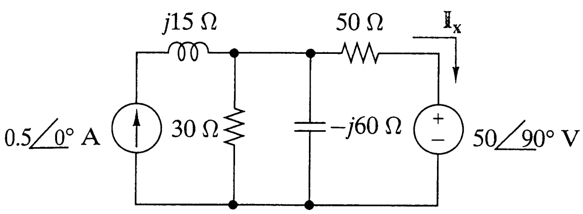


FIGURE P8–29

8–30 The circuit in Figure P8–30 is operating in the sinusoidal steady state. Use superposition to find the response $v_x(t)$. *Note:* The sources do not have the same frequency.

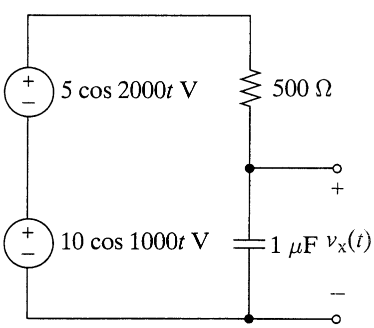


FIGURE P8–30

8–31 The circuit in Figure P8–31 is operating in the sinusoidal steady state. Use superposition to find the response $v_x(t)$. *Note:* The sources do not have the same frequency.

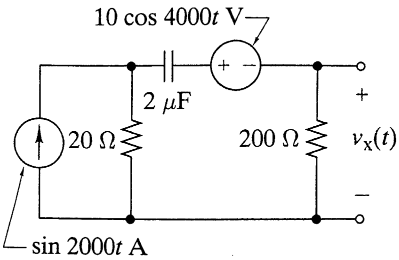


FIGURE P8–31

8–32 The circuit in Figure P8–32 is operating in the sinusoidal steady state. Find the input impedance seen by the voltage source and the phasor response $\mathbf{V}_x$.

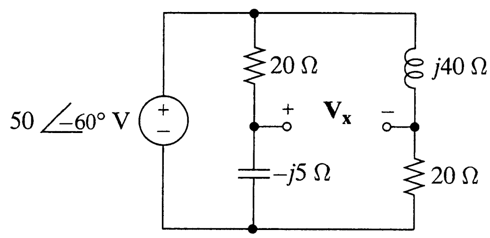


FIGURE P8–32

8–33 The circuit in Figure P8–33 is operating in the sinusoidal steady state. Use the unit output method to find the input impedance seen by the voltage source and the phasor response $\mathbf{V}_x$.

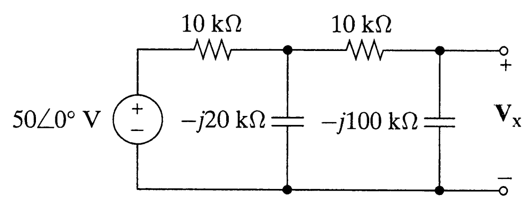


FIGURE P8–33

8–34 Find the phasor Thévenin equivalent of the source circuit to the left of the interface in Figure P8–34. Then use the equivalent circuit to find the steady-state voltage $v(t)$ and current $i(t)$ delivered to the load.

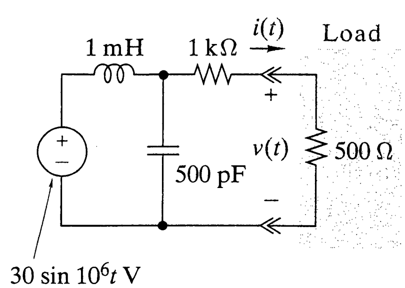


FIGURE P8–34

8–35 Find the phasor Thévenin equivalent of the source circuit to the left of the interface in Figure P8–35. Then use the equivalent circuit to find the phasor voltage **V** and current **I** delivered to the load.

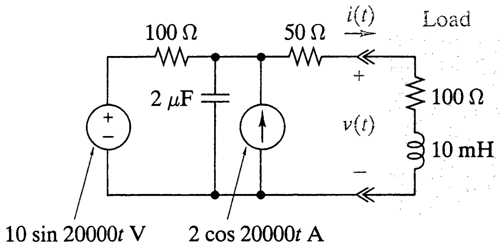


FIGURE P8–35

8–36 The circuit in Figure P8–36 is operating in the sinusoidal steady state. When $Z_L = 0$, the phasor current at the interface is $\mathbf{I} = 4.8 - j3.6$ mA. When $Z_L = -j20$ kΩ, the phasor interface current is $\mathbf{I} = 10 + j0$ mA. Find the Thévenin equivalent of the source circuit.

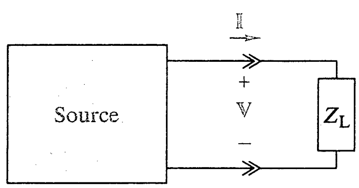


FIGURE P8–36

8–37 The circuit in Figure P8–36 is operating in the sinusoidal steady state with ω = 2 krad/s. When $Z_L = 0$, the phasor short-circuit current is $\mathbf{I} = \mathbf{I}_{SC} = 0.8 - j0.4$ A. When a 1-nF capacitor is connected across the interface, the current delivered is $\mathbf{I} = \mathbf{I}_{LOAD} = 3 + j0$ A. Note that the amplitude of the load current is greater than the amplitude of the short-circuit current. Find the Thévenin equivalent of the source circuit and then explain why $|\mathbf{I}_{LOAD}| > |\mathbf{I}_{SC}|$.

8–38 Use a Thévenin equivalent circuit to find the phasor response $\mathbf{V}_x$ in Figure P8–33.

8–39 Design a two-port circuit so that an input voltage $v_S(t) = 100\cos(10^4 t)$ V delivers a steady-state output current of $i_O(t) = 10\cos(10^4 t - 35°)$ mA to a 50-Ω resistive load.

8–40 Design a two-port circuit so that an input voltage $v_S(t) = 50\sin(1000t)$ V delivers a steady-state output voltage of $v_O(t) = 50\cos(1000t - 45°)$ V.

ERO 8–4 GENERAL CIRCUIT ANALYSIS (SECT. 8–5)

Given a linear circuit operating in the sinusoidal steady state, find equivalent impedances and phasor responses using node-voltage or mesh-current analysis.
See Examples 8–20, 8–21, 8–22, 8–23, 8–24, 8–25, 8–26 and Exercises 8–16, 8–17, 8–18

8–41 Use node-voltage analysis to find the sinusoidal steady-state response $v_x(t)$ in the circuit shown in Figure P8–41.

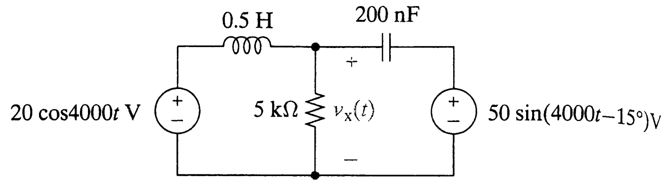


FIGURE P8–41

8–42 Use node-voltage analysis to find the steady-state phasor response $\mathbf{V}_O$ in the circuit shown in Figure P8–42.

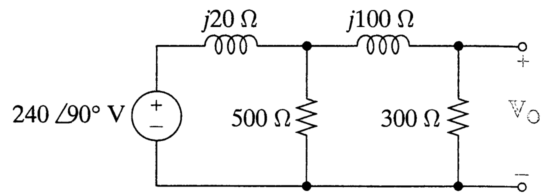


FIGURE P8–42

8–43 Use node-voltage analysis to find the input impedance Z_{IN} and phasor gain $K = \mathbf{V}_O/\mathbf{V}_S$ of the circuit shown in Figure P8–43 with μ = 100.

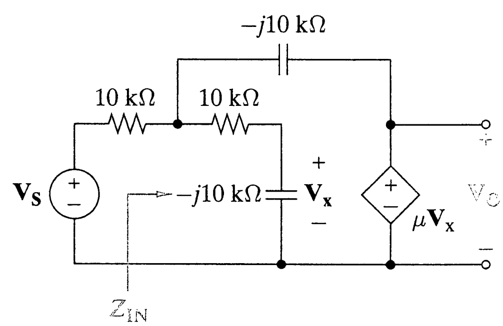


FIGURE P8–43

8–44 Use mesh-current analysis to find the phasor branch currents $\mathbf{I}_1$, $\mathbf{I}_2$, and $\mathbf{I}_3$ in the circuit shown in Figure P8–44.

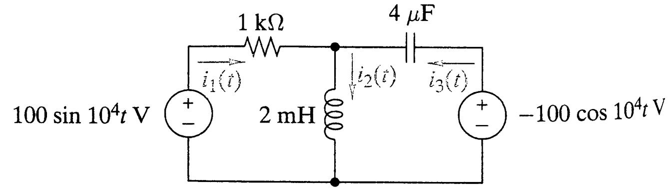


FIGURE P8–44

8–45 Use mesh-current analysis to find the phasor response $\mathbf{V}_y$ and $\mathbf{I}_x$ in the circuit shown in Figure P8–45.

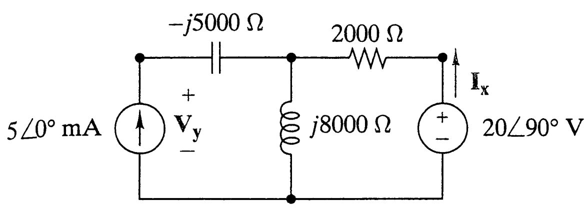


FIGURE P8–45

8–46 Use mesh-current analysis to find the input impedance Z_{IN} and phasor gain $K = \mathbf{V}_O/\mathbf{V}_S$ of the circuit shown in Figure P8–46.

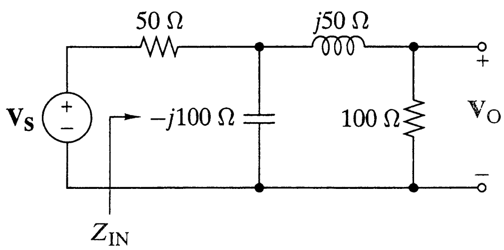


FIGURE P8–46

8–47 Find the input impedance Z_{IN} and phasor gain $K = \mathbf{V}_O/\mathbf{V}_S$ of the circuit shown in Figure P8–47.

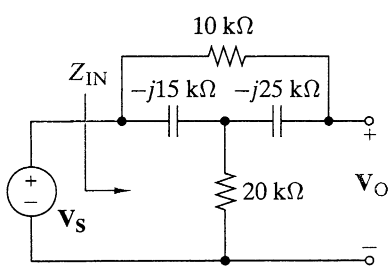


FIGURE P8–47

8–48 Find the sinusoidal steady-state response $v_O(t)$ in the circuit shown in Figure P8–48. The element values are $\mathbf{V}_S = 80$ mV, $R_1 = 10$ kΩ, $R_P = 5$ kΩ, $R_F = 1$ MΩ, $R_C = 10$ kΩ, $R_L = 100$ kΩ, $C = 0.25$ nF, and $\beta = 50$. The frequency is $\omega = 500$ rad/s.

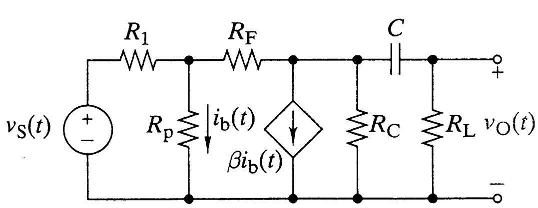


FIGURE P8–48

8–49 Find the phasor response $\mathbf{I}_{IN}$ and $\mathbf{V}_O$ in the circuit shown in Figure P8–49.

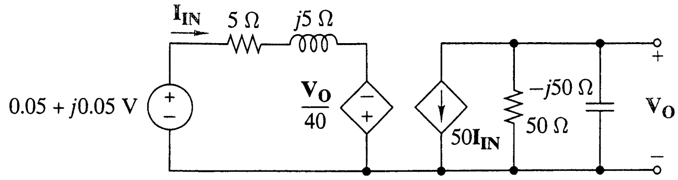


FIGURE P8–49

8–50 The OP AMP circuit in Figure P8–50 is operating in the sinusoidal steady state with $\omega = 100$ krad/s. Find the input phasor $\mathbf{V}_S$ when the output phasor is $\mathbf{V}_O = 10 + j0$ V.

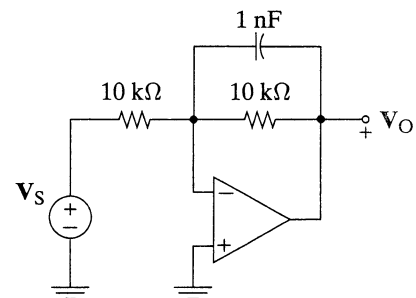


FIGURE P8–50

ERO 8–5 AVERAGE POWER AND MAXIMUM POWER TRANSFER (SECT. 8–6)

Given a linear circuit operating in the sinusoidal steady state,

(a) Find the average power delivered at a specified interface.
(b) Find the maximum average power available at a specified interface.
(c) Find the load impedance required to draw the maximum available power.

See Examples 8–27, 8–28 and Exercises 8–19, 8–20

8–51 A load consisting of a 50-Ω resistor in series with a 100-mH inductor is connected across a voltage source $v_S(t) = 35 \cos 500t$ V. Find the phasor voltage, current, and average power delivered to the load.

8–52 A load consisting of a 50-Ω resistor in series with a 8-μF capacitor is connected across a voltage source $v_S(t) = 50 \cos 2500t$ V. Find the phasor voltage, current, and average power delivered to the load.

8–53 A load consisting of a resistor and capacitor connected in parallel draws an average power of 100 mW and a peak current of 35 mA when connected to voltage source $v_S(t) = 15 \cos 2500t$ V. Find the values of R and C.

8–54 A load consists of an 800-Ω resistor in parallel with an inductor whose reactance is 400 Ω. Find the average power delivered when the load is connected to a current source whose peak amplitude is 0.2 A.

8–55 **(a)** Find the average power delivered to the load in Figure P8–55.
(b) Find the maximum available average power at the interface shown in Figure P8–55.
(c) Specify the load required to extract the maximum average power.

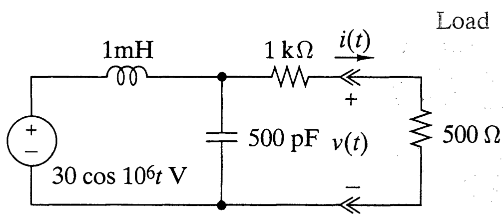


FIGURE P8–55

8–56 A 200-V (rms) source delivers 100 W to an inductive load whose series resistance is 8 Ω. What is the load impedance?

8–57 **(a)** Find the maximum average power available at the interface in Figure P8–57.
(b) Specify the values of R and C that will extract the maximum power from the source circuit.

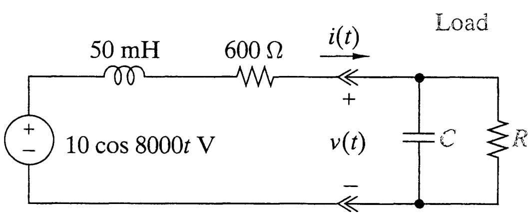


FIGURE P8–57

8–58 The steady-state open-circuit voltage at the output interface of a source circuit is $10\angle 0°$ V. When a 100-Ω resistor is connected across the interface, the steady-state output voltage is $4\angle -60°$ V. Find the maximum average power available at the interface and the load impedance required to extract the maximum power.

8–59 The phasor Thévenin voltage of a certain source is $\mathbf{V}_T = 10 + j0$ V, and the Thévenin impedance is $Z_T = 100 + j50$ Ω. The problem is to extract as much average power as possible from this source using a single standard value resistor as the load. The values of resistance available are 1.0, 1.5, 2.2, 3.3, 4.7, 6.8, and multiples of 10 times these values.
(a) Find the maximum available average power from the source.
(b) Find the standard load resistor that extracts the most average power.

8–60 The 220-V (rms) power delivery circuit can be modeled as shown in Figure P8–60. Find the average power delivered by the source and absorbed by the load.

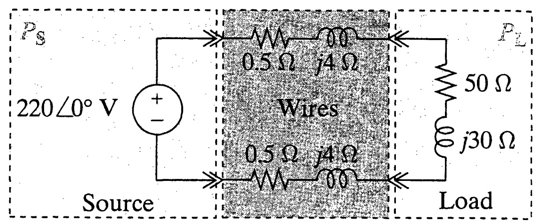


FIGURE P8–60

INTEGRATING PROBLEMS

8–61 AC VOLTAGE MEASUREMENT

An ac voltmeter measurement indicates the amplitude of a sinusoid and not its phase angle. The magnitude and phase can be inferred by making several measurements and using KVL. For example, Figure P8–61 shows a relay coil of unknown resistance and inductance. The following ac voltmeter readings are taken with the circuit operating in the sinusoidal steady state at $f = 1$ kHz: $|\mathbf{V}_S| = 10$ V, $|\mathbf{V}_1| = 4$ V, and $|\mathbf{V}_2| = 8$ V.
(a) Use these voltage magnitude measurements to solve for R and L.
(b) Determine the phasor voltage across each element and show that they satisfy KVL.

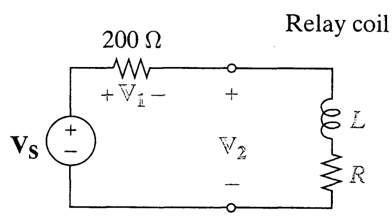


FIGURE P8–61

8–62 OP AMP CIRCUITS

The characteristics of resistive OP AMP circuits can be extended to dynamic circuits operating in the sinusoidal steady state using the concept of impedance. For the circuit in Figure P8–62,

(a) Find the phasor gain $K = \mathbf{V}_O/\mathbf{V}_S$ in terms of the impedances Z_1 and Z_2.

(b) Find the magnitude and angle of K when $Z_1 = 100$ kΩ and $Z_2 = 10 - j20$ kΩ.

(c) Select values for Z_1 and Z_2 so that $K = 2\angle{-60°}$.

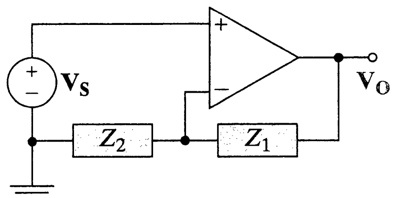


FIGURE P8-62

8–63 A CIRCUIT FORCED RESPONSE

The purpose of this problem is to demonstrate that the steady-state response obtained using phasor circuit analysis is the forced component of the solution of the circuit differential equation.

(a) Transform the circuit in Figure P8–63 into the phasor domain and use voltage division to solve for phasor output $\mathbf{V}$.

(b) Convert the phasor found in (a) into a sinusoid of the form $v(t) = a \cos \omega t + b \sin \omega t$.

(c) Formulate the circuit differential equation in the capacitor voltage $v(t)$.

(d) Show that the $v(t)$ found in part (b) satisfies the differential equation in (c).

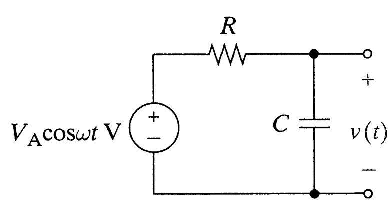


FIGURE P8–63

8–64 A AVERAGE STORED ENERGY

In the sinusoidal steady state the phasor voltage across a capacitor is $\mathbf{V}_C = V_A + j0$. Derive an expression for the average energy stored in the capacitor.

8–65 D AC CIRCUIT DESIGN

Select values for the reactances L and C in Figure P8–65 so that the input impedance seen by the voltage source is $75 + j0\ \Omega$ when the frequency is $\omega = 10^6$ rad/s. For these values of L and C, find the Thévenin impedance seen by the 600-Ω load resistor.

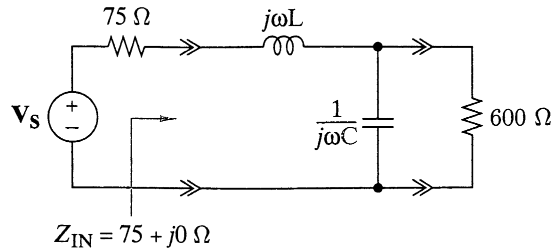


FIGURE P8–65

8–66 A AC CIRCUIT ANALYSIS

Ten years after graduating with a BSEE you decide to go to graduate schools for a masters degree. In desperate need of income, you agree to sign on as a grader in the basic circuit analysis course. One of the problems asks the students to find $v(t)$ in Figure P8–66 when the circuit operates in the sinusoidal steady state. One of the students offers the following solution:

$$\begin{aligned} v(t) &= (R + j\omega L) \times i(t) \\ &= (20 + j20) \times 0.5 \cos 200t \\ &= 10 \cos 200t + j10 \cos 200t \\ &= 10\sqrt{2} \cos (200t + 45°) \end{aligned}$$

Is the answer correct? If not, what grade would you give the student? If correct, what comments would you give the student about the method of solution?

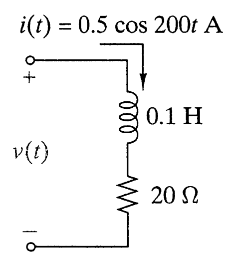


FIGURE P8–66

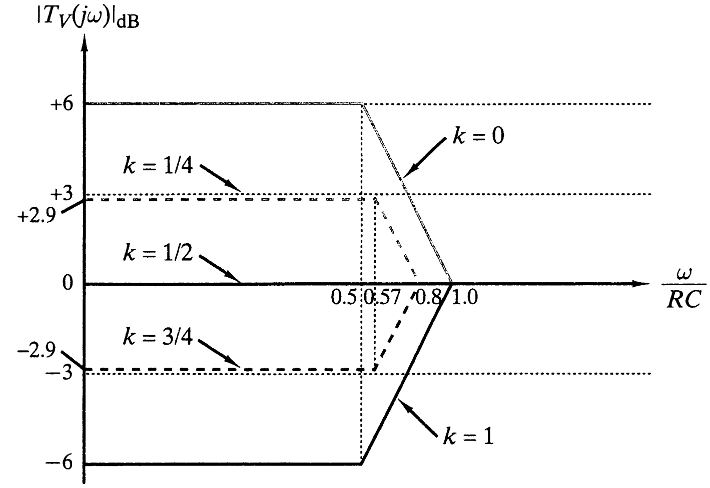


FIGURE 12–56 *Bass tone control Bode diagram.*

emphasis and de-emphasis gain responses (in dB) are mirror images across the 0 dB gain axis (see Figure 12–56).

Numerical values of R and C are determined by the frequency range to be affected by the circuit. For example, to affect frequencies below 300 Hz requires $RC = 1/(2\pi 300) = 5.3 \times 10^{-4}$. Selecting $R = 10$ kΩ requires $C = 53$ nF.

SUMMARY

- The frequency response of a circuit is defined by the variation of the gain $|T(j\omega)|$ and phase $\angle T(j\omega)$ with frequency. The gain function is usually expressed in dB in frequency-response plots. Logarithmic frequency scales are used on frequency-response plots of the gain and phase functions.
- A passband is a range of frequencies over which the steady-state output is essentially constant with very little attenuation. A stopband is a range of frequencies over which the steady-state output is significantly attenuated. The cutoff frequency is the boundary between a passband and the adjacent stopband.
- Circuit gain responses are classified as low pass, high pass, bandpass, and bandstop depending on the number and location of the stop and passbands. The performance of devices and circuits is often specified in terms of frequency-response descriptors such as bandwidth, passband gain, and cutoff frequency.
- The low- and high-frequency gain asymptotes of a first-order circuit intersect at a corner frequency determined by the location of its pole. The total phase change from low to high frequency is ±90°. First-order circuits can be connected to produce bandpass and bandstop responses.
- The low- and high-frequency gain asymptotes of second-order circuits intersect at a corner frequency determined by the natural frequency of the poles. The total phase change from low to high frequency is 180°.

Second-order circuits with complex critical frequencies may exhibit narrow resonant peaks and valleys.

- Series and parallel *RLC* circuits provide bandpass and bandstop gain characteristics that are easily related to the circuit parameters.
- Bode plots are graphs of the gain (in dB) and phase angle (in degrees) versus log-frequency scales. Straight-line approximations to the gain and phase can be constructed using the corner frequencies defined by the poles and zeros of $T(s)$. The purpose of the straight-line approximations is to develop a conceptual understanding of frequency response. The straight-line plots do not necessarily provide accurate data at all frequencies, especially for circuits with complex poles.
- Computer-aided circuit analysis programs can accurately generate and plot frequency-response data. The user must have a rough idea of the gain and frequency ranges of interest to use these tools intelligently.
- It is often necessary to relate the time-domain characteristics of a circuit to its frequency response, and vice versa. The transfer function provides a link between the frequency-domain and time-domain responses.

PROBLEMS

ERO 12–1 FIRST-ORDER CIRCUIT FREQUENCY RESPONSE (SECTS. 12–1, 12–2)

Given a first-order circuit or transfer function,

(a) Determine frequency response descriptors and classify the response.
(b) Draw the straight-line approximations of the gain and phase responses.
(c) Use the straight-line approximations to estimate the gain, phase, or steady-state output at specified frequencies.
(d) Select circuit parameters to produce specified descriptors.

See Examples 12–2, 12–3, 12–4, 12–5, 12–6, 12–7, 12–8 and Exercise 12–1

12–1 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–1.

(a) Find the dc gain and cutoff frequency. What kind of gain response is this?
(b) Draw the straight-line approximations of the gain and phase responses.
(c) Use the straight-line approximation to estimate the gain at $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

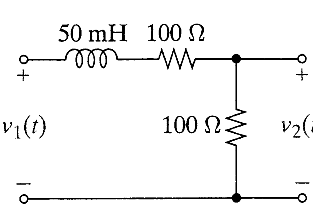


FIGURE P12–1

12–2 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–2.

(a) Find the dc gain, infinite frequency gain, and cutoff frequency. What kind of gain response is this?
(b) Use the straight-line approximation to estimate the gain at $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

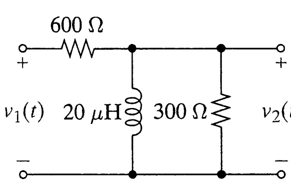


FIGURE P12–2

12–3 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–3.

(a) Find the dc gain and cutoff frequency. What kind of gain response is this?
(b) Draw the straight-line approximations of the gain and phase responses.
(c) Use the straight-line approximation to estimate the phase response at $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

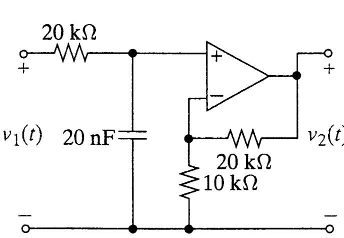


FIGURE P12–3

12–4 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–4.

(a) Find the dc gain and cutoff frequency. What kind of gain response is this?

(b) Draw the straight-line approximations of the gain and phase of $T_V(j\omega)$.

(c) Use the straight-line gain to estimate the amplitude of the steady-state output for a 5-V sinusoidal input with $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

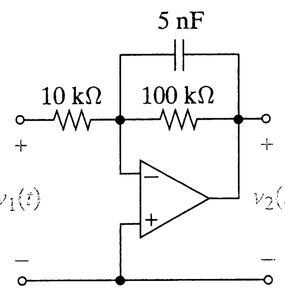


FIGURE P12–4

12–5 **(a)** Find the dc gain, infinite frequency gain, and cutoff frequency of the circuit in Figure P12–5.

(b) What type of gain response does this circuit have?

(c) Draw the straight-line approximations of the gain and phase responses.

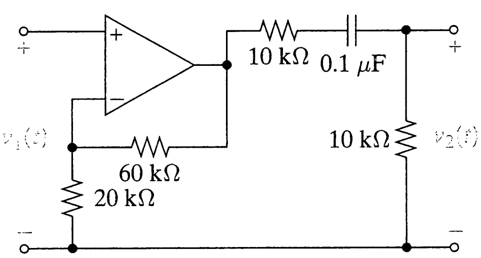


FIGURE P12–5

12–6 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–6. What type of gain response does the circuit have? What is the passband gain? Select values of R and C to produce a cutoff frequency of 500 Hz. What is the phase shift at the cutoff frequency?

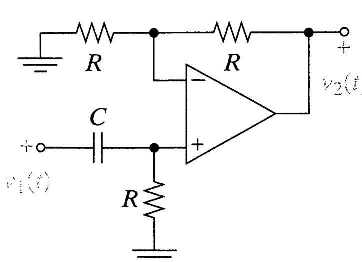


FIGURE P12–6

12–7 A first-order low-pass circuit has a passband gain of 20 dB and a cutoff frequency of 350 rad/s. Find the straight-line approximations of the gain(in dB) at ω = 200, 400, and 800 rad/s?

12–8 A first-order high-pass circuit has a passband gain of 5 dB and a cutoff frequency of 2 krad/s. Find the straight-line approximations to the phase response at $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

12–9 The transfer function of a first-order circuit is

$$T(s) = \frac{0.1}{10^{-2} + \dfrac{20}{s}}$$

(a) What type of gain response does this circuit have? What is the cutoff frequency and the passband gain?

(b) Draw the straight-line approximations of the gain and phase responses.

(c) Use the straight-line approximation to estimate the gain at $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

12–10 Repeat Problem 12–9 for

$$T(s) = \frac{10}{10^2 + \dfrac{s}{20}}$$

ERO 12–2 SECOND-ORDER CIRCUIT FREQUENCY RESPONSE (SECT. 12–3)

Given a second-order linear circuit or its transfer function,

(a) Determine frequency response descriptors and classify the circuit response.

(b) Draw the straight-line approximations of the gain and phase responses.

(c) Use the straight-line approximations to estimate the gain, phase, or steady-state output at specified frequencies.

(d) Select circuit parameters to produce specified descriptors.

See Examples 12–9, 12–10, 12–11 and Exercises 12–3, 12–4, 12–5, 12–6, 12–8

12–11 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–11.

(a) Find the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(b) Draw the straight-line approximation of the gain.

(c) Use the straight-line gain to estimate the gain $\omega = 0.5\omega_0$, ω_0, and $2\omega_0$.

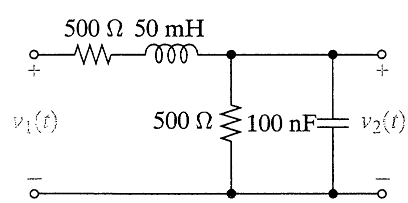


FIGURE P12–11

12–12 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–12.

(a) Determine the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(b) Draw the straight-line approximation of the gain.

(c) Use the straight-line gain to estimate the gain $\omega = 0.5\omega_0$, ω_0, and $2\omega_0$.

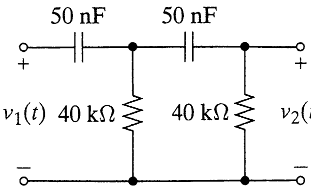


FIGURE P12–12

12–13 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–13.

(a) Determine the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(b) Draw the straight-line approximation of the gain.

(c) Compare the straight-line gain and the actual gain at $\omega = 0.5\omega_0$, ω_0, and $2\omega_0$.

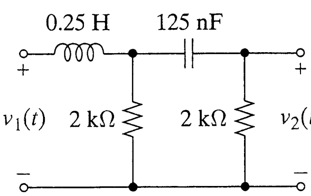


FIGURE P12–13

12–14 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–14.

(a) Determine the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(b) Use the straight-line approximation to estimate the gain at $\omega = 0.5\omega_0$, ω_0, and $2\omega_0$.

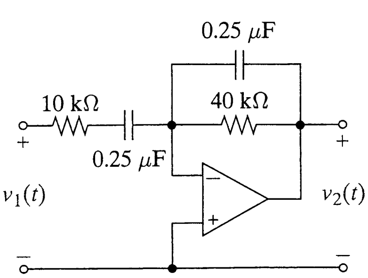


FIGURE P12–14

12–15 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–15.

(a) Determine the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(b) Draw the straight-line approximation of the gain.

(c) Compare the straight-line gain and the actual gain at $\omega = 0.5\omega_0$, ω_0, and $2\omega_0$.

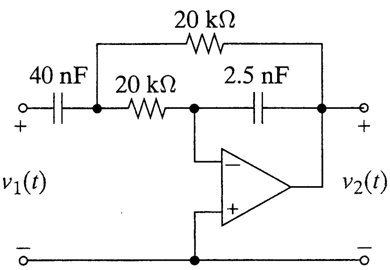


FIGURE P12–15

12–16 **(a)** Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–16 for $R_1 = 10$ kΩ, $R_2 = 40$ kΩ, and $C = 20$ nF.

(b) Determine the dc gain, infinite-frequency gain, the damping ratio ζ, and the undamped natural frequency ω_0. What type of gain response does this circuit have?

(c) Draw the straight-line approximation of the gain.

(d) Use the straight-line gain to estimate the amplitude of the steady-state output for a 0.5-V sinusoidal input with $\omega = 0.5\omega_C$, ω_C, and $2\omega_C$.

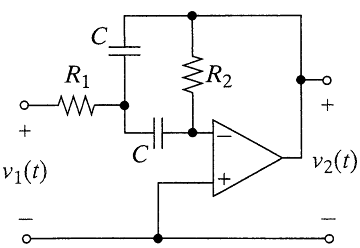


FIGURE P12–16

12–17 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–17. What type of gain response does this circuit have? Derive expressions for the damping ratio ζ and the undamped natural frequency ω_0 in terms of circuit parameters. Select values of the circuit parameters so that $\zeta = 2$ and $\omega_0 = 5$ krad/s. What is the passband gain for your choice?

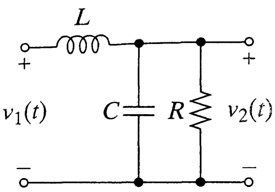


FIGURE P12–17

12–18 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–18. What type of gain response does this circuit have? Derive expressions for the damping ratio ζ and the undamped natural frequency ω_0 in terms of circuit parameters. Select values of the circuit parameters so that $\zeta = 0.7$ and $\omega_0 = 2500$ rad/s. What is the passband gain for your choice?

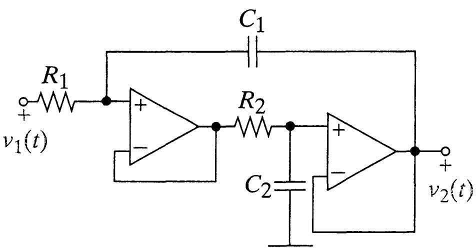


FIGURE P12–18

12–19 The circuit in Figure P12–19 produces a bandpass response. With $R_1 = R_2 = R_4 = 10$ kΩ, select the values of R_3, C_1, and C_2 to produce a passband gain of 5 with cutoff frequencies at 500 rad/s and 50 krad/s.

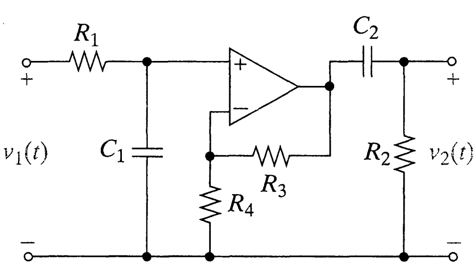


FIGURE P12–19

12–20 The transfer function of a bandpass circuit can be written as

$$T(s) = \frac{2.5 \times 10^4}{s + 5.5 \times 10^3 + \dfrac{2.5 \times 10^6}{s}}$$

(a) What are the cutoff frequencies and the passband gain?

(b) Draw the straight-line approximations of the gain and phase responses.

ERO 12–3 THE FREQUENCY RESPONSE OF RLC CIRCUITS (SECT. 12–4)

Given a series or parallel *RLC* circuit connected as a bandpass or bandstop filter,

(a) Find the circuit parameters or frequency response descriptors.
(b) Select the circuit parameters to achieve specified filter characteristics.
(c) Derive expressions for the frequency response descriptors.

See Examples 12–12, 12–13, 12–14 and Exercises 12–10, 12–11, 12–12

12–21 A series *RLC* circuit is designed to have a bandwidth of 8 Mrad/s and an input impedance of 50 Ω at its resonant frequency of 40 Mrad/s. Determine the values *L*, *C*, *Q*, and the upper and lower cutoff frequencies.

12–22 A parallel *RLC* circuit with $C = 20$ pF and $Q = 10$ has a resonant frequency of 100 Mrad/s. Find the values of *R*, *L*, ω_{C1}, and ω_{C2}.

12–23 A series *RLC* circuit with $R = 100$ Ω, $L = 20$ mH, and $C = 200$ pF is driven by a sinusoidal voltage source with a peak amplitude of 10 V.

(a) Calculate the circuit bandwidth and the upper and lower cutoff frequencies.

(b) Calculate the amplitude of the steady-state voltage across the capacitor and the inductor at the resonant frequency.

12–24 A series *RLC* circuit has a resonant frequency of 400 krad/s and an upper cutoff frequency of 420 krad/s. Find the bandwidth, *Q*, and the lower cutoff frequency.

12–25 A parallel *RLC* circuit with $R = 40$ kΩ is to have a resonant frequency of 100 MHz. Calculate the values of *L* and *C* required to produce a bandwidth of 100 kHz.

12–26 A series *RLC* bandpass filter is required to have a resonance at $f_0 = 200$ kHz. The series connected *L* and *C* are to be driven by a sinusoidal source with a Thévenin resistance of 50 Ω. The following standard capacitors are available in the stock room: 1 μF, 680 nF, 470 nF, 330 nF, 200 nF, and 120 nF. The inductor will be custom-designed to match the capacitor used. Select from available capacitors the one that minimizes the circuit bandwidth.

12–27 A series *RLC* circuit is to be used as a notch filter to eliminate a bothersome 60-Hz hum in an audio channel. The signal source has a Thévenin resistance of 600 Ω. Select values of *L* and *C* so the upper cutoff frequency is below 200 Hz.

12–28 Find the transfer function $T_V(s) = V_2(s)/V_1(s)$ for the bandpass circuit in Figure P12–28. Derive expressions for the parameters *B*, *Q*, ω_{C1}, and ω_{C2} in terms of the circuit parameters *R*, *L*, and *C*.

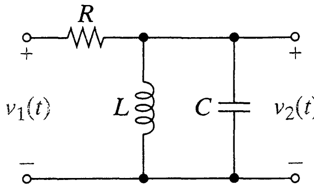


FIGURE P12–28

12–29 The transfer function $T_V(s) = V_2(s)/V_1(s)$ of the circuit in Figure P12–29 has a bandstop filter characteristic. Without solving for the transfer function, use the element impedances to

(a) Explain why the low- and high-frequency passband gains are unity.

(b) Explain why the bandstop notch occurs at $\omega_0 = 1/\sqrt{LC}$.

(c) Derive expressions ω_{C1} and ω_{C2} in terms of circuit parameters R, L, and C.

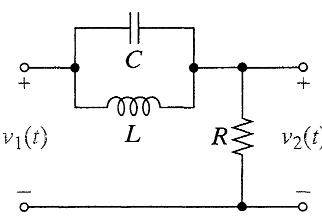


FIGURE P12–29

12–30 Find the transfer impedance $T_Z(s) = V_2(s)/I_1(s)$ for the bandpass circuit in Figure P12–30. Derive expressions for the parameters B, Q, ω_{C1}, and ω_{C2} in terms of the circuit parameters R, L, and C.

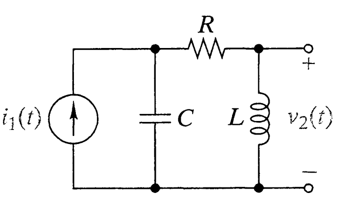


FIGURE P12–30

ERO 12–4 Bode Plots (Sects. 12–5, 12–6)

(a) Construct Bode plots of the straight-line approximations of gain and phase responses of a given circuit or transfer function.
(b) Construct the transfer function corresponding to a given straight-line gain plot.
(c) Use the straight-line gain plots to estimate frequency response descriptors or steady-state outputs.

See Examples 12–15, 12–16, 12–17, 12–18, 12–19, 12–20, 12–21 and Exercises 12–13, 12–14, 12–15, 12–16

12–31 Construct Bode plots of the straight-line approximations of gain response of the circuit in Figure P12–31. Use the straight-line gain plot to estimate the amplitude of the steady-state output for an input $v_1(t) = 10 \sin 500t$ V. Calculate the actual amplitude of the steady-state output for this input and compare the two results.

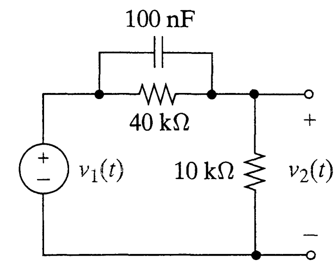


FIGURE P12–31

12–32 Repeat Problem 12–31 using the circuit in Figure P12–32.

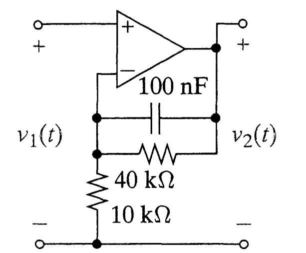


FIGURE P12–32

12–33 Construct Bode plots of the straight-line approximations of gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{(s + 25)}{(5s + 5)(s + 5)}$$

12–34 Construct Bode plots of the straight-line approximations to the gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{s(s + 5)}{(s + 1)(s + 25)}$$

12–35 Construct Bode plots of the straight-line approximations to the gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{25\, s(s + 100)}{(s + 10)(s + 25)}$$

12–36 Construct Bode plots of the straight-line approximations to the gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{2.5s^2}{(0.05\, s + 1)^2}$$

12–37 Construct Bode plots of the straight-line approximations to the gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{2000}{s^2 + 5\, s + 100}$$

12–38 Construct Bode plots of the straight-line approximations to the gain and phase responses of the following transfer function. Is this a low-pass, high-pass, bandpass, or bandstop function? Estimate the cutoff frequency and passband gain.

$$T(s) = \frac{100\, s^2}{s^2 + 5\, s + 25}$$

12–39 Find the transfer function corresponding to the straight-line gain plot in Figure P12–39. Compare the straight-line gain and the actual gain at the corner frequencies shown in the figure.

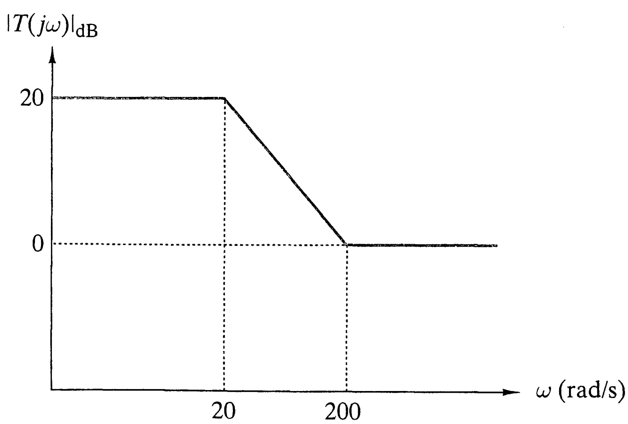


FIGURE P12–39

12–40 Find the transfer function corresponding to the straight-line gain plot in Figure P12–40. Compare the straight-line gain and the actual gain at the corner frequencies shown in the figure.

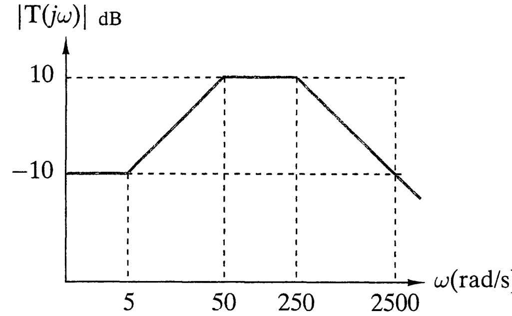


FIGURE P12–40

ERO 12–5 FREQUENCY RESPONSE AND STEP RESPONSE (SECT. 12–7)

(a) Find the step response corresponding to a given straight-line gain response.
(b) Find the straight-line approximations to the gain and phase responses corresponding to a given step response.
(c) Construct a transfer function that meets constraints on both the frequency and step responses.

See Examples 12–22, 12–23, 12–24 and Exercises 12–2, 12–7, 12–9

12–41 Find the step response corresponding to the straight-line gain response in Figure P12–41.

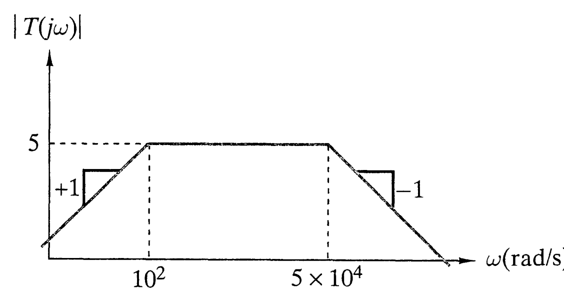


FIGURE P12–41

12–42 Repeat Problem 12–41 for the gain response in Figure P12–39.

12–43 Repeat Problem 12–41 for the gain response in Figure P12–40

12–44 The step response of a linear circuit is

$$g(t) = 12 - 10\, e^{-10t} - 2\, e^{-100t} \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–45 The step response of a linear circuit is

$$g(t) = 5 - 5\,e^{-100t}\sin 200\,t \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–46 The step response of a linear circuit is

$$g(t) = 10\,e^{-100t}\sin 200t \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct a Bode plot of the straight-line approximation to the gain response.

12–47 The step response of a linear circuit is

$$g(t) = e^{-100t} + 2\,e^{-2000t} \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–48 Construct a first-order low-pass transfer function with a dc gain of 10, a bandwidth less than 250 rad/s, and a step response that rises to 50% of its final value in less than 4 ms.

12–49 Construct a first-order high-pass transfer function whose step response decays to 5% of its peak value in less than 10 μs and whose cutoff frequency is less than 100 kHz.

12–50 Construct a second-order bandpass transfer function with a midband gain of 10, a center frequency of 100 kHz, a bandwidth less than 50 kHz, and a step response that decays to less that 20% of its peak value in less than 5 μs.

INTEGRATING PROBLEMS

12–51 DC, AC, AND IMPULSE RESPONSES

A linear circuit is driven by an input $v_1(t) = 2e^{-1000t}$. The zero-state response for this input is observed to be $v_2(t) = 5e^{-1000t}[1 - \cos(2000t)]$.

(a) Find the steady-state output when the input is $v_1(t) = 4\cos(2000t)$.

(b) Find the steady-state output when the input is 15 V dc.

(c) Construct the Bode plot of the circuit gain as a function of frequency.

(d) Find the circuit impulse response.

12–52 BANDPASS FILTER STEP RESPONSES

The step responses of the two second-order bandpass filters are

$$g_1(t) = 2e^{-60t}\sin(600t)u(t) \text{ and } g_2(t) = 10(e^{-30t} - e^{-12000t})u(t)$$

(a) Find the transfer function, center frequency, and bandwidth of each filter. Sketch the Bode plot of the gain response of each filter.

(b) A filter is required for an input signal

$$v_1(t) = 8\cos(100t) + 6\cos(600\,t) + 10\cos(3000\,t)$$

that will pass the desired sinusoid at $\omega = 600$ with about 20 dB gain, and keep amplitudes of the undesired sinusoids at $\omega = 100$ and $\omega = 3000$ at least 20 dB below the amplitude of the desired sinsuoid. Which filter would you use?

(c) A filter is required for an input signal

$$v_1(t) = 6\cos(400\,t) + 6\cos(800\,t) + 6\cos(1600\,t)$$

that will pass all three sinusoid with about 20 dB gain. Which filter would you use?

12–53 FILTER DESIGN WITH INPUT IMPEDANCE SPECIFIED

Design a circuit whose gain response lies entirely within the unshaded region in Figure P12–53 and whose input impedance is around 50 Ω for most of the frequencies in the passband.

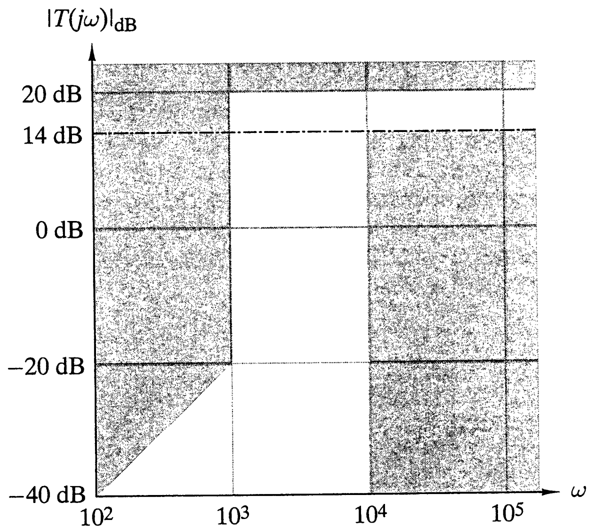


FIGURE P12–53

12–54 HIGH-FREQUENCY MODEL OF A RESISTOR

Figure P12–54 shows a circuit model of a resistor R that includes parasitic capacitance C and parasitic lead inductance L. The purpose of this problem is to investigate the effect of these parasitic elements on the high-frequency characteristics of the resistor device.

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–45 The step response of a linear circuit is

$$g(t) = 5 - 5\,e^{-100t}\sin 200\,t \qquad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–46 The step response of a linear circuit is

$$g(t) = 10\,e^{-100t}\sin 200t \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct a Bode plot of the straight-line approximation to the gain response.

12–47 The step response of a linear circuit is

$$g(t) = e^{-100t} + 2\,e^{-2000t} \quad t > 0$$

Is the circuit a low-pass, high-pass, bandpass, or bandstop filter? Construct Bode plots of the straight-line approximations to the gain and phase responses.

12–48 Construct a first-order low-pass transfer function with a dc gain of 10, a bandwidth less than 250 rad/s, and a step response that rises to 50% of its final value in less than 4 ms.

12–49 Construct a first-order high-pass transfer function whose step response decays to 5% of its peak value in less than 10 μs and whose cutoff frequency is less than 100 kHz.

12–50 Construct a second-order bandpass transfer function with a midband gain of 10, a center frequency of 100 kHz, a bandwidth less than 50 kHz, and a step response that decays to less that 20% of its peak value in less than 5 μs.

INTEGRATING PROBLEMS

12–51 DC, AC, AND IMPULSE RESPONSES

A linear circuit is driven by an input $v_1(t) = 2e^{-1000t}$. The zero-state response for this input is observed to be $v_2(t) = 5e^{-1000t}[1 - \cos(2000t)]$.

(a) Find the steady-state output when the input is $v_1(t) = 4\cos(2000t)$.

(b) Find the steady-state output when the input is 15 V dc.

(c) Construct the Bode plot of the circuit gain as a function of frequency.

(d) Find the circuit impulse response.

12–52 BANDPASS FILTER STEP RESPONSES

The step responses of the two second-order bandpass filters are

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(a) Find the transfer function, center frequency, and bandwidth of each filter. Sketch the Bode plot of the gain response of each filter.

(b) A filter is required for an input signal

$$v_1(t) = 8\cos(100t) + 6\cos(600\,t) + 10\cos(3000\,t)$$

that will pass the desired sinusoid at ω = 600 with about 20 dB gain, and keep amplitudes of the undesired sinusoids at ω = 100 and ω = 3000 at least 20 dB below the amplitude of the desired sinsuoid. Which filter would you use?

(c) A filter is required for an input signal

$$v_1(t) = 6\cos(400\,t) + 6\cos(800\,t) + 6\cos(1600\,t)$$

that will pass all three sinusoid with about 20 dB gain. Which filter would you use?

12–53 FILTER DESIGN WITH INPUT IMPEDANCE SPECIFIED

Design a circuit whose gain response lies entirely within the unshaded region in Figure P12–53 and whose input impedance is around 50 Ω for most of the frequencies in the passband.

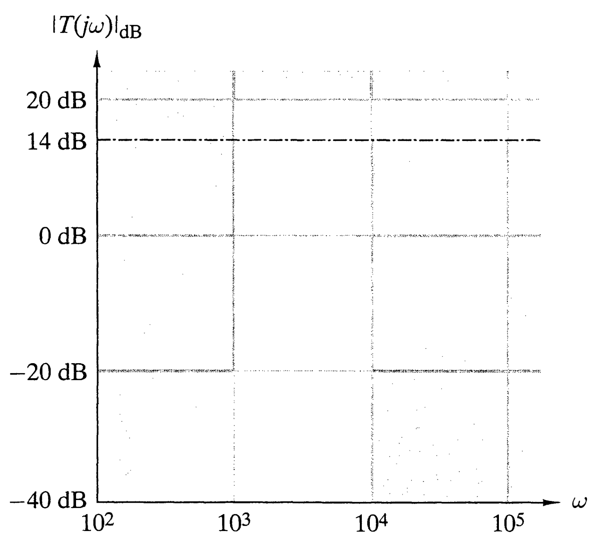

FIGURE P12–53

12–54 HIGH-FREQUENCY MODEL OF A RESISTOR

Figure P12–54 shows a circuit model of a resistor R that includes parasitic capacitance C and parasitic lead inductance L. The purpose of this problem is to investigate the effect of these parasitic elements on the high-frequency characteristics of the resistor device.

(a) Derive an expression for the impedance $Z(s)$ of the circuit model in Figure P12–54 in terms of the circuit parameters R, L, and C.

(b) For $R = 10$ kΩ, $L = 2$ μH, and $C = 4$ pF, find the poles and zeros of $Z(s)$. Construct a Bode plot of the straight-line asymptotes of the impedance magnitude $|Z(j\omega)|$ expressed in ohms. Do not express $|Z(j\omega)|$ in dB. Identify the corner frequencies and slopes (in ohms per decade) in this plot.

(c) Use the straight-line plot in (b) to identify the frequency range (in Hz) over which the resistor device appears to be: (1) a 10-kΩ resistance, (2) a 4-pF capacitance, and (3) a 2-μH inductor.

(d) Over what frequency range can this device be treated as a 10-kΩ resistor?

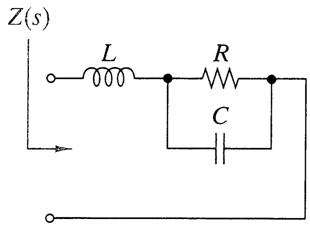

FIGURE P12–54

12–55 COMPENSATOR DESIGN

A modification is required to improve the performance of an existing output transducer. The compensator/transducer combination must meet the following performance specification: *dc gain 0 dB, gain = 0 ±5 dB for ω between 20 rad/s and 200 rad/s, gain slope of –40 dB/dec for ω > 1000 rad/s.* The two designs in Figure P12–55 have been proposed.

(a) Verify that both designs meet the performance specification.

(b) The compensator is to be built using an RC OP AMP circuit with no more than one OP AMP. Which of the two designs would you recommend and why?

(c) Design an OP AMP circuit to implement your recommendation in (b).

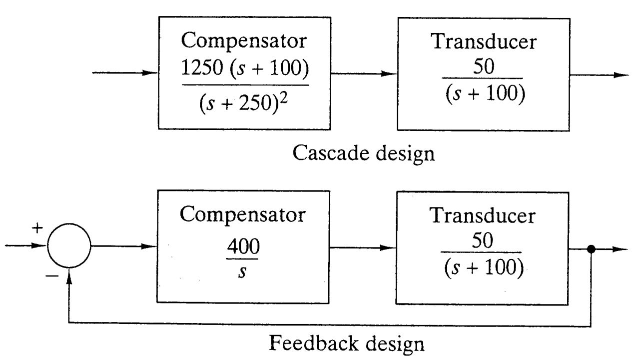

FIGURE P12–55

12–56 USING A BODE PLOT

Figure P12–56 shows the gain response of a second-order filter. The purpose of this problem is to infer things about the performance of the filter with various inputs. The only additional data is that the filter output is an OP AMP with $V_{CC} = \pm 15$ V.

(a) What is the maximum allowable dc input voltage?

(b) Estimate the maximum allowable sinusoidal input voltage at $f = 20$ Hz.

(c) A short rectangular pulse is to be used to evaluate the impulse response of the filter. Estimate the required pulse duration.

(d) What is the final value of the impulse response of the filter? About how long does it take to settle within 1% of this value?

(e) A 0.5-volt step function is to be applied at the input. Estimate the final value of the output response and about how long it takes the response to reach 50% of this value.

(f) The signal $v(t) = 0.5 \sin(100t) + 0.25 \sin(1000t)$ V is to be applied at the input. About how long will it take for a steady-state condition to be reached? What will be the ratio of the steady-state output amplitude at $\omega = 100$ rad/s to the amplitude of the output at $\omega = 1000$ rad/s? Express the ratio in dB.

(g) Your boss needs to know the frequency at which the phase shift is –90°. What is your estimate?

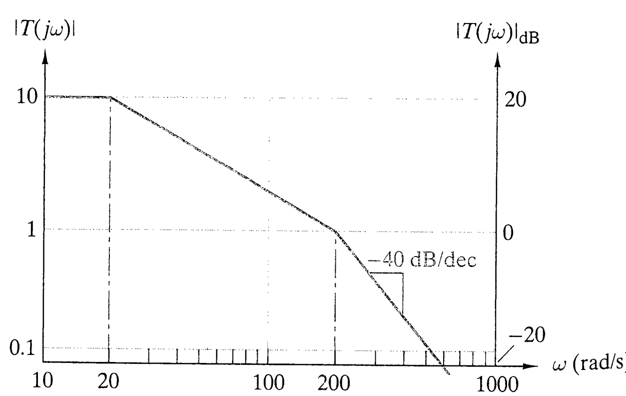

FIGURE P12–56