4

NOISE, BROADBAND, AND HIGH-POWER DESIGN METHODS

4.1 INTRODUCTION

In Chapter 3, design methods for given stability and gain criteria were discussed. This chapter presents the basic principles involved in the design of low-noise, broadband, and high-power transistor amplifiers.

In some applications the design objective is for a minimum noise figure. Since a minimum noise figure and maximum power gain cannot be obtained simultaneously, constant noise figure circles, together with constant available power gain circles, can be drawn on the Smith chart, and reflection coefficients can be selected that compromise between the noise figure and gain performance. The trade-offs that result from noise considerations, stability, and gain are discussed in this chapter.

The noise performance of the GaAs FET is superior to that of the BJT above 4 GHz. A minimum noise figure in both BJTs and GaAs FETs is obtained at low collector or drain current.

The design philosophy in a broadband amplifier is to obtain flat gain over the prescribed range of frequencies. This can be obtained by the use of compensated matching networks, negative feedback, or balance amplifiers.

The small-signal S parameters can be used in the design of microwave transistor amplifiers with linear power output (i.e., class A operation). However, the small-signal S parameters are not useful in the design of large-output power amplifiers. In this case, large-signal impedance or reflection coefficient data as a function of output power and gain are needed.

4.2 NOISE IN TWO-PORT NETWORKS

In a microwave amplifier, even when there is no input signal, a small output voltage can be measured. We refer to this small output power as the *amplifier noise power*. The total noise output power is composed of the amplified noise input power plus the noise output power produced by the amplifier.

The model of a noisy two-port microwave amplifier is shown in Fig. 4.2.1. The noise input power can be modeled by a noisy resistor that produces thermal or Johnson noise. This noise is produced by the random fluctuations of the electrons due to thermal agitation. The rms value of the noise voltage V_N, produced by the noisy resistor R_N over a frequency range $f_H - f_L$, is given by

$$V_N = \sqrt{4kTBR_N} \tag{4.2.1}$$

where k is Boltzmann's constant (i.e., $k = 1.374 \times 10^{-23}$ J/°K), T is the resistor noise temperature, and B is the noise bandwidth (i.e., $B = f_H - f_L$).

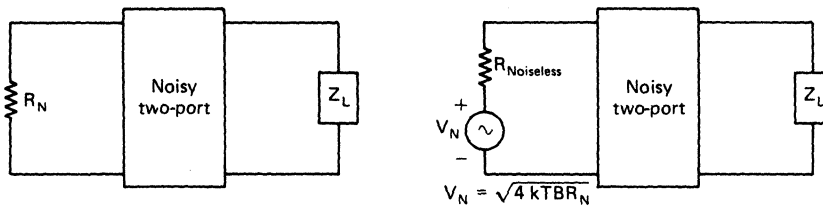


Figure 4.2.1 Model of a noisy microwave amplifier.

Equation (4.2.1) shows that the thermal noise power depends on the bandwidth and not on a given center frequency. Such a distribution of noise is called *white noise.*

The maximum available noise power from R_N is

$$P_N = \frac{V_N^2}{4R_N} = kTB \tag{4.2.2}$$

Example 4.2.1

Calculate the noise voltage and maximum available noise power produced by a 2-MΩ resistor at a standard temperature ($T = 290$°K) in a 5-kHz bandwidth.

Solution. Using (4.2.1) and (4.2.2), the noise voltage and maximum available noise power are

$$V_N = \sqrt{4(1.374 \times 10^{-23})(290)(5 \times 10^3)(2 \times 10^6)} = 12.6\ \mu\text{V}$$

and

$$P_N = \frac{(12.6 \times 10^{-6})^2}{4(2 \times 10^6)} = 19.9 \times 10^{-18}\ \text{W}$$

The noise figure (F) describes quantitatively the performance of a noisy microwave amplifier. The noise figure of a microwave amplifier is defined as the ratio of the total available noise power at the output of the amplifier to the available noise power at the output due to thermal noise from R_N. The noise figure can be expressed in the form

$$F = \frac{P_{N_o}}{P_{N_i} G_A} \tag{4.2.3}$$

where P_{N_o} is the total available noise power at the output of the amplifier, $P_{N_i} = kTB$ is the available noise power due to R_N in a bandwidth B, and G_A is the available power gain.

Since G_A can be expressed in the form

$$G_A = \frac{P_{S_o}}{P_{S_i}}$$

where P_{S_o} is the available signal power at the output and P_{S_i} is the available signal power at the input, then (4.2.3) can be written as

$$F = \frac{P_{S_i}/P_{N_i}}{P_{S_o}/P_{N_o}}$$

In other words, F can also be defined as the ratio of the available signal-to-noise power ratio at the input to the available signal-to-noise power ratio at the output. A minimum noise figure is obtained by properly selecting the source reflection coefficient of the amplifier.

A model for the calculation of the noise figure of a two-stage amplifier is shown in Fig. 4.2.2. P_{N_i} is the available input noise power, G_{A1} and G_{A2} are the available power gains of each stage, and P_{n1} and P_{n2} represent the noise power appearing at the output of amplifiers 1 and 2, respectively, due to the internal amplifier noise.

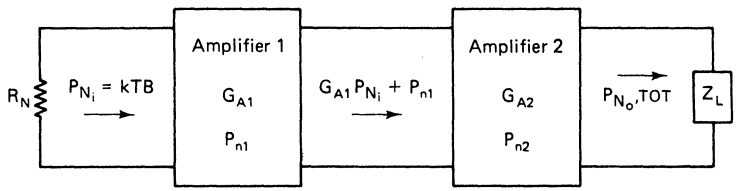


Figure 4.2.2 Noise figure model of a two-stage amplifier.

The total available noise power at the output ($P_{N_o,\text{TOT}}$) is given by

$$P_{N_o,\text{TOT}} = G_{A2}(G_{A1}P_{N_i} + P_{n1}) + P_{n2}$$

Therefore, from (4.2.3) the noise figure of the two-stage amplifier is given by

$$F = \frac{P_{N_o,\text{TOT}}}{P_{N_i} G_{A1} G_{A2}} = 1 + \frac{P_{n1}}{P_{N_i} G_{A1}} + \frac{P_{n2}}{P_{N_i} G_{A1} G_{A2}}$$

or

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} \tag{4.2.4}$$

where

$$F_1 = 1 + \frac{P_{n1}}{P_{N_i} G_{A1}}$$

and

$$F_2 = 1 + \frac{P_{n2}}{P_{N_i} G_{A2}}$$

F_1 and F_2 are recognized as the individual noise figures of the first and second stages, respectively.

Equation (4.2.4) shows that the noise figure of the second stage is reduced by G_{A1}. Therefore, the noise contribution from the second stage is small if G_{A1} is large, and can be significant if the gain G_{A1} is low. It is not always important to minimize the first-stage noise if the gain reduction is too large. In fact, we can select a higher gain, even if F_1 is higher than the minimum noise figure of the first stage, such that a low value of F is obtained. In a design, a trade-off between gain and noise figure is usually made.

4.3 CONSTANT NOISE FIGURE CIRCLES

The noise figure of a two-port amplifier is given by [4.1]

$$F = F_{\min} + \frac{r_n}{g_s} |Y_s - Y_o|^2 \tag{4.3.1}$$

where r_n is the equivalent normalized noise resistance of the two-port (i.e., $r_n = R_N/Z_o$), $Y_s = g_s + jb_s$ represents the source admittance, and $Y_o = g_o + jb_o$ represents that source admittance which results in the minimum noise figure, called $F_{\min}$.

We can express Y_s and Y_o in terms of the reflection coefficients Γ_s and Γ_o, namely

$$Y_s = \frac{1 - \Gamma_s}{1 + \Gamma} \tag{4.3.2}$$

and

$$Y_o = \frac{1 - \Gamma_o}{1 + \Gamma_o} \tag{4.3.3}$$

Substituting (4.3.2) and (4.3.3) into (4.3.1) results in the relation

$$F = F_{\min} + \frac{4r_n |\Gamma_s - \Gamma_o|^2}{(1 - |\Gamma_s|^2)|1 + \Gamma_o|^2} \tag{4.3.4}$$

Equation (4.3.4) depends on $F_{\min}$, r_n, and Γ_o. These quantities are known as the *noise parameters* and are given by the manufacturer of the transistor or can be determined experimentally. The source reflection coefficient can be varied until a minimum noise figure is read in a noise figure meter. The value of $F_{\min}$, which occurs when $\Gamma_s = \Gamma_o$, can be read from the meter, and the source reflection coefficient that produces $F_{\min}$ can be determined accurately using a network analyzer. The noise resistance r_n can be measured by reading the noise figure when $\Gamma_s = 0$, called $F_{\Gamma_s = 0}$. Then, using (4.3.4) we obtain

$$r_n = (F_{\Gamma_s = 0} - F_{\min}) \frac{|1 + \Gamma_o|^2}{4|\Gamma_o|^2}$$

$F_{\min}$ is a function of the device operating current and frequency, and there is one value of Γ_o associated with each $F_{\min}$. A typical plot of $F_{\min}$ versus current for a BJT is illustrated in Fig. 4.3.1.

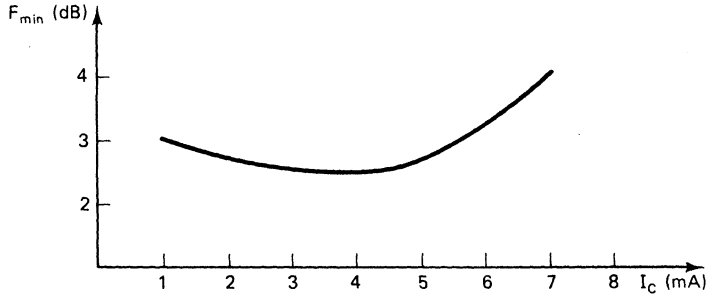


Figure 4.3.1 Typical $F_{\min}$ versus collector current measured at $V_{CE} = 10$ V and $f = 4$ GHz.

Equation (4.3.4) can be used to design Γ_s for a given noise figure. For a given noise figure F_i, we define a noise figure parameter, called N_i, as

$$N_i = \frac{|\Gamma_s - \Gamma_o|^2}{1 - |\Gamma_s|^2} = \frac{F_i - F_{\min}}{4r_n} |1 + \Gamma_o|^2 \tag{4.3.5}$$

Equation (4.3.5) can be written as

$$(\Gamma_s - \Gamma_o)(\Gamma_s^* - \Gamma_o^*) = N_i - N_i |\Gamma_s|^2$$

or

$$|\Gamma_s|^2(1 + N_i) + |\Gamma_o|^2 - 2 \text{ Re } (\Gamma_s \Gamma_o^*) = N_i$$

If we now multiply both sides by $1 + N_i$, we obtain

$$|\Gamma_s|^2(1 + N_i)^2 + |\Gamma_o|^2 - 2(1 + N_i) \text{ Re } (\Gamma_s \Gamma_o^*) = N_i^2 + N_i(1 - |\Gamma_o|^2)$$

or

$$\left| \Gamma_s - \frac{\Gamma_o}{1 + N_i} \right|^2 = \frac{N_i^2 + N_i(1 - |\Gamma_o|^2)}{(1 + N_i)^2} \tag{4.3.6}$$

Equation (4.3.6) is recognized as a family of circles with N_i as a parameter. The circles are centered at

$$C_{F_i} = \frac{\Gamma_o}{1 + N_i} \tag{4.3.7}$$

with radii

$$R_{F_i} = \frac{1}{1 + N_i} \sqrt{N_i^2 + N_i(1 - |\Gamma_o|^2)} \tag{4.3.8}$$

Equations (4.3.5), (4.3.7), and (4.3.8) show that when $F_i = F_{\min}$, then $N_i = 0$, $C_{F_{\min}} = \Gamma_o$, and $R_{F_{\min}} = 0$. That is, the center of the $F_{\min}$ circle is located at Γ_o with zero radius. From (4.3.7), the centers of the other noise figure circles are located along the Γ_o vector.

A typical set of constant noise figure circles is shown in Fig. 4.3.2. This set of curves show that $F_{\min} = 3$ dB is obtained when $\Gamma_s = \Gamma_o = 0.58 \underline{|138°}$ and at point A, $\Gamma_s = 0.38 \underline{|119°}$ produces $F_i = 4$ dB.

In a design there is always a difference between the designed noise figure and the measured noise figure of the final amplifier. This occurs because of the loss associated with the matching elements and the transistor noise figure variations from unit to unit. Typically, the noise figure difference can be from a fraction of a decibel to 1 dB in a narrowband design.

In the unilateral case, a set of G_s constant-gain circles can be drawn in the Smith chart containing the noise figure circles. A typical plot for a GaAs FET is illustrated in Fig. 4.3.3. This plot shows the trade-offs that can be made between gain and noise figure in a design. Maximum gain and minimum noise figure cannot, in general, be obtained simultaneously. In Fig. 4.3.3, the maximum G_s gain of 3 dB, obtained with $\Gamma_s = 0.7 \underline{|110°}$, results in a noise figure of $F_i \approx 4$ dB; and the minimum noise figure $F_{\min} = 0.8$ dB, obtained with $\Gamma_s = 0.6 \underline{|40°}$, results in a gain $G_s \approx -1$ dB.

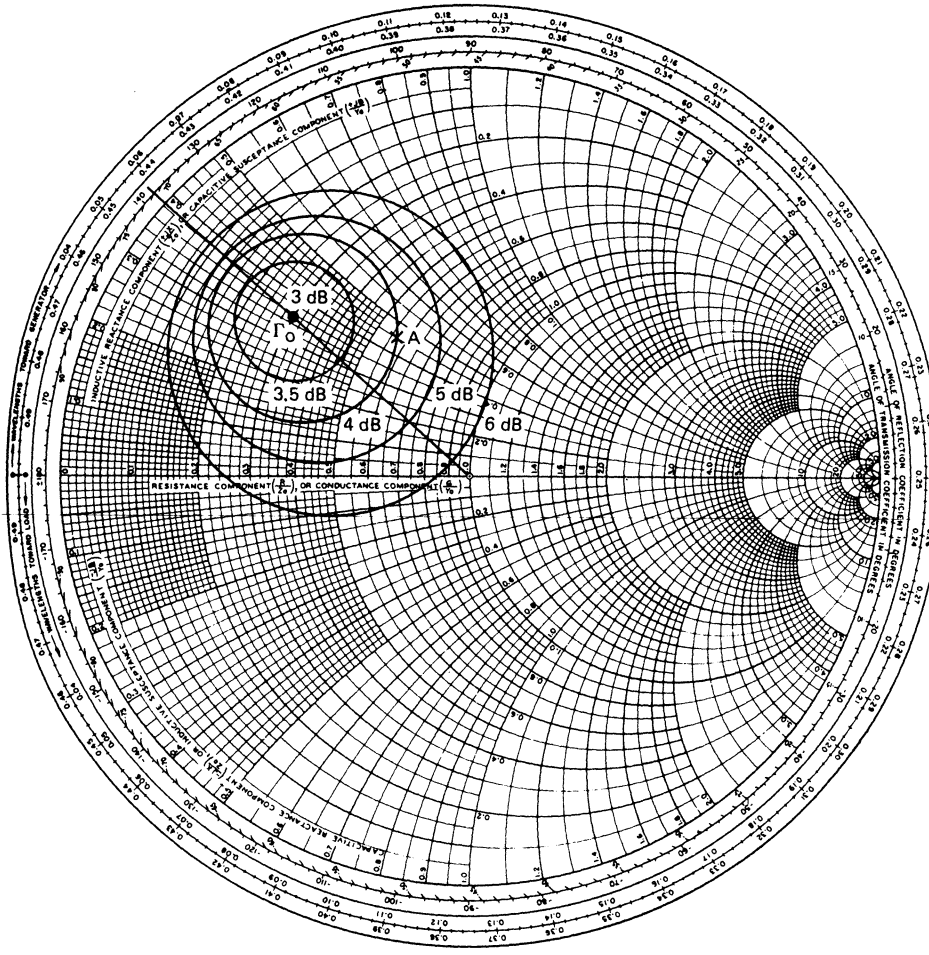


Figure 4.3.2 Typical constant noise figure circles in the Γ_s plane.

Example 4.3.1

The scattering and noise parameters of a BJT measured at a bias point for low-noise operation ($V_{CE} = 10$ V, $I_C = 4$ mA) at $f = 4$ GHz are

$$S_{11} = 0.552\angle 169°$$

$$S_{12} = 0.049\angle 23°$$

$$S_{21} = 1.681\angle 26°$$

$$S_{22} = 0.839\angle -67°$$

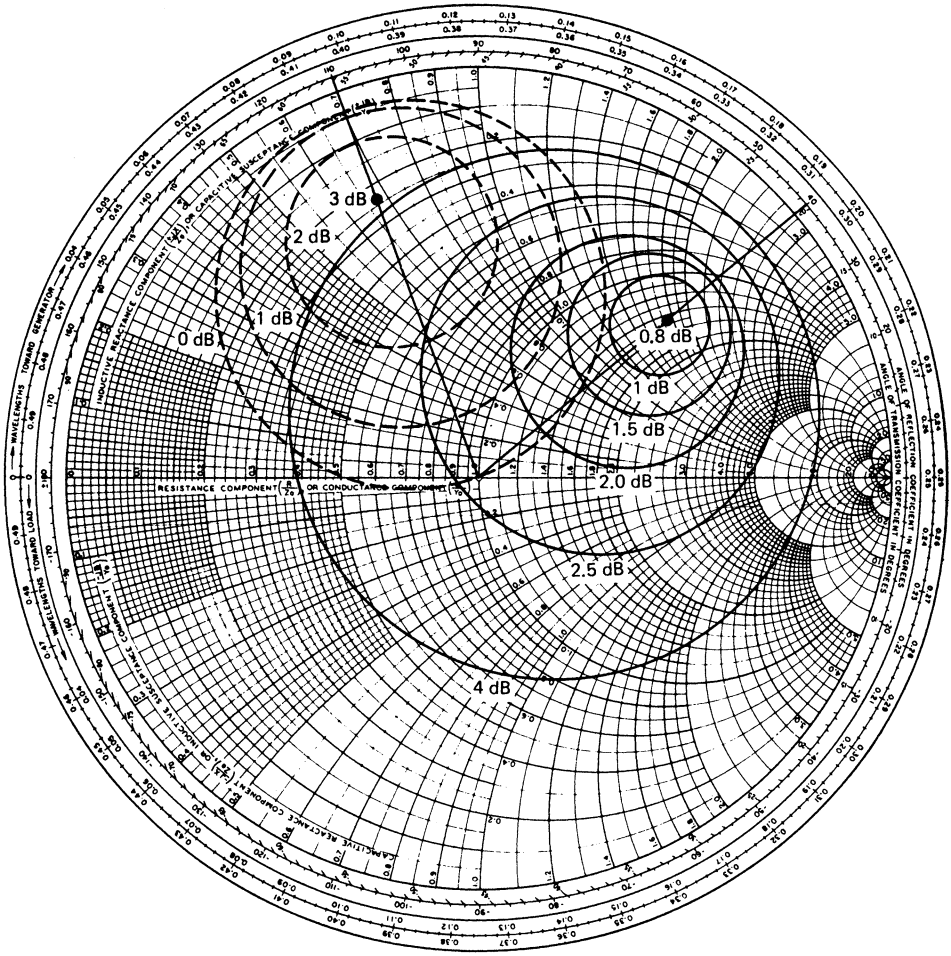


Figure 4.3.3 Noise figure circles (solid curves) and G_s constant-gain circles (dashed curves). The transistor is a GaAs FET with $V_{DS} = 4$ V, $I_{DS} = 12$ mA, and $f =$ 6 GHz.

and

$$F_{\min} = 2.5 \text{ dB}$$

$$\Gamma_o = 0.475 \angle 166°$$

$$R_N = 3.5\ \Omega$$

Design a microwave transistor amplifier to have a minimum noise figure. (This example is based on a design from Hewlett-Packard Application Note 967 [4.2].)

Solution. The transistor is unconditionally stable at 4 GHz. A minimum noise figure of 2.5 dB is obtained with $\Gamma_s = \Gamma_o = 0.475\angle 166°$. The constant noise figure circles in Fig. 4.3.4 for $F_i = 2.5$ to 3 dB were calculated using (4.3.5), (4.3.7), and (4.3.8). For example, the $F_i = 2.8$-dB circle was obtained as follows:

$$N_i = \frac{1.905 - 1.778}{4(3.5/50)}|1 + 0.475\angle 166°|^2 = 0.1378$$

$$C_{F_i} = \frac{0.475\angle 166°}{1 + 0.1378} = 0.417\angle 166°$$

and

$$R_{F_i} = \frac{1}{1 + 0.1378}\sqrt{(0.1378)^2 + 0.1378[1 - (0.475)^2]} = 0.312$$

Figure 4.3.4 shows that for this transistor $F_{\min}$ is not very sensitive to small variations in Γ_s around Γ_o. In fact, the 2.6-dB constant-noise circle (i.e., a 0.1-dB increase in noise figure) results when Γ_s changes in magnitude by 0.2 from its value at Γ_o.

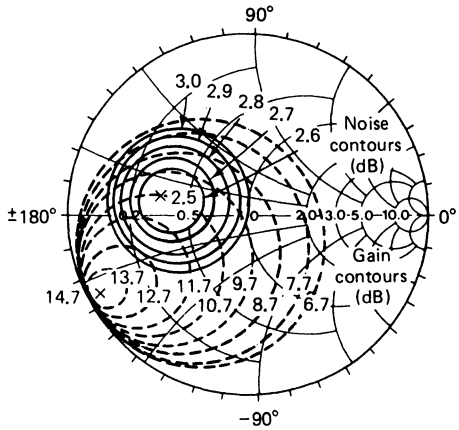


Figure 4.3.4 Constant noise figure circles and available power gain circles. (From Ref. [4.2]; courtesy of Hewlett-Packard.)

The load reflection coefficient is selected to provide maximum gain for the lowest noise figure (i.e., with $\Gamma_s = \Gamma_o$) and, of course, for optimum VSWR at the output. Therefore,

$$\Gamma_L = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_o}{1 - S_{11}\Gamma_o}\right)^* = 0.844\angle 70.4°$$

and the resulting gains are $G_T = G_A = 11$ dB and $G_p = 12.7$ dB.

The amplifier was designed, built, and tested by Hewlett-Packard [4.2]. The ac amplifier schematic is shown in Fig. 4.3.5. The input matching network was designed with a short-circuited stub and a quarter-wave transformer with $Z_o = 31.1\ \Omega$. The output matching network was designed with a 0.61-cm microstrip line to provide soldering area, followed by a $\lambda/8$ short-circuited stub to tune out most of the susceptance component of $Y_1 = 1/Z_1$. Then, another series microstrip line followed by an

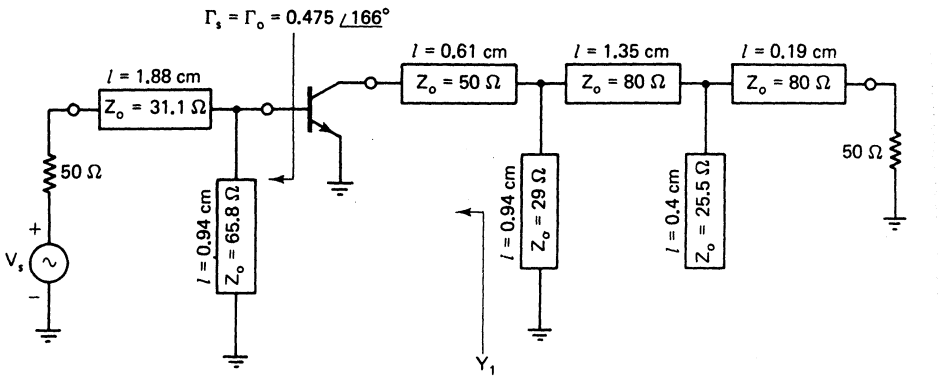


Figure 4.3.5 Amplifier schematic. The microstrip lengths are given for $\varepsilon_{ff} = 1$ at $f = 4$ GHz. (From Ref. [4.2]; courtesy of Hewlett-Packard.)

open stub that provides some tuning capabilities was used. A final series microstrip line was used to obtain the match to 50 Ω.

Of course, the output matching network could have been designed differently. The form selected (see Fig. 4.3.5) provides flexibility for tuning by adjusting the lengths of the series lines (i.e., the $l = 1.35$-cm and $l = 0.19$-cm lines), by changing the width (i.e., the characteristic impedance) of the open-circuited stub and by modifying the lengths of the short-circuited stub.

The complete amplifier schematic and the microstrip board layout are shown in Fig. 4.3.6. The board material is Duroid ($\varepsilon_r = 2.23$, $h = 0.031$ in.).

The measured characteristics of the amplifier are shown in Fig. 4.3.7. Figure 4.3.7 shows that the amplifier performance is very good in the frequency range 3.7 to 4.2 GHz. The 3-dB bandwidth (see Fig. 4.3.7e) is 850 MHz, which corresponds to a 21% bandwidth.

It is easy to show that for this BJT, $K = 1.012$, $\Delta = 0.419 \lfloor 111.04°$, $G_{T,\max} = G_{A,\max} = 14.7$ dB, $\Gamma_{Ms} = 0.941 \lfloor -154°$, and $\Gamma_{ML} = 0.979 \lfloor 70°$. Since the available power gain with $\Gamma_s = \Gamma_o$ is $G_A = 11$ dB, a sacrifice in gain was needed to obtain optimum noise performance.

Example 4.3.2

The scattering and noise parameters of a GaAs FET measured at three different optimum bias settings at $f = 6$ GHz are:

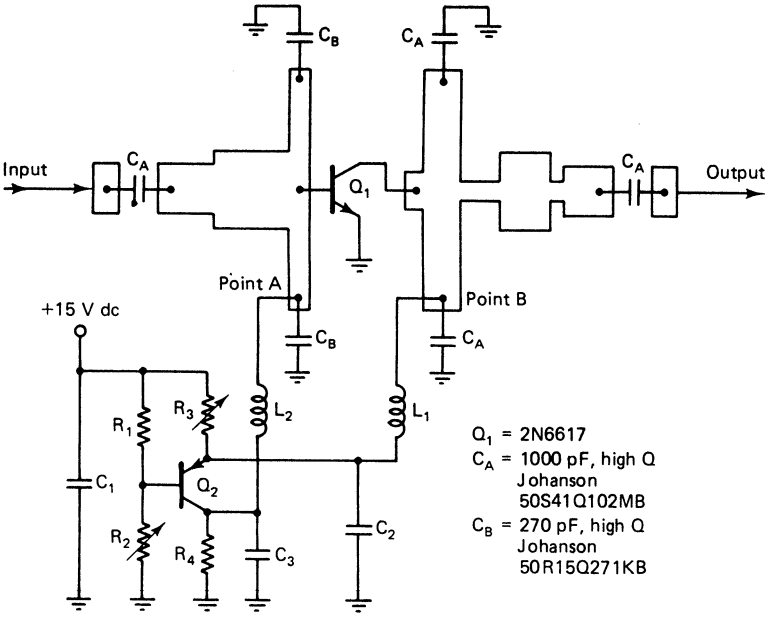
Minimum Noise Figure ($V_{DS} = 3.5$ V, $I_{DS} = 15\% I_{DSS}$):

$$S_{11} = 0.674 \lfloor -152° \qquad F_{\min} = 2.2 \text{ dB}$$

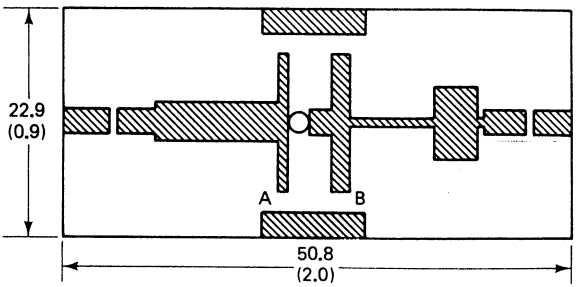
$$S_{12} = 0.075 \lfloor 6.2° \qquad \Gamma_o = 0.575 \lfloor 138°$$

$$S_{21} = 1.74 \lfloor 36.4° \qquad R_N = 6.64\ \Omega$$

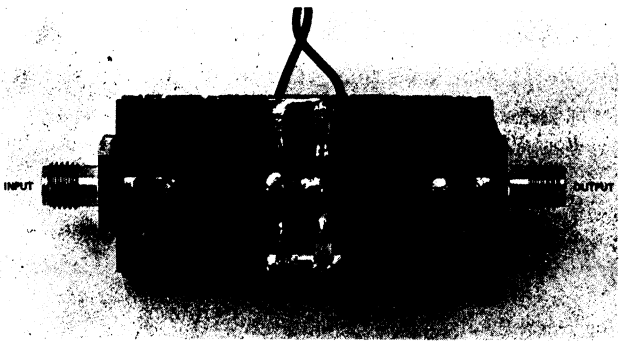
$$S_{22} = 0.6 \lfloor -92.6°$$



(a)

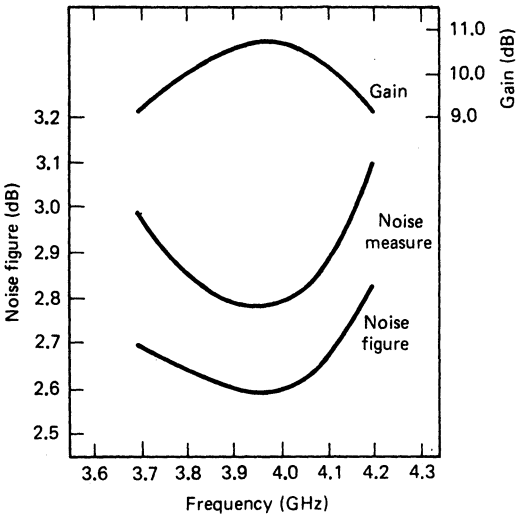


Dimensions in millimeters (inches)

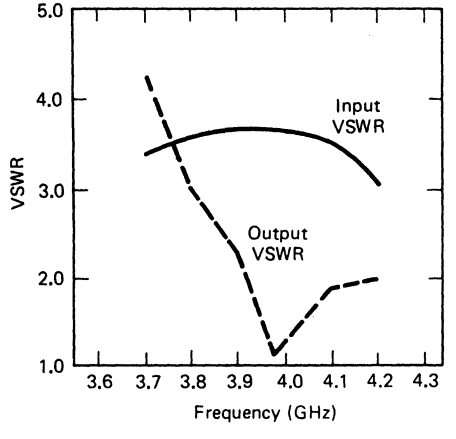


(b)

Figure 4.3.6 (a) Complete amplifier schematic; (b) microstrip board layout. (From Ref. [4.2]; courtesy of Hewlett-Packard.)



(a)



(b)

Figure 4.3.7 Measured amplifier characteristics: (a) noise and gain performance; (b) input–output VSWR performance; (c) power output performance; (d) temperature performance at 4 GHz; (e) wideband gain performance. (From Ref. [4.2]; courtesy of Hewlett-Packard.)

Linear Power Output ($V_{DS} = 4$ V, $I_{DS} = 50\% I_{DSS}$):

$$S_{11} = 0.641 \angle -171.3° \qquad F_{\min} = 2.9 \text{ dB}$$

$$S_{12} = 0.057 \angle 16.3° \qquad \Gamma_o = 0.542 \angle 141°$$

$$S_{21} = 2.058 \angle 28.5° \qquad R_N = 9.42\ \Omega$$

$$S_{22} = 0.572 \angle -95.7°$$

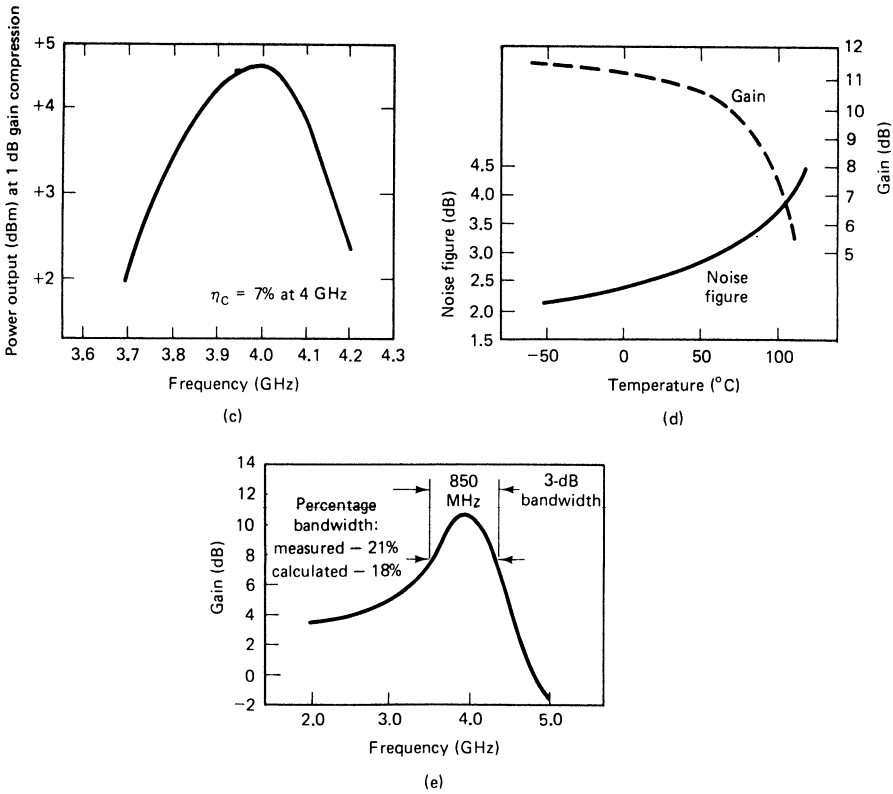


Figure 4.3.7 (*continued*)

Maximum Gain ($V_{DS} = 4$ V, $I_{DS} = 100\% I_{DSS}$):

$$S_{11} = 0.614 \angle -167.4°$$

$$S_{12} = 0.046 \angle 65°$$

$$S_{21} = 2.187 \angle 32.4°$$

$$S_{22} = 0.716 \angle -83°$$

Design a microwave transistor amplifier to have good ac performance. (This example is based on a design from Hewlett-Packard Application Note 970 [4.3].)

Solution. There are four ac performances that must be considered: noise figure, power gain, power output, and input and output VSWR. The linear power-output bias point ($V_{DS} = 4$ V, $I_{DS} = 50\% I_{DSS}$) provides a good compromise between the minimum noise figure and maximum gain. At this bias point Fig. 4.3.8 gives the noise, gain, and power parameters. The output power performance, measured at the 1-dB compression point, was experimentally measured and it is given in the figure. (See Section 4.7 for the definition of the 1-dB compression point.) The data for the output power were taken with an input power drive of 8.3 dBm.

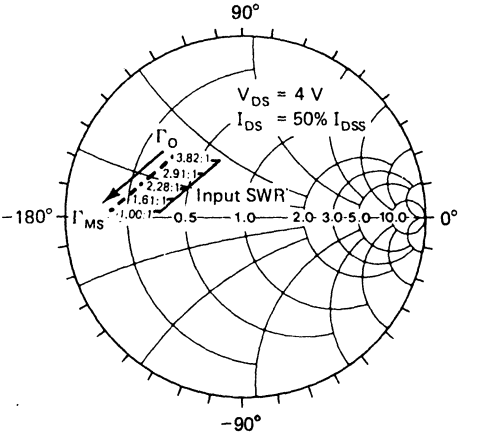
Noise Parameters	Gain Parameters	Power Parameters
$\Gamma_o = 0.542 \angle 141°$	$\Gamma_{Ms} = 0.762 \angle 177.3°$	$\Gamma_{PS} = 0.729 \angle 166°$
$\Gamma_L = 0.575 \angle 104.5°$	$\Gamma_{ML} = 0.718 \angle 103.9°$	$\Gamma_{PL} = 0.489 \angle 101°$
$F_{min} = 2.9$ dB	$F = 4.44$ dB	$F = 3.69$ dB
$G_A = 9.33$ dB	$G_{A,max} = 11.38$ dB	$G_p = 8.2$ dB
$P_{1dB} = 9.3$ dBm	$P_{1dB} = 13.4$ dBm	$P_{1dB} = 15.5$ dBm

Figure 4.3.8 Noise, gain, and power parameters at the linear power output bias ($V_{DS} = 4$ V, $I_D = 50\% I_{DSS}$).

The input VSWR with $\Gamma_s = \Gamma_{Ms}$ is 1, and the VSWR = 3.82 with $\Gamma_s = \Gamma_o$. In order to calculate the VSWR, we obtained $|\Gamma_a|$ (see Fig. 4.3.10a) and used (1.3.11), namely

$$\text{VSWR} = \frac{1 + |\Gamma_a|}{1 - |\Gamma_a|}$$

Other relations for calculating $|\Gamma_a|$ are given in Problem 4.6.



Γ_s	Mag./Ang.	Γ_L Mag./Ang.	F (dB)	G_A (dB)	Input VSWR	Output VSWR
Γ_o –	0.542 ∠141°	0.575 ∠104°	2.90	9.33	3.82:1	1.00:1
	0.572 ∠152°	0.601 ∠105°	2.97	10.04	2.91:1	1.00:1
	0.614 ∠160°	0.627 ∠106°	3.14	10.55	2.28:1	1.00:1
	0.678 ∠169°	0.667 ∠105°	3.57	11.10	1.61:1	1.00:1
Γ_{Ms} –	0.762 ∠177°	0.718 ∠104°	4.44	11.38	1.00:1	1.00:1

Figure 4.3.9 Trade-offs between noise figure, power gain, and VSWR. (From Ref. [4.3]; courtesy of Hewlett-Packard.)

Figure 4.3.9 shows the noise figure, G_A and input and output VSWR as the reflection coefficient is varied from Γ_o to Γ_{Ms}, along a straight line, in the Smith chart. Figure 4.3.9 shows that a good compromise between noise figure, G_A, and VSWR is to use $\Gamma_s = 0.614 \angle 160°$ and $\Gamma_L = 0.627 \angle 106°$. The noise figure is increased by 0.24 dB from the minimum noise, but G_A is increased by 1.22 dB and the input VSWR is improved by 40% (i.e., VSWR = 2.28). The ac schematic of the amplifier for the selected values of Γ_s and Γ_L is shown in Fig. 4.3.10a and the microstrip board layout is shown in Fig. 4.3.10b. The board material is Duroid ($\varepsilon_r = 2.23$, $h = 0.031$ in.). The measured characteristics of the amplifier are shown in Fig. 4.3.11.

In the last two examples the transistors were unconditionally stable. In a potentially unstable situation, we must check that the optimum noise reflection coefficient $\Gamma_s = \Gamma_o$ is in the stable region of the source stability circle. Once Γ_s is selected, Γ_L is selected for maximum gain (i.e., $\Gamma_L = \Gamma^*_{OUT}$), and again we must check that the value of Γ_L is in the stable region of the load stability circle.

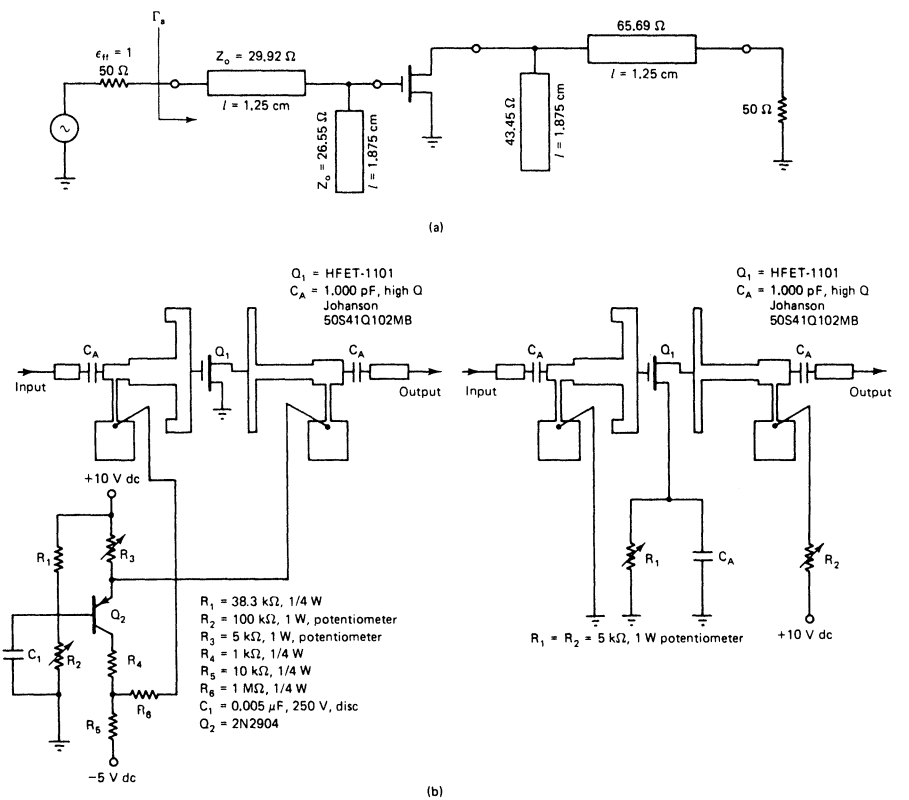


Figure 4.3.10 (a) The ac schematic of the amplifier with $\varepsilon_{ff} = 1$; (b) microstrip layout with two different dc bias networks. (From Ref. [4.3]; courtesy of Hewlett-Packard.)

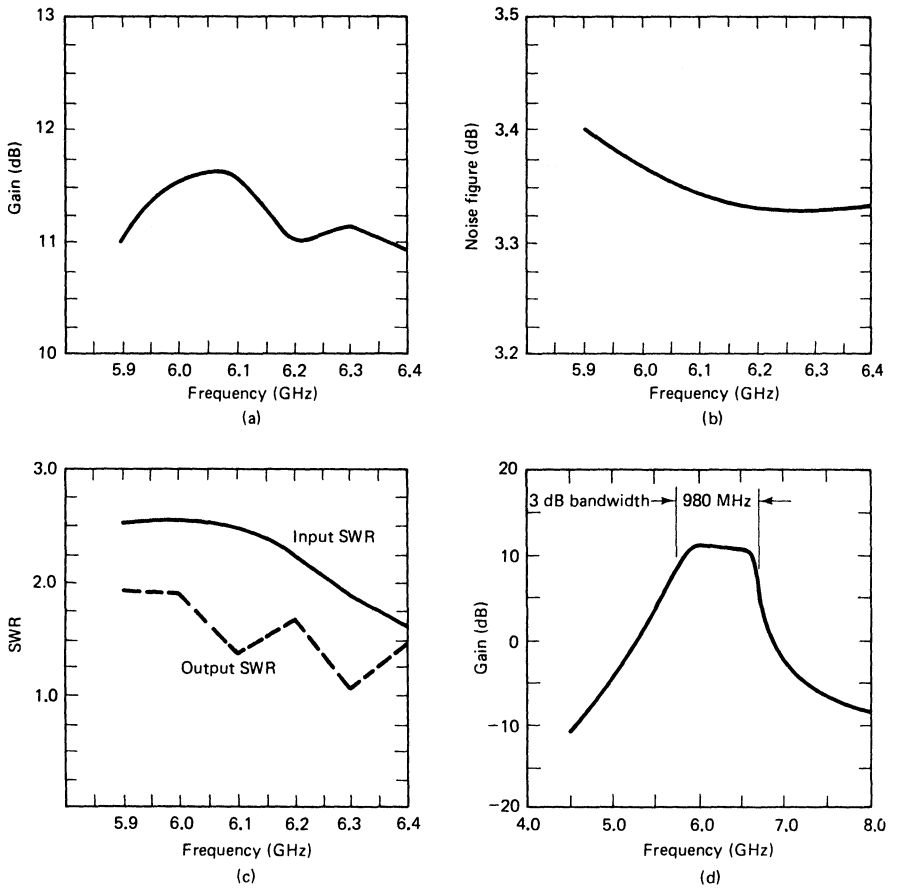


Figure 4.3.11 Measured characteristics of the amplifier: (a) gain performance; (b) noise performance; (c) input–output VSWR performance; (d) wideband gain performance. (From Ref. [4.3]; courtesy of Hewlett-Packard.

4.4 BROADBAND AMPLIFIER DESIGN

The design of broadband amplifiers introduces new difficulties which require careful considerations. Basically, the design of a constant-gain amplifier over a broad frequency range is a matter of properly designing the matching networks, or the feedback network, in order to compensate for the variations of $|S_{21}|$ with frequency. The design specifications might require the use of rather sophisticated synthesis procedures in the design of the matching networks.

Some of the difficulties encountered in the design of a broadband amplifier are:

1. The variations of $|S_{21}|$ and $|S_{12}|$ with frequency. Typically, $|S_{21}|$ decreases with frequency at the rate of 6 dB/octave and $|S_{12}|$ increases with frequency at the same rate. Typical variations of $|S_{21}|$, $|S_{12}|$, and $|S_{12}S_{21}|$ with frequency are illustrated in Fig. 1.9.7. The variations of $|S_{12}S_{21}|$ with frequency is important since the stability of the circuit depends on this quantity. It is in the flat region that we have to check the amplifier stability.
2. The scattering parameters S_{11} and S_{22} are also frequency dependent and their variations are significant over a broad range of frequencies.
3. There is a degradation of the noise figure and VSWR in some frequency range of the broadband amplifier.

Two techniques that are commonly used to design broadband amplifiers are (1) the use of compensated matching networks and (2) the use of negative feedback.

The technique of compensated matching networks involves mismatching the input and output matching networks to compensate for the changes with frequency of $|S_{21}|$. The matching networks are designed to give the best input and output VSWR. However, because of the broad bandwidth the VSWR will be optimum around certain frequencies, and a balanced amplifier design may be required.

The design of compensated matching networks can be done in analytical form with the help of the Smith chart. However, the use of a computer is usually required because of the complex analytical procedures. Of course, the use of a proper analytical procedure produces a starting design which can be optimized using computer-aided design (CAD) methods.

The matching networks can also be designed using network synthesis techniques. Passive network synthesis for the design of networks using lumped elements is well developed, and the techniques to implement the filter with microwave components are also well known [4.4, 4.5]. The microwave filters, typically, operate between two different impedances and must provide a prescribed insertion loss and bandwidth.

Insertion-loss synthesis techniques can be used to design impedance matching networks with prescribed responses. The synthesis process is a powerful tool when used in a CAD program. A good commercially available program is AMPSYN [4.6]. AMPSYN is a user-oriented interactive program for obtaining impedance matching networks with a desired frequency characteristic. AMPSYN synthesizes lumped elements matching networks and provides for transformations of the lumped design to approximate transmission-line equivalents.

An interesting method for broadband amplifier design suitable to CAD has been developed by Mellor [4.7]. The broadband design involves the use of an interstage matching network. The amplifier schematic is shown in Fig. 4.4.1.

Transistors Q_1 and Q_2 have a gain that decreases with increasing fre-

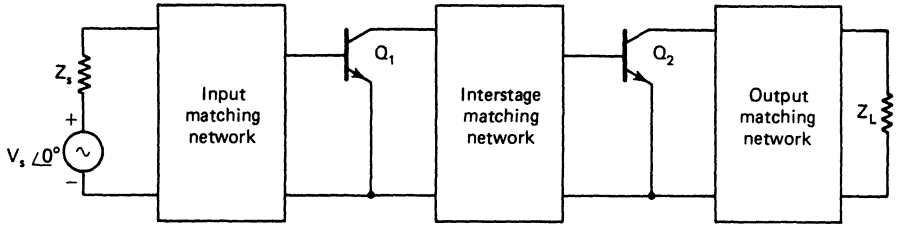


Figure 4.4.1 Broadband amplifier schematic.

quency. The specifications for a good input and output match will require that the input and output matching networks have a constant gain over the frequency range of the amplifier (i.e., a flat frequency response). The interstage matching network must provide a gain having a positive slope with increasing frequency to compensate for the transistor roll-off and, therefore, to give an overall flat frequency response. The synthesis approach involves modeling the transistors with lumped elements and using an insertion-loss method to obtain the matching networks. The design of a broadband amplifier for a specific gain and noise figure requires, in general, the use of CAD techniques.

Example 4.4.1

The S parameters of a BJT are given in Fig. 4.4.2. Design a broadband amplifier with a transducer power gain of 10 dB in the frequency range 300 to 700 MHz. (This example is based on a design from Hewlett-Packard Application Note 95-1 [4.8].)

f (MHz)	S_{11}	S_{21}	S_{22}
300	$0.3\lfloor -45°$	$4.47\lfloor 40°$	$0.86\lfloor -5°$
450	$0.27\lfloor -70°$	$3.16\lfloor 35°$	$0.855\lfloor -14°$
700	$0.2\lfloor -95°$	$2.0\lfloor 30°$	$0.85\lfloor -22°$

Figure 4.4.2 Scattering parameters of a BJT.

Solution. The values in Fig. 4.4.2 show that

$$\begin{aligned} |S_{21}|^2 &= 13 \text{ dB} \quad \text{at} \quad 300 \text{ MHz} \\ &= 10 \text{ dB} \quad \text{at} \quad 450 \text{ MHz} \\ &= 6 \text{ dB} \quad \text{at} \quad 700 \text{ MHz} \end{aligned}$$

Therefore, in order to compensate for the variations of $|S_{21}|$, the matching networks must decrease the gain by 3 dB at 300 MHz, 0 dB at 450 MHz, and increase the gain by 4 dB at 700 MHz.

For this transistor

$$G_{s,\max} = \frac{1}{1 - |S_{11}|^2} = \begin{cases} 0.409 \text{ dB} & \text{at} \quad 300 \text{ MHz} \\ 0.329 \text{ dB} & \text{at} \quad 450 \text{ MHz} \\ 0.177 \text{ dB} & \text{at} \quad 700 \text{ MHz} \end{cases}$$

and little is to be gained by matching the source. Therefore, only the output matching network needs to be designed. Observe that $|S_{22}| \approx 0.85$ over the frequency range. Therefore,

$$G_{L,\max} = \frac{1}{1 - |S_{22}|^2} = 5.6 \text{ dB}$$

and the gain of 4 dB from G_L at 700 MHz is possible.

The output matching network is designed by plotting the constant-gain circles for $G_L = -3$ dB at 300 MHz, $G_L = 0$ dB at 450 MHz, and $G_L = 4$ dB at 700 MHz (see Fig. 4.4.3). The matching networks must transform the 50-Ω load to some point on the −3-dB circle at 300 MHz, to some point on the 0-dB circle at 450 MHz, and to some point on the 4-dB gain circle at 700 MHz. Of course, there are many matching networks that can perform the required transformation. The matching network selected is an ell network consisting of a shunt and series inductor combination (see Fig. 4.4.4).

The shunt inductor susceptance decreases with frequency and transforms the 50-Ω load along the constant-conductance circle as shown in Fig. 4.4.3. The series inductor reactance increases with frequency and transforms the parallel combination of 50 Ω and shunt inductance along a constant-resistance circle as shown in Fig. 4.4.3. Optimizing the values of L_1 and L_2 is a trial-and-error procedure. The graphical construction is illustrated in Fig. 4.4.3 and the final ac schematic of the amplifier is shown in Fig. 4.4.4.

The value of L_1 is obtained at 300 MHz (i.e., the lowest frequency), from Fig. 4.4.3, as

$$\frac{50}{j\omega L_1} = -j1.2$$

or

$$L_1 = 22.1 \text{ nH}$$

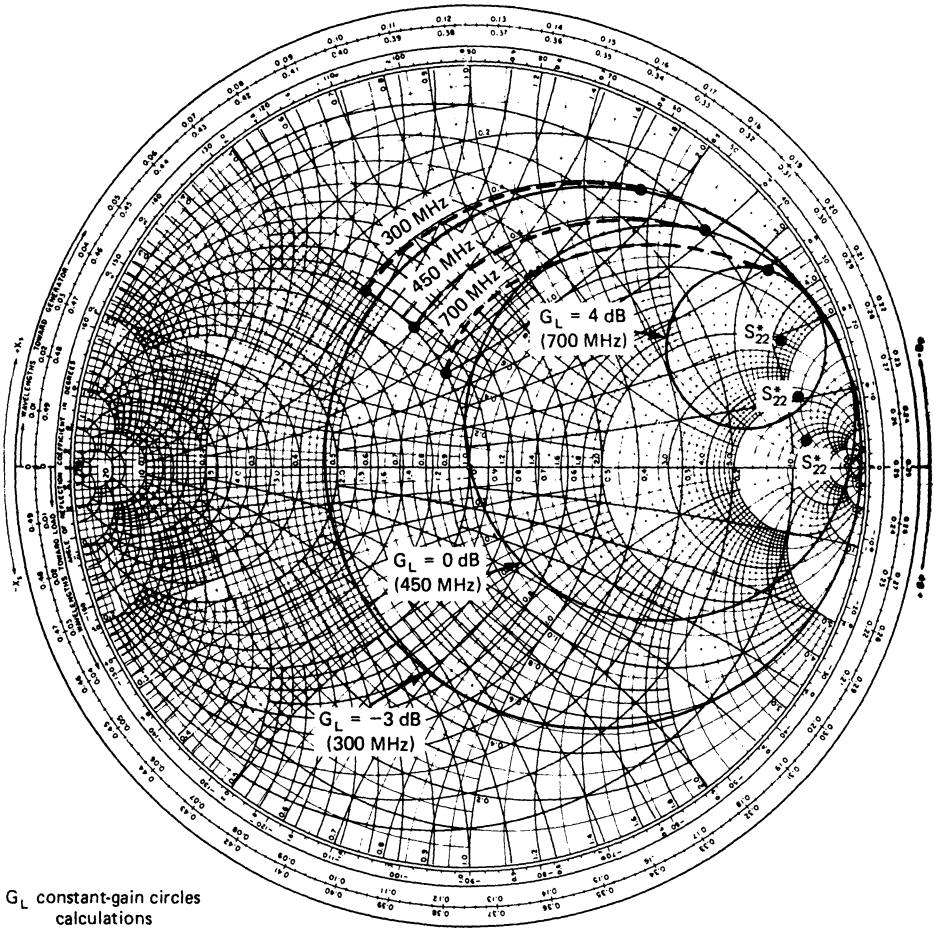
and the value of L_2 is obtained at 700 MHz (i.e., the highest frequency), from Fig. 4.4.3, as

$$\frac{j\omega L_2}{50} = j(3.2 - 0.4)$$

or

$$L_2 = 31.8 \text{ nH}$$

At the input, the direct connection of the 50-Ω source resistor to the base of the transistor results in $G_s = 0$ dB and an input VSWR smaller than 1.86 [i.e.,



G_L constant-gain circles calculations

F (MHz)	Center	Radius
300	0.31	0.68
450	0.49	0.49
700	0.76	0.2

Figure 4.4.3 Broadband design in the Smith chart.

$(1 + 0.3)/(1 - 0.3) = 1.86$]. The VSWR can be improved by matching the 50-Ω source to S_{11} over the frequency band. The corresponding improvement in gain is small since $G_{s,\max} = 0.409$ dB at $f = 300$ MHz.

The design of compensated matching networks to obtain gain flatness results in impedance mismatching that can significantly degrade the input and output VSWR. The use of balanced amplifiers is a practical method for obtaining a broadband amplifier with flat gain and good

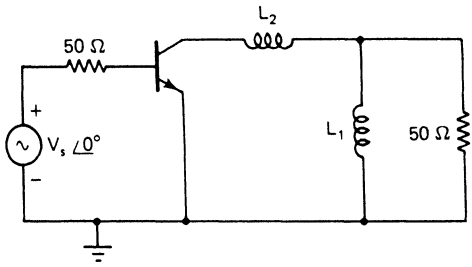


Figure 4.4.4 The ac schematic of the broadband amplifier.

VSWR. The most popular arrangement of a balanced amplifier, shown in Fig. 4.4.5, uses two 3-dB hybrid couplers. A microstrip realization, shown in Fig. 4.4.6, uses an interdigitated structure which is known as the 3-dB *Lange coupler* [4.9].

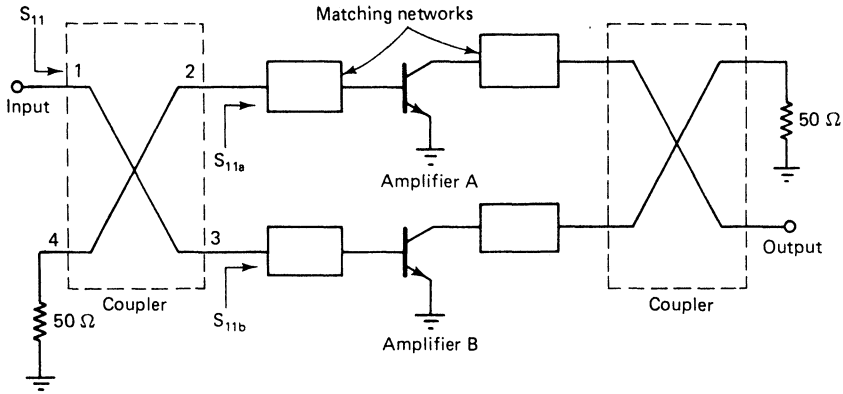


Figure 4.4.5 Balanced amplifier configuration.

The input 3-dB coupler divides the input power equally between ports 2 and 3, and the output 3-dB coupler recombines the output signals from the amplifiers. The reflected signals at the input and output due to mismatching are coupled to the 50-Ω loads. It can be shown that the S parameters of the $\lambda/4$, 3-dB Lange coupler are given by

$$|S_{11}| = 0.5|S_{11_a} - S_{11_b}|$$

$$|S_{21}| = 0.5|S_{21_a} + S_{21_b}|$$

$$|S_{12}| = 0.5|S_{12_a} + S_{12_b}|$$

$$|S_{22}| = 0.5|S_{22_a} - S_{22_b}|$$

If the two amplifiers are identical, then $S_{11} = 0$ and $S_{22} = 0$ and the gain S_{21}

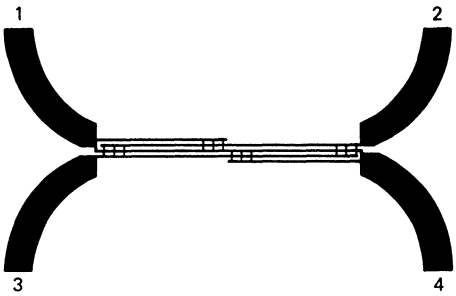


Figure 4.4.6 A 3-dB Lange coupler. (From J. Lange [4.9]; copyright 1969, IEEE; reproduced with permission of IEEE.)

the balanced amplifier is limited by the bandwidth of the coupler (about 2 octaves).

The advantages of the balanced amplifier configuration are many:

1. The individual amplifiers can be designed for flat gain, noise figure, and so on (even if the individual amplifier VSWR is high), with the balanced amplifier input and output VSWR dependent on the coupler (i.e., ideally the VSWR is 1 if the amplifiers are identical).
2. A high degree of stability.
3. The output power is twice that obtained from the single amplifier.
4. If one of the amplifiers fails, the balanced amplifier unit will still operate with reduced gain.
5. Balanced amplifier units are easy to cascade with other units, since each unit is isolated by the coupler.

The disadvantages of the balanced amplifier configuration are that the unit uses two amplifiers, consumes more dc power, and is larger.

Negative feedback can be used in broadband amplifiers to provide a flat gain response and to reduce the input and output VSWR. It also controls the amplifier performance due to variations in the S parameters from transistor to transistor. As the bandwidth requirements of the amplifier approach a decade of frequency, gain compensation based on matching networks only is very difficult, and negative feedback techniques are used. In fact, a microwave transistor amplifier using negative feedback can be designed to have very wide bandwidths (greater than 2 decades) with small gain variations (tenths of a decibel). On the minus side, negative feedback will degrade the noise figure and reduce the maximum power gain available from a transistor.

The most common methods of applying negative feedback are by the series and shunt resistor feedback configurations shown in Fig. 4.4.7. The coupling capacitors and the dc bias network have been omitted.

The following simple analysis illustrates the use of negative feedback. The BJT and GaAs FET can be represented by the equivalent circuit shown in Fig. 4.4.8 when the parasitic elements can be neglected (i.e., at low frequencies)

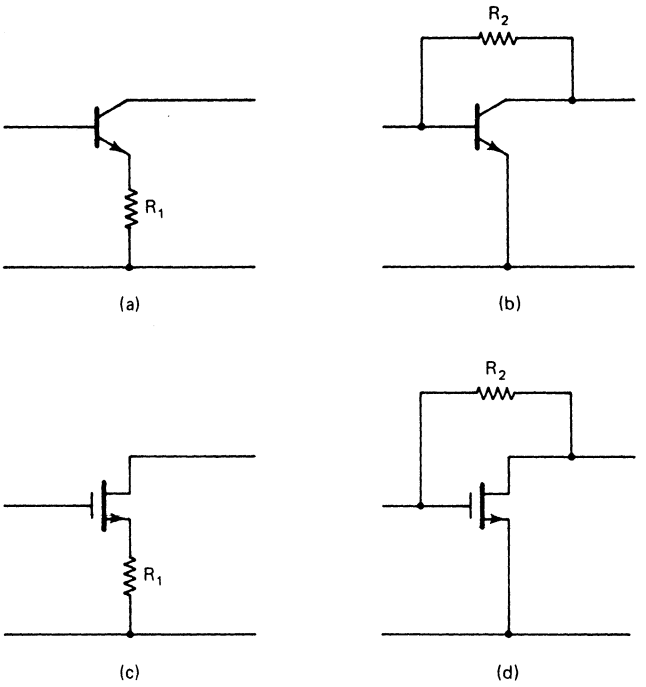


Figure 4.4.7 (a) BJT with series feedback resistor; (b) BJT with shunt feedback resistor; (c) GaAs FET with series feedback resistor; (d) GaAs FET with shunt feedback resistor.

The resulting negative-feedback equivalent networks, including both series and shunt feedback, are shown in Fig. 4.4.9.

The admittance matrix for the network shown in Fig. 4.4.9b can be written in the form

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \dfrac{1}{R_2} & -\dfrac{1}{R_2} \\ \dfrac{g_m}{1+g_m R_1} - \dfrac{1}{R_2} & \dfrac{1}{R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

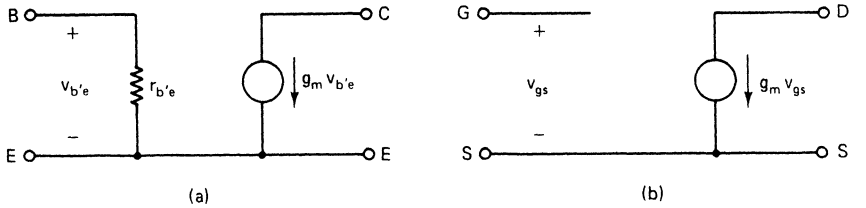


Figure 4.4.8 (a) BJT equivalent network; (b) GaAs FET equivalent network.

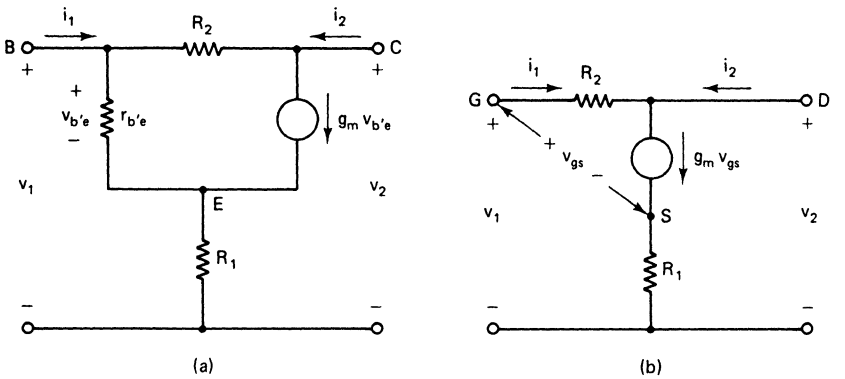


Figure 4.4.9 (a) BJT negative-feedback model; (b) GaAs FET negative-feedback model.

and a similar matrix can be written for Fig. 4.4.9a. Using Fig. 1.8.1 to convert from y parameters to S parameters gives

$$S_{11} = S_{22} = \frac{1}{D}\left[1 - \frac{g_m Z_o^2}{R_2(1 + g_m R_1)}\right] \tag{4.4.1}$$

$$S_{21} = \frac{1}{D}\left(\frac{-2g_m Z_o}{1 + g_m R_1} + \frac{2Z_o}{R_2}\right) \tag{4.4.2}$$

and

$$S_{12} = \frac{2Z_o}{DR_2} \tag{4.4.3}$$

where

$$D = 1 + \frac{2Z_o}{R_2} + \frac{g_m Z_o^2}{R_2(1 + g_m R_1)}$$

From (4.4.1) the conditions $S_{11} = S_{22} = 0$ (i.e., input and output VSWR = 1) are satisfied when

$$1 + g_m R_1 = \frac{g_m Z_o^2}{R_2}$$

or

$$R_1 = \frac{Z_o^2}{R_2} - \frac{1}{g_m} \tag{4.4.4}$$

Substituting (4.4.4) into (4.4.2) and (4.4.3) gives

$$S_{21} = \frac{Z_o - R_2}{Z_o} \tag{4.4.5}$$

and

$$S_{12} = \frac{Z_o}{R_2 + Z_o}$$

Equation (4.4.4) shows that $S_{11} = S_{22} = 0$ can be satisfied, with positive values of R_1, if the transconductance is large.

A range of values that satisfies $S_{11} = S_{22} = 0$ can be found. The minimum transconductance [called $g_{m(\min)}$] occurs when $R_1 = 0$ [i.e., $g_{m(\min)} = R_2/Z_o^2$] and it follows from (4.4.5) that

$$g_{m(\min)} = \frac{1 - S_{21}}{Z_o}$$

For example, if an amplifier has $|S_{21}|^2 = 10$ dB in a 50-Ω system, the minimum transconductance required is

$$g_{m(\min)} = \frac{1 - (-3.16)}{50} = 83 \text{ mS}$$

and the required shunt feedback resistor is

$$R_2 = 83 \times 10^{-3}(50)^2 = 208\ \Omega$$

Observe that (4.4.5) shows that

$$R_2 = Z_o(1 + |S_{21}|) \tag{4.4.6}$$

which is a well-known relation in feedback amplifiers.

When both R_1 and R_2 are used and g_m has a high value, (4.4.4) shows that the minimum input and output VSWR is obtained when $R_1 R_2 \approx Z_o^2$. The high value of g_m in a BJT makes them suitable for negative-feedback applications. However, most GaAs FETs have low values of g_m and one must be careful when using them in negative-feedback configurations. Equation (4.4.5) shows that S_{21} depends only on R_2 and not on the transistor parameters. Therefore, gain flattening can be achieved with negative feedback.

An important consideration in negative-feedback design is the phase of S_{21}. At low frequencies the phase of S_{21} is close to 180°, and as the frequency increases (above f_β) the phase of S_{21} varies rapidly. At some frequency the phase of S_{21} is such that a portion of the output voltage is in phase with the input voltage (i.e., positive feedback). This problem can be solved by decreasing the feedback when the phase shift of S_{21} approaches 90°. For example, in the case of shunt negative feedback (see Fig. 4.4.7), an inductor can be connected in series with R_2 such that after a certain frequency the negative feedback decreases in proportion to the S_{21} roll-off.

The previous analysis, although based on a simplified model, can be used in a preliminary design. Then CAD methods can be used to calculate the S parameters of the transistor with the feedback network connected, and to obtain the required Γ_s and Γ_l for optimum performance.

Example 4.4.2

Perform a preliminary analysis in the design of a BJT broadband amplifier having a transducer power gain of 10 dB from 10 to 1500 MHz. The S parameters of the transistor (in a 50-Ω system) at 10 V, 4 mA, the associated K factors, and $|S_{21}|^2$ in decibels (i.e., the transducer power gain in a 50-Ω system) are given in Fig. 4.4.10. (This example is based on a design from Ref. [4.10].)

F	S_{11}		S_{21}		S_{12}		S_{22}		$\lvert S_{21}\rvert^2$	
(MHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	(dB)	K
10	0.95	−2°	7.35	174.6°	0.003	84.3°	1.01	−1°	17.3	0.11
100	0.92	−11°	7.15	168.0°	0.007	79.0°	0.99	−4°	17.1	0.18
250	0.87	−28°	6.83	154.5°	0.015	69.2°	0.96	−10°	16.7	0.29
500	0.78	−54°	6.28	135.0°	0.026	54.0°	0.90	−18°	16.0	0.42
750	0.69	−78°	5.67	123.0°	0.033	41.4°	0.84	−25°	15.1	0.53
1000	0.63	−98°	5.04	113.0°	0.037	33.0°	0.79	−30°	14.1	0.67
1250	0.60	−114°	4.42	99.9°	0.038	29.3°	0.77	−33°	13.0	0.81
1500	0.60	−127°	3.88	87.0°	0.039	28.0°	0.76	−35°	11.8	0.91

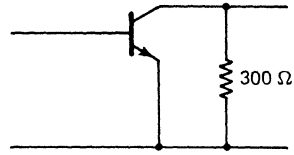
Figure 4.4.10 S parameters of the transistor, K factors, and $|S_{21}|^2$ in decibels.

Solution. The transistor is certainly capable of providing a transducer power gain of 10 dB. However, since $K < 1$, the transistor is potentially unstable and a stability analysis must be performed. Also, observe that above 1250 MHz the phase of S_{21} is less than 90°, and a portion of the output voltage is in phase with the input.

The input and output stability circles are given in Fig. 4.4.11. The analysis of the output stability circles show that a shunt resistor of 300 Ω at the output of the transistor provides stability. The resulting S parameters for the network shown in Fig. 4.4.12a are given in Fig. 4.4.12b. The stability of the network in Fig. 4.4.12a is much improved.

F	C_s			Stable	C_L			Stable
(MHz)	Mag.	Ang.	r_s	Region	Mag.	Ang.	r_L	Region
10	1.27	−43°	0.90	Inside	1.05	13°	0.24	Outside
100	30.53	88°	30.34	Outside	1.13	21°	0.37	Outside
250	4.61	89°	4.24	Outside	1.26	32°	0.54	Outside
500	3.61	103°	3.08	Outside	1.40	39°	0.64	Outside
750	2.63	117°	1.96	Outside	1.39	42°	0.58	Outside
1000	2.26	129°	1.46	Outside	1.41	44°	0.53	Outside
1250	2.14	140°	1.24	Outside	1.40	44°	0.46	Outside
1500	1.99	150°	1.04	Outside	1.39	45°	0.42	Outside

Figure 4.4.11 Stability circles locations



(a)

F	S_{11}		S_{21}		S_{12}		S_{22}		$\lvert S_{21}\rvert^2$		
(MHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	(dB)	K	$\lvert\Delta\rvert$
10	0.95	−2°	6.30	174.7°	0.003	84.4°	0.72	−1°	15.98	1.4	0.69
100	0.92	−11°	6.13	168.3°	0.006	79.3°	0.71	−4°	15.75	1.1	0.66
250	0.87	−28°	5.88	155.2°	0.013	69.9°	0.69	−10°	15.38	0.94	0.61
500	0.79	−53°	5.44	136.1°	0.023	55.1°	0.65	−19°	14.71	1.0	0.54
750	0.70	−77°	4.94	124.5°	0.029	42.9°	0.61	−26°	13.88	1.2	0.45
1000	0.64	−97°	4.42	114.7°	0.032	34.7°	0.57	−32°	12.90	1.4	0.37
1250	0.61	−113°	3.89	101.7°	0.033	31.1°	0.56	−35°	11.79	1.6	0.34
1500	0.60	−126°	3.42	88.8°	0.034	29.8°	0.55	−38°	10.67	1.9	0.33

(b)

Figure 4.4.12 (a) Stabilized transistor network; (b) the resulting S parameters.

The gain $|S_{21}|^2$ is reduced because the 300-Ω resistor dissipates some of the output power. Still, the network in Fig. 4.2.12a can easily provide the transducer power gain of 10 dB. The S_{11} and S_{22} parameters are large, showing that the input and output VSWR are poor. The phase of S_{21} above 1250 MHz remains less than 90°.

The shunt negative-feedback resistor–inductor combination, shown in Fig. 4.4.13, can now be designed to provide a flat gain of 10 dB (i.e., $|S_{21}|^2 = 10$ dB or $|S_{21}| = 3.16$) with 50-Ω input and output impedances. The value of R_2 is calculated using (4.4.6), namely

$$R_2 = 50(1 + 3.16) = 208\ \Omega$$

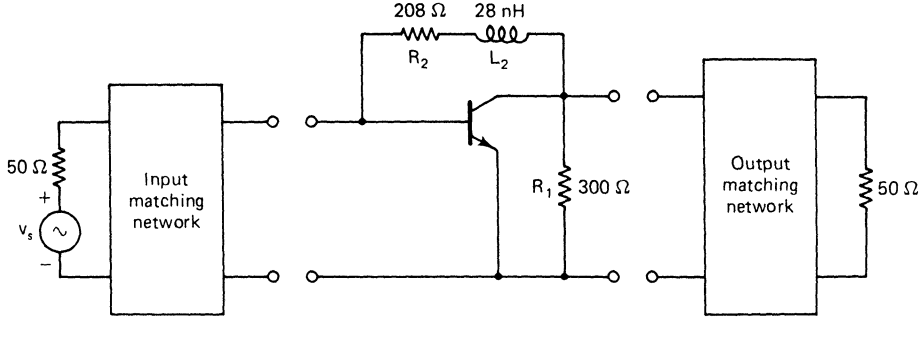


Figure 4.4.13 The feedback network and the matching networks

The value of L_2 is designed to provide negative feedback above 1200 MHz (i.e., to decrease the gain, so that the phase of S_{21} in the feedback network remains above 90°). That is, the value of L_2 is selected from

$$R_2 = \omega L_2|_{f=1200\text{ MHz}} \quad \text{or} \quad L_2 = \frac{208}{2\pi(1200 \times 10^6)} = 28 \text{ nH}$$

The resulting S parameters of the feedback network in Fig. 4.4.13 are given in Fig. 4.4.14. We can observe from Fig. 4.4.14a that negative feedback has reduced S_{11} and S_{22} considerably. The input VSWR is less than 2, except at 1500 MHz. Also, the gain $|S_{21}|^2$ in decibels in a 50-Ω system is close to the designed value of 10 dB over the frequency band.

In order to improve the input and output VSWR, and to flatten the gain, the feedback network elements (i.e., R_2 and L_2) can be varied using trial and error. Obviously, the number of calculations required are considerable and CAD methods are necessary.

This example is revisited in Appendix A, where CAD methods are used to optimize the feedback network design. In fact, it is shown that using $R_2 = 274.8\ \Omega$ and $L_2 = 12.9$ nH results in the S parameters given in Fig. 4.4.14b. From Fig. 4.4.14b it is observed that the gain flatness is improved.

F	S_{11}		S_{21}		S_{12}		S_{22}		$\lvert S_{21}\rvert^2$		
(MHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	(dB)	K	$\lvert\Delta\rvert$
10	0.08	17°	2.68	176.7°	0.184	1.0°	0.04	140°	8.58	1.25	0.50
100	0.07	17°	2.67	175.5°	0.182	−2.9°	0.07	113°	8.53	1.26	0.48
250	0.08	11°	2.73	171.5°	0.180	−9.6°	0.14	93°	8.74	1.23	0.48
500	0.10	−5°	3.03	163.7°	0.172	−20.4°	0.26	77°	9.62	1.14	0.51
750	0.12	−46°	3.37	156.6°	0.154	−32.6°	0.35	62°	10.56	1.11	0.53
1000	0.18	−77°	3.65	146.3°	0.133	−43.6°	0.44	45°	11.25	1.10	0.54
1250	0.28	−93°	3.79	128.9°	0.112	−54.4°	0.56	26°	11.58	1.08	0.56
1500	0.39	−109°	3.70	109.5°	0.087	−64.1°	0.65	8°	11.35	1.12	0.55

F	S_{11}		S_{21}		S_{12}		S_{22}		$\lvert S_{21}\rvert^2$		
(MHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	(dB)	K	$\lvert\Delta\rvert$
10.00	0.18	5°	3.14	176.3°	0.161	1.0°	0.07	20°	9.95	1.22	0.52
100.00	0.18	−4°	3.11	173.0°	0.159	−1.9°	0.08	32°	9.86	1.23	0.51
250.00	0.17	−22°	3.10	165.5°	0.156	−6.8°	0.11	45°	9.83	1.25	0.50
500.00	0.18	−52°	3.17	153.7°	0.148	−14.0°	0.17	49°	10.01	1.26	0.49
750.00	0.21	−87°	3.20	145.8°	0.134	−21.2°	0.21	44°	10.11	1.33	0.47
1000.00	0.25	−110°	3.19	137.4°	0.120	−26.6°	0.25	36°	10.06	1.40	0.44
1250.00	0.30	−120°	3.14	124.2°	0.109	−31.2°	0.34	25°	9.95	1.45	0.44
1500.00	0.36	−128°	3.06	109.5°	0.098	−35.7°	0.43	15°	9.72	1.49	0.45

Figure 4.4.14 (a) S parameters of the feedback network with $R_2 = 208\ \Omega$ and $L_2 = 28$ nH; (b) S parameters of the feedback network with $R_2 = 274.8\ \Omega$ and $L_2 = 12.9$ nH.

Further performance improvements can be obtained with the addition of input and output matching networks, and using CAD methods to optimize the overall design for a flat transducer power gain of 10 dB with good input and output VSWR. The optimization and final design are discussed in Appendix A.

A matching network produces the desired match at one frequency and matching degradation occurs at the other frequencies. Fano [4.11] has derived a complete set of integrals that predict the gain–bandwidth restrictions for lossless matching networks terminated in an arbitrary load impedance. The derivations of the results are covered in Fano's paper and only the appropriate results will be given. For the network shown in Fig. 4.4.15a, the best Γ that can be achieved over a frequency range is restricted by the integral

$$\int_0^\infty \ln \left| \frac{1}{\Gamma} \right| d\omega \leq \frac{\pi}{RC} \tag{4.4.7}$$

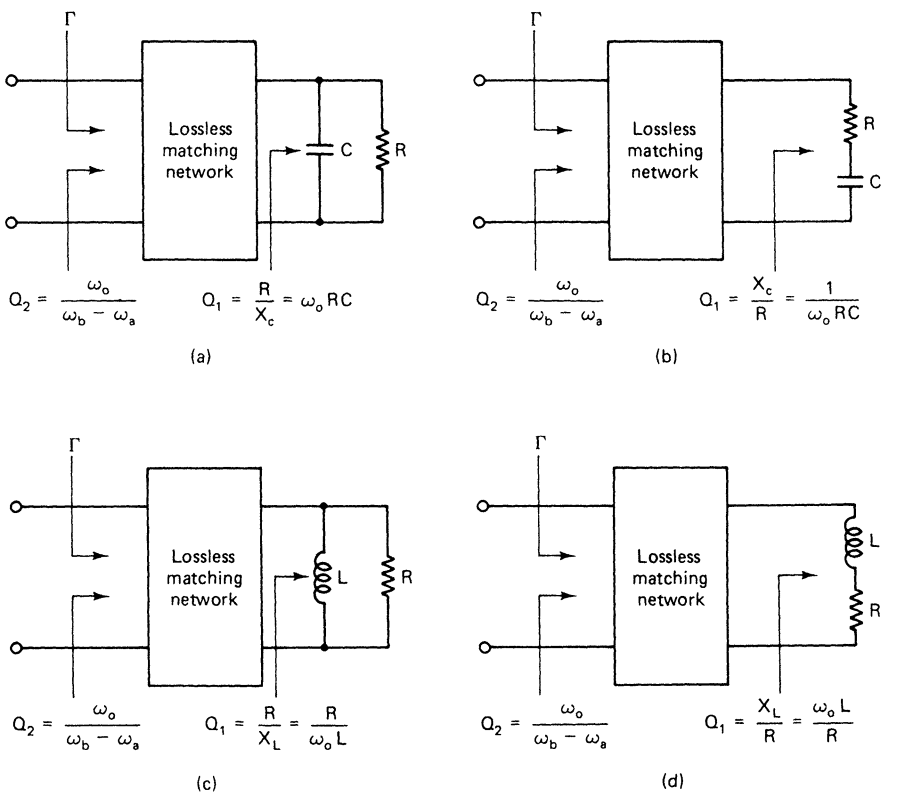


Figure 4.4.15 Network topologies used in the calculations of the gain–bandwidth limitations.

Equation (4.4.7) expresses the fact that the area under the curve $\ln|1/\Gamma|$ cannot be greater than π/RC. Therefore, if matching is required over a certain bandwidth, it can be obtained at the expense of less power transfer.

The best utilization of the area under the curve $\ln|1/\Gamma|$ is obtained when $|\Gamma|$ is constant over the frequency range ω_a to ω_b and equal to 1 outside that range. This situation is illustrated in Fig. 4.4.16, and it follows from (4.4.7) that

$$|\Gamma| = \Gamma_x = e^{-\pi/(\omega_b - \omega_a)RC}$$

or

$$\Gamma_x = e^{-\pi(Q_2/Q_1)} \tag{4.4.8}$$

where

$$Q_1 = \frac{R}{X_c}$$

and

$$Q_2 = \frac{\omega_o}{\omega_b - \omega_a}$$

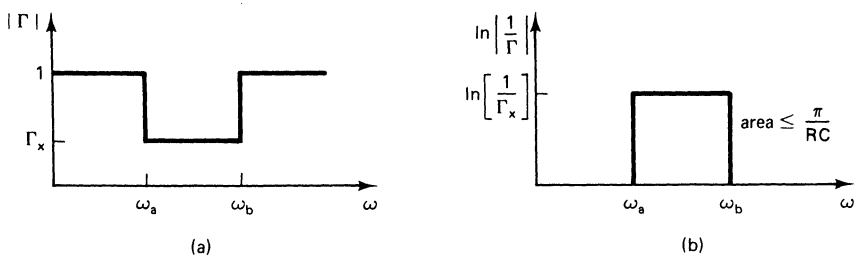


Figure 4.4.16 Optimum values of $|\Gamma|$.

Equation (4.4.8) gives the best ideally achievable Γ_x that can be obtained in the band ω_a to ω_b with no power transfer outside the band. Although a matching network satisfying the requirements above cannot be obtained in practice, the relation (4.4.8) can be used as a guideline for the best Γ_x.

The expression (4.4.8) can also be used for the networks shown in Figs. 4.4.15b to 4.4.15d when the appropriate definition of Q_1 and Q_2 are used. These are given in the figures.

Example 4.4.3

Over the frequency range $f_a = 500$ MHz to $f_b = 900$ MHz, find the best Γ_x that can be achieved in the network shown in Fig. 4.4.17.

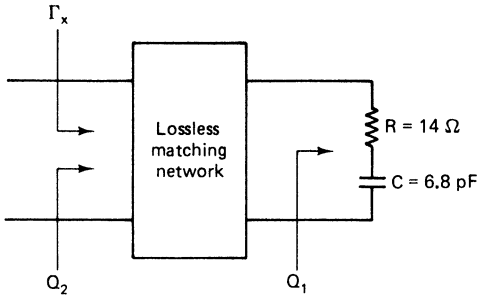


Figure 4.4.17 Calculation of Γ_x.

Solution. At $f_o = 700$ MHz we obtain

$$Q_1 = \frac{1}{\omega_o RC} = \frac{1}{2\pi(700 \times 10^6)14(6.8 \times 10^{-12})} = 2.39$$

and

$$Q_2 = \tfrac{7}{4} = 1.75$$

Then, from (4.4.8), the value of Γ_x is

$$\Gamma_x = e^{-\pi(1.75/2.39)} = 0.1$$

The normalized load impedance of the network in Fig. 4.4.17 (i.e., $z = 0.28 - j468 \times 10^6/f$) is plotted in Fig. 4.4.18 over the frequency range f_a to f_b. Also, the region $\Gamma_x < 0.1$ for the ideally achievable match is shown shaded.

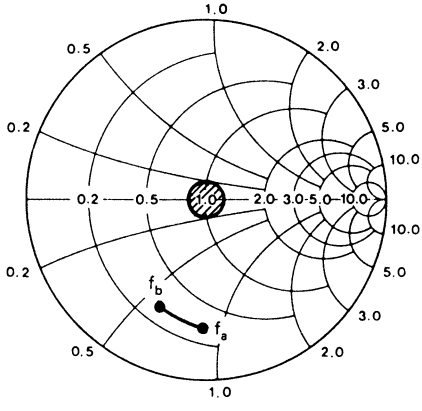


Figure 4.4.18 Best achievable match Γ_x.

4.5 AMPLIFIER TUNING

The input reflection coefficient in the bilateral case is a function of the output reflection coefficient, and vice versa. Therefore, Γ_{IN} varies with output tuning and Γ_{OUT} varies with input tuning.

After an amplifier is built, tuning or alignment is necessary in order for the amplifier to provide optimum performance. The tuning is usually done by performing minor changes and adjusting the components of the matching networks.

An amplifier is easy to tune when the ratios of the fractional changes in Γ_{IN} due to Γ_L, and Γ_{OUT} due to Γ_s, are small.

The input reflection tuning factor δ_{IN} is defined as

$$\delta_{IN} = \left| \frac{d\Gamma_{IN}/\Gamma_{IN}}{d\Gamma_L/\Gamma_L} \right|$$

which in terms of the two-port network S parameters can be written as

$$\delta_{IN} = \frac{|S_{21}|\,|S_{12}|\,|\Gamma_L|}{|1 - S_{22}\Gamma_L|\,|S_{11} - \Delta\Gamma_L|} \tag{4.5.1}$$

In practice, a value of $\delta_{IN} < 0.3$ produces good tunability. Equation (4.5.1) shows that δ_{IN} can be zero under some circumstances. That is, $\delta_{IN} = 0$ when $S_{12} = 0$, which occurs when the unilateral assumption can be made. In this case, the output tuning does not affect the input. Also, $\delta_{IN} = 0$ when $\Gamma_L = 0$, which is a very specific value of Γ_L that probably degrades the gain and noise performance of the amplifier. Of course, $\delta_{IN} = 0$ when $S_{21} = 0$, that is, when there is no power gain. The derivation for the output tunability factor δ_{OUT} is left as an exercise.

Equation (4.5.1) can be solved for Γ_L in terms of δ_{IN}, namely

$$|\Gamma_L| = \left| \alpha \pm \left| \alpha^2 - \frac{S_{11}}{S_{22}\Delta} \right|^{1/2} \right| \tag{4.5.2}$$

where

$$\alpha = \frac{\Delta + S_{11}S_{22} + S_{12}S_{21}\delta_{IN}^{-1}}{2S_{22}\Delta} \tag{4.5.3}$$

The value of $|\Gamma_L|$ obtained from (4.5.2) and (4.5.3) for a given δ_{IN} is, in general, different from the value that produces maximum power gain or optimum noise performance. Therefore, this value of Γ_L produces good tunability but mismatches the amplifier.

4.6 BANDWIDTH ANALYSIS

The conditions for a conjugate match at the input and output ports are satisfied at one frequency. One reason the output power varies with frequency is the frequency dependence of the matching networks. However, the most important factor that limits the frequency response is the variations of the transistor S parameters with frequency.

The input port, under conjugate matched conditions, is shown in Fig. 4.6.1a. A conjugate match means that $\Gamma_s = \Gamma_{IN}^*$ or $Y_s = Y_{IN}^*$. With

$$Y_{IN} = G_{s,M} + jB_{s,M}$$

and

$$Y_s = G_{s,M} - jB_{s,M}$$

the network in Fig. 4.6.1a can be represented by the *RLC* network shown in Fig. 4.6.1b. The values $G_{s,M}$ and $B_{s,M}$ represent the conductance and susceptance obtained under conjugate match conditions.

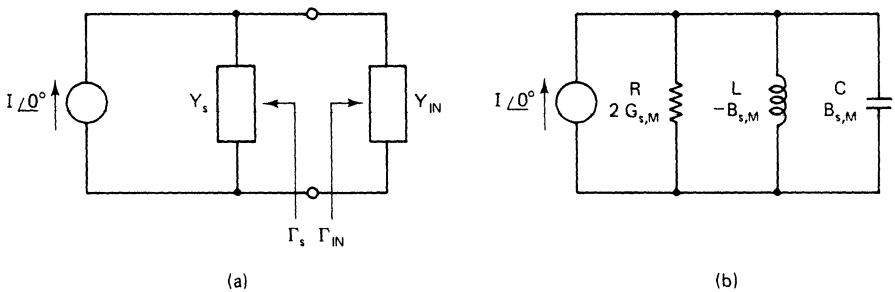


Figure 4.6.1 Equivalent networks of the input port under conjugate match conditions.

The input inherent bandwidth, $(BW)_{IN}^i$, is the bandwidth obtained under conjugate matched conditions where the matched terminations are determined by the *S* parameters of the two-port device. The input inherent bandwidth is given by

$$(BW)_{IN}^i = \frac{f_o}{Q_{IN}} \quad \text{Hz} \tag{4.6.1}$$

where f_o is the frequency at which the conjugate matched values were obtained and Q_{IN} is the "que" of the equivalent input network. The value of Q_{IN}, for the network in Fig. 4.6.1b, can be expressed in different forms, namely

$$Q_{IN} = \omega_o RC = \frac{R}{\omega_o L} \tag{4.6.2}$$

where $\omega_o = 2\pi f_o = 1/\sqrt{LC}$. Substituting (4.6.2) into (4.6.1), we obtain

$$(BW)_{IN}^i = \frac{2f_o G_{s,M}}{|B_{s,M}|} \tag{4.6.3}$$

where $R = 1/2G_{s,M}$ and $|B_{s,M}| = \omega_o C = 1/\omega_o L$. Similarly, the output inherent bandwidth is given by

$$(\text{BW})^i_{\text{OUT}} = \frac{2f_o G_{s,M}}{|B_{L,M}|} \tag{4.6.4}$$

where $Y_L = Y^*_{\text{OUT}}$.

Example 4.6.1

In the microwave transistor amplifier of Example 3.7.1 we found that for a simultaneous conjugate match at $f = 6$ GHz, $\Gamma_{Ms} = 0.762\underline{|177.3°}$, and $\Gamma_{ML} = 0.718\underline{|103.9°}$. Calculate the amplifier bandwidth limitation due to the matching networks.

Solution. The admittances $Y_{\text{IN}} = Y_s^*$ and $Y_{\text{OUT}} = Y_L^*$ associated with Γ_{Ms} and Γ_{ML} are

$$Y_{\text{IN}} = (144 + j24.6) \times 10^{-3}\ S$$

and

$$Y_{\text{OUT}} = (8.28 + j23.8) \times 10^{-3}\ S$$

The equivalent network at the input port is illustrated in Fig. 4.6.1. The equivalent network for the output port is similar. From Y_{IN} and Y_{OUT}, it follows that $G_{s,M} = 144 \times 10^{-3}$, $B_{s,M} = 24.6 \times 10^{-3}$, $G_{L,M} = 8.28 \times 10^{-3}$, and $B_{L,M} = 23.8 \times 10^{-3}$. Therefore, from (4.6.3) and (4.6.4),

$$(\text{BW})^i_{\text{IN}} = \frac{2(6 \times 10^9)144 \times 10^{-3}}{24.6 \times 10^{-3}} = 70.2 \text{ GHz}$$

and

$$(\text{BW})^i_{\text{OUT}} = \frac{2(6 \times 10^9)8.28 \times 10^{-3}}{23.8 \times 10^{-3}} = 4.17 \text{ GHz}$$

Since $(\text{BW})^i_{\text{IN}} \gg (\text{BW})^i_{\text{OUT}}$, the bandwidth limitations due to the matching networks are determined by $(\text{BW})^i_{\text{OUT}}$.

The broad bandwidth $(\text{BW})^i_{\text{OUT}}$ cannot be obtained in practice because of the transistor S-parameter variations with frequency. In fact, the overall bandwidth of the amplifier, as shown in Fig. 4.3.11d, is 980 MHz.

The inherent bandwidth of either the input or output port can be decreased by increasing the Q of the network. From (4.6.2), we can increase Q by increasing the capacitance or decreasing the inductance of the network. When Y_{IN} has a capacitive susceptance, the bandwidth is decreased by adding capacitance, and when Y_{IN} has an inductive susceptance, the bandwidth is decreased by adding inductance.

Consider the case where Y_{IN} has a capacitive susceptance. The admittance Y_{IN} is given by

$$Y_{\text{IN}} = G_{\text{IN},M} + jB_{\text{IN},M}$$

where $R = 1/2G_{s,M}$ and $|B_{s,M}| = \omega_o C = 1/\omega_o L$. Similarly, the output inherent bandwidth is given by

$$(\mathrm{BW})^i_{\mathrm{OUT}} = \frac{2f_o G_{s,M}}{|B_{L,M}|} \tag{4.6.4}$$

where $Y_L = Y^*_{\mathrm{OUT}}$.

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Consider the case where Y_{IN} has a capacitive susceptance. The admittance Y_{IN} is given by

$$Y_{\mathrm{IN}} = G_{\mathrm{IN},M} + jB_{\mathrm{IN},M}$$

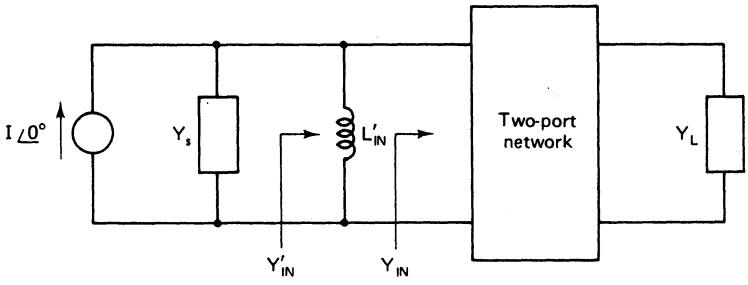


Figure 4.6.3 Increasing Q by adding the inductance L'_{IN}.

In the output port, the value of inductance required to obtain $(BW)_{OUT}$ is

$$L'_{OUT} = \frac{1}{\omega_o |B_{OUT,M}| \left[\frac{(BW)'_{OUT}}{(BW)_{OUT}} - 1\right]}$$

The previous methods of adding capacitance or inductance to narrowband the amplifier response does not affect the original simultaneous conjugate matched calculations.

The overall bandwidth of n identical single tuned networks is related to the bandwidth of one stage, $(BW)_1$, by the relation

$$(BW)_n = (BW)_1\sqrt{2^{1/n} - 1} \tag{4.6.6}$$

The factor

$$\sqrt{2^{1/n} - 1}$$

is called the *bandwidth reduction factor*. In the case of two single tuned networks (i.e., $n = 2$), (4.6.6) gives

$$(BW)_2 = (BW)_1(0.644)$$

4.7 HIGH-POWER AMPLIFIER DESIGN

Thus far we have presented design techniques, based on the small-signal S parameters of transistors, for maximum or arbitrary power gain, low noise, and broadband amplifiers. The small-signal S parameters are not useful for power amplifier design because power amplifiers usually operate in nonlinear regions. The small-signal S parameters can be used in large-signal amplifiers operating in class A (i.e., linear output power). However, for class AB, B, or C the small-signal S parameters are not suitable for design purposes.

A set of large-signal S parameters is needed to characterize the transistor for power applications. Unfortunately, the measurement of large-signal S parameters is difficult and is not properly defined. Therefore, an alternative set of

large-signal parameters is needed to characterize the transistor. This can be done by providing information of source and load reflection coefficients as a function of output power and gain, especially the measurement of the source and load reflection coefficients, together with the output power, when the transistor is operated at its 1-dB gain compression point. The listing of the 1-dB compression point data is used to specify the power-handling capabilities of the transistor.

The 1-dB gain compression point (called $G_{1\,dB}$) is defined as the power gain where the nonlinearities of the transistor reduces the power gain by 1 dB over the small-signal linear power gain. That is,

$$G_{1\,dB}(dB) = G_o(dB) - 1 \tag{4.7.1}$$

where $G_o(dB)$ is the small-signal linear power gain in decibels. Since the power gain is defined as

$$G_p = \frac{P_{OUT}}{P_{IN}}$$

or

$$P_{OUT}(dBm) = G_p(dB) + P_{IN}(dBm)$$

we can write the output power at the 1-dB gain compression point, called $P_{1\,dB}$, as

$$P_{1\,dB}(dBm) = G_{1\,dB}(dB) + P_{IN}(dBm) \tag{4.7.2}$$

Substituting (4.7.1) into (4.7.2) gives

$$P_{1\,dB}(dBm) - P_{IN}(dBm) = G_o(dB) - 1 \tag{4.7.3}$$

Equation (4.7.3) shows that the 1-dB gain compression point is that point at which the output power minus the input power in dBm is equal to the small-signal power gain minus 1 dB.

A typical plot of P_{OUT} versus P_{IN} which illustrates the 1-dB gain compression point is shown in Fig. 4.7.1. Observe the linear output power characteristics for power levels between the minimum detectable signal output power ($P_{o,mds}$) and $P_{1\,dB}$. The dynamic range (DR), shown in Fig. 4.7.1, is that range where the amplifier has a linear power gain. The dynamic range is limited at low power levels by the noise level. An input signal ($P_{i,mds}$) is detectable only if its output power level ($P_{o,mds}$) is above the noise power level.

The thermal noise power level of a two-port, with noise figure F, is given by

$$P_{N_o} = kTBG_A F$$

Observing that $kT = -174$ dBm (or $kTB = -114$ dBm/MHz at $T = 290°K$) and assuming that the minimum detectable input signal is X decibels above

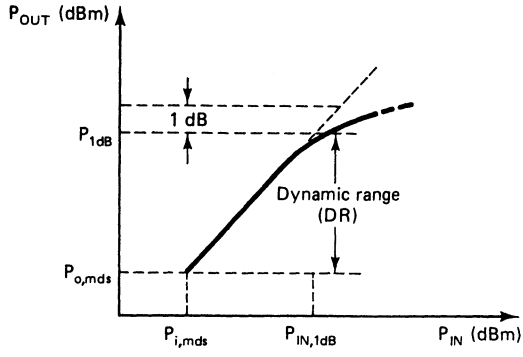


Figure 4.7.1 The 1-dB gain compression point and the dynamic range of microwave amplifiers.

thermal noise, we can write

$$P_{i,\text{mds}} = -174 \text{ dBm} + 10 \log B + F(\text{dB}) + X(\text{dB}) \tag{4.7.4}$$

and

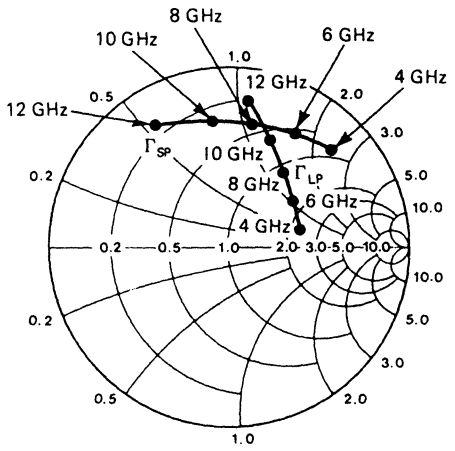
$$P_{o,\text{mds}} = -174 \text{ dBm} + 10 \log B + F(\text{dB}) + X(\text{dB}) + G_A(\text{dB}) \tag{4.7.5}$$

A typical value of X(dB) is 3 dB.

As previously discussed, a power transistor can be described in terms of the large-signal source and load reflection coefficients required to produce a given output power and gain. Of course, these parameters are functions of frequency and bias conditions. For example, in a GaAs FET the 1-dB gain compression point is usually measured at a drain-to-source voltage and gate-to-source voltage that optimizes the output power. From Fig. 3.9.7, this is usually at $I_{DS} = 50\% I_{DSS}$.

A typical set of power reflection coefficients is shown in Fig. 4.7.2a. The values of Γ_{SP} and Γ_{LP} denoted by points are the source and load power reflection coefficients for maximum output power. The values of Γ_{SP} and Γ_{LP} are given for $f = 4$ GHz to $f = 12$ GHz. Figure 4.7.2b illustrates typical output power contours as a function of the load reflection coefficient. For this transistor $P_{1\text{dB}} = 19$ dBm and $G_{1\text{dB}} = 6$ dB. The 18-dBm and 17-dBm output power contours are also shown. The input was conjugately matched at all times.

A typical measuring system for large-signal parameters is illustrated in Fig. 4.7.3. The transistor under test is placed in a measuring setup where the dc bias and ac input signal level can be varied. The output tuning stubs are adjusted until the power meter C measures a given power level and the input tuning stubs are adjusted for zero reflected power (read at power meter B). The power meter A reads the incident power, and the power gain (at given output power level) can be obtained. Since there is no reflected power, the input port is conjugately matched, and the output impedance is that impedance required to produce the output power read at power meter C.



f (GHz)	Output power P_{1dB}	G_p
4	19 dBm	13 dB
6	18 dBm	12 dB
8	18 dBm	10 dB
10	17 dBm	8 dB
12	16 dBm	6 dB

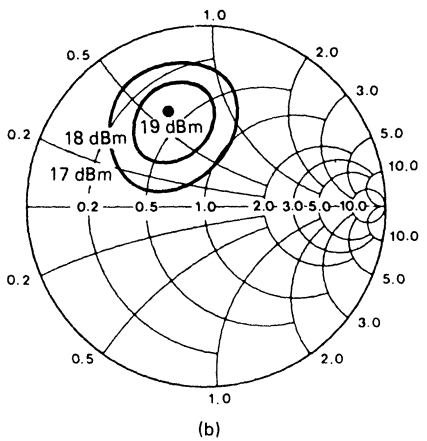


Figure 4.7.2 (a) Typical large-signal reflection coefficients. (b) Typical output power contours as a function of Γ_{LP} for a GaAs FET at $f = 10$ GHz, $V_{DS} = 10$ V, and $I_D = 50\% I_{DSS}$. For this transistor the optimum output power is 19 dBm at 1-dB gain compression and $G_{1dB} = 6$ dB.

The transistor can then be disconnected from the test setup and the impedance at the reference planes A and B is measured with a network analyzer. These measurements produce the values of Γ_{SP} and Γ_{LP} for a given output power and gain. Of course, Γ_{SP} and Γ_{LP} are functions of output power level, frequency, and bias conditions.

A source of distortion in power amplifiers is that caused by intermodulation products. When two or more sinusoidal frequencies are applied to a

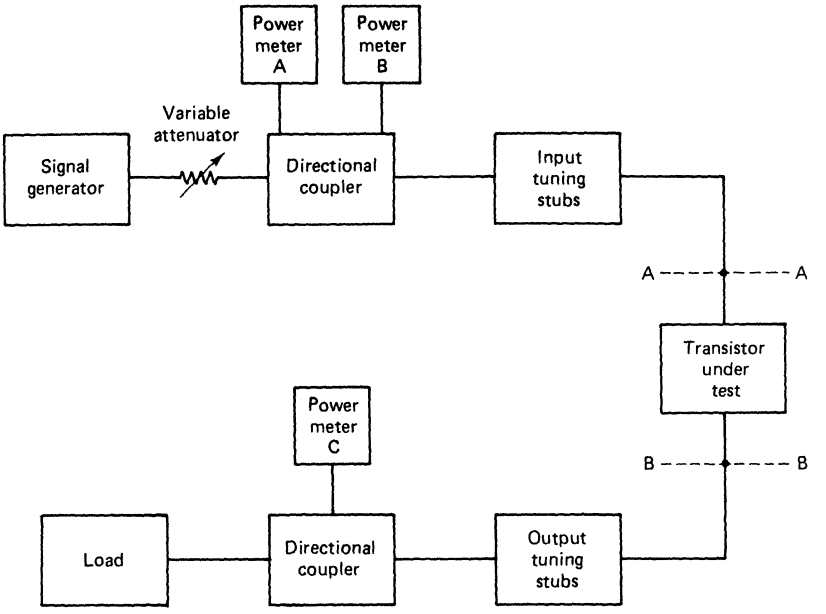


Figure 4.7.3 Measuring system for large-signal parameters.

called *intermodulation products*. For example, if two sinusoidal signals

$$v(t) = A \cos 2\pi f_1 t + A \cos 2\pi f_2 t \tag{4.7.6}$$

are applied to a nonlinear amplifier whose output voltage can be represented by the power series

$$v_o(t) = \alpha_1 v(t) + \alpha_2 v^2(t) + \alpha_3 v^3(t) \tag{4.7.7}$$

the output signal will contain frequency components at dc, $f_1, f_2, 2f_1, 2f_2, 3f_1, 3f_2, f_1 \pm f_2, 2f_1 \pm f_2$, and $2f_2 \pm f_1$. The frequencies $2f_1$ and $2f_2$ are the second harmonics, $3f_1$ and $3f_2$ are the third harmonics, $f_1 \pm f_2$ are the second-order intermodulation products (since the sum of the f_1 and f_2 coefficients is 2), and $2f_1 \pm f_2$ and $2f_2 \pm f_1$ are the third-order intermodulation products (since the sum of the f_1 and f_2 coefficients is 3). The input and output power spectra, from (4.7.6) and (4.7.7), are shown in Fig. 4.7.4.

Figure 4.7.4 shows that the third-order intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$ are very close to the fundamental frequencies f_1 and f_2 and fall within the amplifier bandwidth, producing distortion in the output.

If we measure the third-order intermodulation product output power ($P_{2f_1-f_2}$) versus the input power at f_1 (P_{f_1}), the graph shown in Fig. 4.7.5 results. The third-order intercept point (called P_{IP}) is defined as the point where P_{f_1} and $P_{2f_1-f_2}$ intercept, when the two-port is assumed to be linear. Observe that the slope of P_{f_1} is 1 and that of $P_{2f_1-f_2}$ is 3. This occurs because

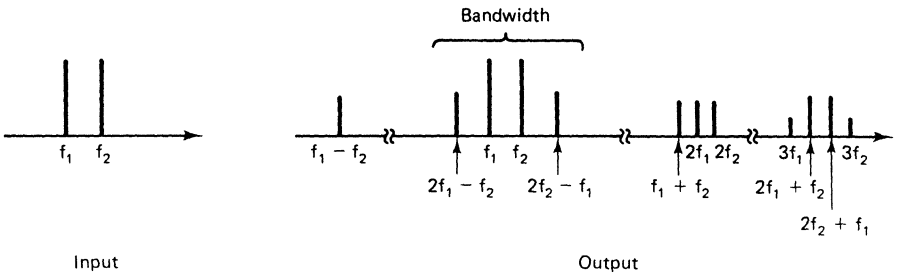


Figure 4.7.4 Input and output power spectrum.

for the assumed $v_o(t)$ in (4.7.7) the power of the third-order intermodulation product is proportional to the cube of the input signal amplitude A. The power P_{IP} is a theoretical level. However, it is a useful quantity to estimate the third-order intermodulation products at different power levels.

For the three-term series in (4.7.7), it can be shown analytically and experimentally that the third-order intercept point is approximately 10 dB above the 1-dB gain compression point. That is,

$$P_{IP}(\text{dBm}) = P_{1\,\text{dB}}(\text{dBm}) + 10\ \text{dB} \tag{4.7.8}$$

Also, it can be shown that

$$2P_{2f_1-f_2} = 3P_{f_1} - 2P_{IP}$$

or

$$P_{f_1} - P_{2f_1-f_2} = \tfrac{2}{3}(P_{IP} - P_{2f_1-f_2}) \tag{4.7.9}$$

The spurious free dynamic range (DR_f) of an amplifier (see Fig. 4.7.5) is defined as the range $P_{f_1} - P_{2f_1-f_2}$, when $P_{2f_1-f_2}$ is equal to the minimum detectable output signal. Therefore, from (4.7.5) and (4.7.9),

$$\begin{aligned}\text{DR}_f &= \tfrac{2}{3}(P_{IP} - P_{o,\text{mds}}) \\ &= \tfrac{2}{3}[P_{IP} + 174\ \text{dBm} - 10\log B - F(\text{dB}) - X(\text{dB}) - G_A(\text{dB})]\end{aligned}$$

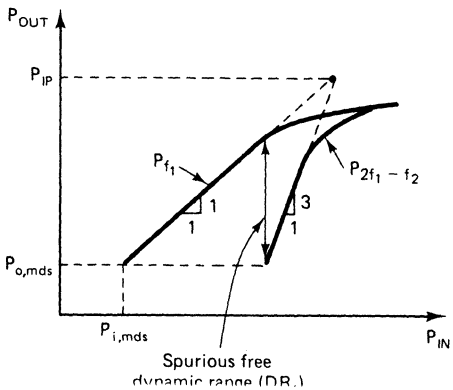


Figure 4.7.5 Third-order intercept point.

Example 4.7.1

An amplifier has an available power gain of 40 dB, 500-MHz bandwidth, noise figure of 7 dB, and a 1-dB gain compression point of 25 dBm. Calculate DR and DR_f.

Solution. The minimum detectable input and output signals, from (4.7.4) and (4.7.5), assuming that $X = 3$ dB, are

$$P_{i,\text{mds}} = -174 \text{ dBm} + 10 \log (500 \times 10^6) \text{ dB} + 7 \text{ dB} + 3 \text{ dB} = -77 \text{ dBm}$$

and

$$P_{o,\text{mds}} = -77 \text{ dBm} + 40 \text{ dB} = -37 \text{ dBm}$$

Therefore,

$$\text{DR} = P_{1\text{dB}} - P_{o,\text{mds}} = 25 \text{ dBm} + 37 \text{ dBm} = 62 \text{ dB}$$

The third-order intercept point, from (4.7.8), is

$$P_{IP} = 25 \text{ dBm} + 10 \text{ dB} = 35 \text{ dBm}$$

and

$$\text{DR}_f = \tfrac{2}{3}(25 \text{ dBm} + 37 \text{ dBm}) = 48 \text{ dB}$$

Another source of signal distortion is caused by a nonlinear phase characteristic. For a signal to be amplified with no distortion, the magnitude of the power gain transfer function must be constant as a function of frequency and the phase must be a linear function of frequency. A linear phase shift produces a constant time delay to signal frequencies, and a nonlinear phase shift produces different time delays to different frequencies.

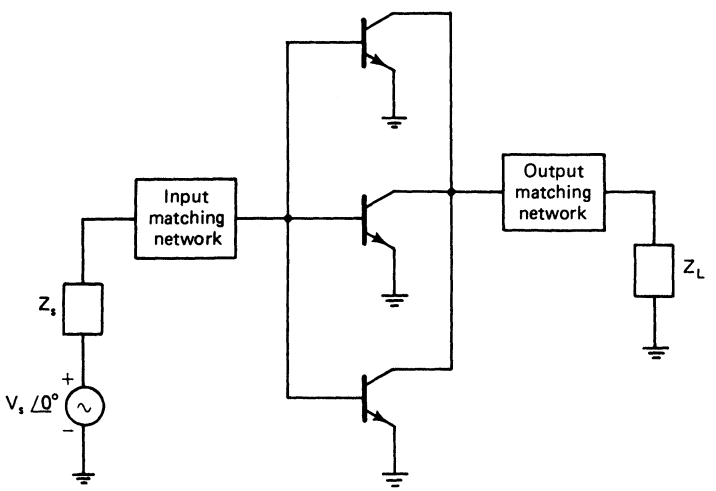


Figure 4.7.6 Method for paralleling transistors

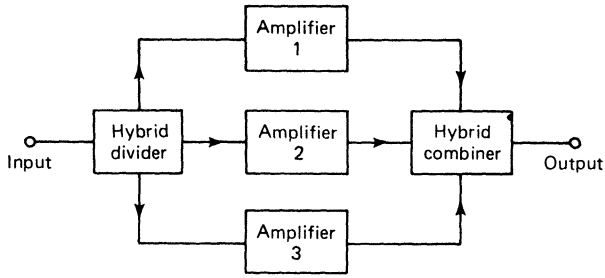


Figure 4.7.7 A hybrid combiner/divider.

A phase distortion called *AM-to-PM conversion* occurs when an AM signal is transmitted through a power amplifier. The phase shift becomes a function of the instantaneous amplitude of the signal, and the output phase consists of a mean value with a small ripple. The AM-to-PM conversion is defined as the change in output phase for a 1-dB increment of the input power.

Power transistors are provided with flanges or studs for proper mounting and heat dissipation. The maximum junction temperature for a BJT is around 200°C and the maximum channel temperature for a GaAs FET is around 175°C.

When more power is required than can be provided by a single microwave transistor amplifier, power-combining techniques are used. One can use a method of paralleling several transistors, as shown in Fig. 4.7.6. However, this method is not recommended, for several reasons:

1. The input and output impedance levels can be of the same order as the losses in the input and output matching networks. For example, a 0.1-nH inductor having a Q of 150, at $f = 400$ MHz, has a resistance loss of $R = \omega L/Q = 1.6\ \Omega$, which can be similar to the input resistance of sev-

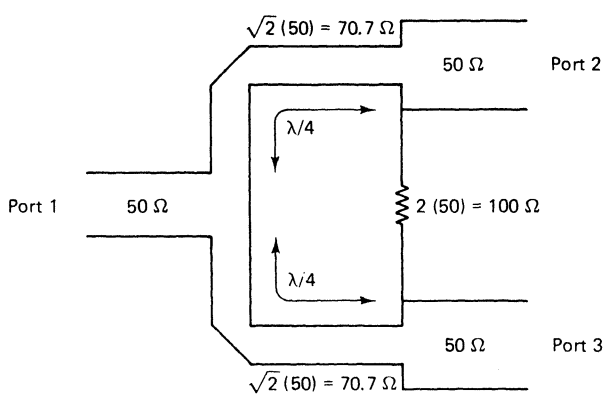


Figure 4.7.8 The Wilkinson coupler.

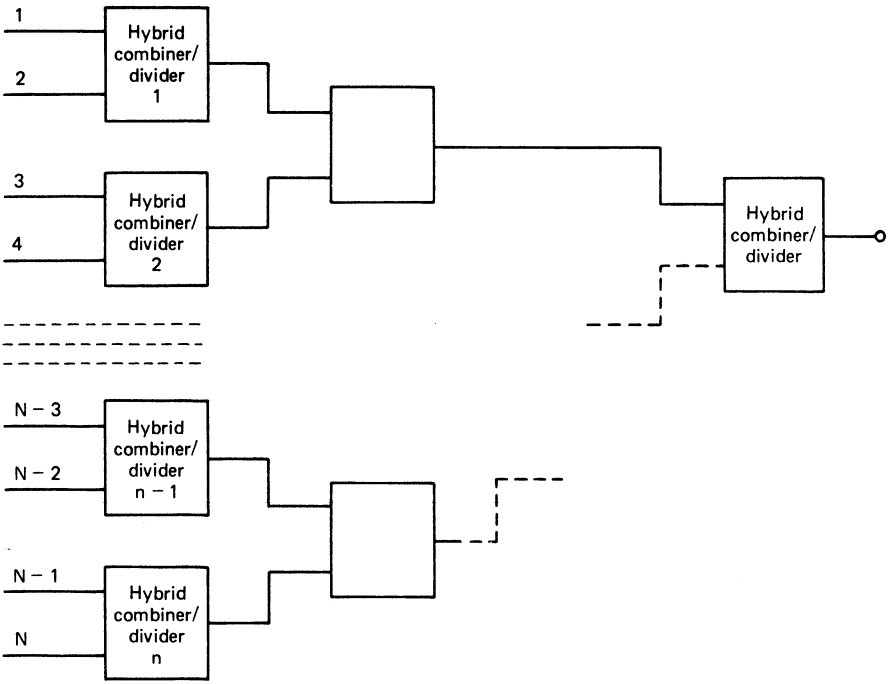


Figure 4.7.9 An n-way hybrid combiner/divider.

eral paralleled transistors. Therefore, the total power output that can be obtained from several paralleled transistors is less than the theoretical total output power because the efficiency decreases as the number of transistors increases.

2. If one transistor fails, the complete amplifier network fails.

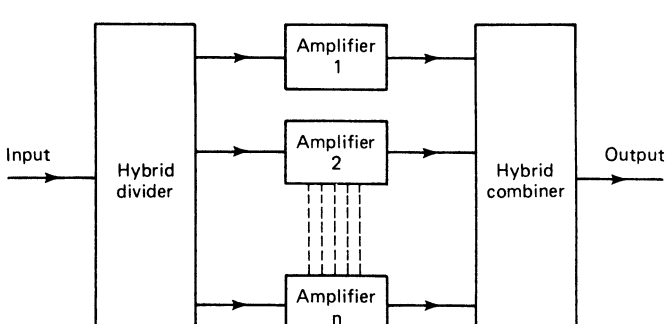


Figure 4.7.10 An n-way power amplifier.

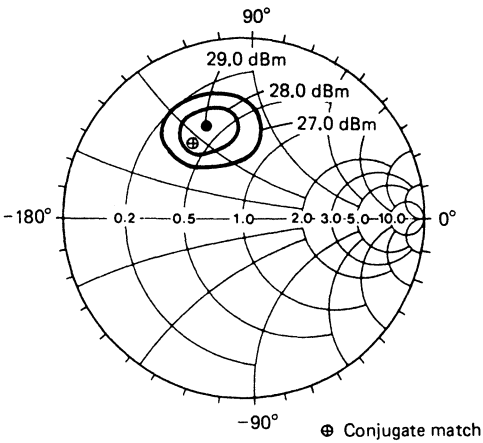


Figure 4.7.11 Output power contours at 2 GHz, $V_{CE} = 18$ V, and $I_C = 110$ mA. (From Ref. [4.12]; courtesy of Hewlett-Packard.)

3. All transistors must be well matched for power output and gain in order to obtain good load sharing.

A method that avoids the problem of paralleling power transistors is shown in Fig. 4.7.7. It uses a hybrid divider and a hybrid combiner to divide the input power equally to several amplifiers, and to combine the output power of each amplifier. The failure of one amplifier does not cause failure of the complete unit. The complete unit will continue to operate with reduced output power.

A popular two-way hybrid divider known as the *Wilkinson coupler* is shown in Fig. 4.7.8. It consists of two $\lambda/4$ transmission lines with characteristic impedances of $Z_o = \sqrt{2}\,(50) = 70.7\ \Omega$. The input signal is connected to port 1 and divides equally, both in amplitude and phase, when ports 2 and 3 are equally terminated. No power is dissipated in the 100-Ω resistor when equal loads are connected to ports 2 and 3. If ports 2 and 3 are terminated in 50 Ω, the input impedance of port 1 is the parallel combination of the two 50-Ω loads, after each is transformed by the $\lambda/4$ line with $Z_o = 70.7\ \Omega$. That is, each 50-Ω load transforms to 100 Ω, and port 1 sees a 50-Ω matched input impedance. When a mismatch occurs at port 2 or 3, the reflected signals split through the two transmission lines, travel to the input port, split again, and travel back to the output ports. That is, the reflected wave returns to the output port in two parts, each 180° out of phase from each other. The value of the resistor $2Z_o = 100\ \Omega$ was selected so that the two parts of the reflected wave have equal amplitude and, therefore, perfect cancellation results.

Of course, the two-way hybrid divider in Fig. 4.7.8 can be used as a two-way combiner by applying the input signals at ports 2 and 3 and taking the output at port 1.

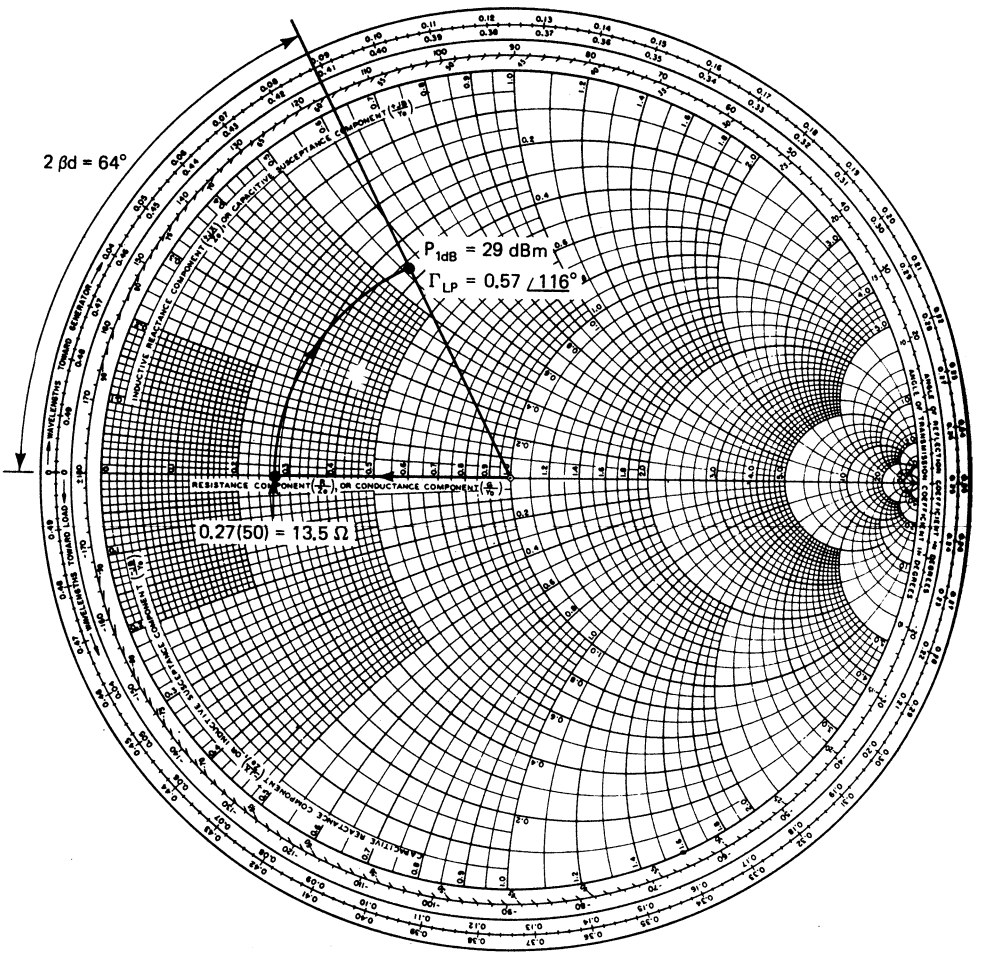


Figure 4.7.12 Design of the output matching network.

Figure 4.7.9 shows the block diagram of an n-way power combiner/divider. The insertion losses of the coupler limit the overall efficiency. The block diagram of an n-way amplifier is shown in Fig. 4.7.10.

Example 4.7.2

Design a power amplifier at 2 GHz using a BJT. The S parameters of the transistor and power characteristics at 2 GHz are

$$S_{11} = 0.64 \angle 153°$$

$$S_{21} = 2.32 \angle 10°$$

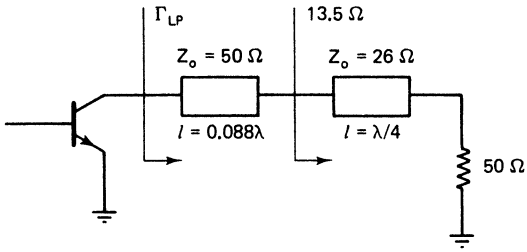


Figure 4.7.13 Output network for the 2-GHz amplifier.

$$S_{12} = 0.07\angle -8°$$

$$S_{22} = 0.51\angle -119°$$

$$P_{1dB} = 29 \text{ dBm}$$

$$G_{1dB} = 11.5 \text{ dB}$$

Output power contours are shown in Fig. 4.7.11. This figure shows the loci of equal P_{1dB} for different output loading. The input was conjugately matched at all times. The P_{1dB} point and the output conjugate match point were close. (This example is based on a design from Hewlett-Packard Application Note 972 [4.12].)

Solution. The transistor is unconditionally stable at 2 GHz since $K = 1.15$ and $\Delta = 0.207\angle 58.5°$. The output network is designed to provide the output power P_{1dB} = 29 dBm. The output matching network design is shown in Fig. 4.7.12. The 50-Ω load was transformed to a resistance of 13.5 Ω using a quarter-wave transformer with characteristic impedance Z_o given by

$$Z_o = \sqrt{50(13.5)} = 26 \ \Omega$$

A transmission line of length $\beta d = 32°$ (i.e., 0.088λ) was used to complete the match. The output network schematic is shown in Fig. 4.7.13.

In order to obtain an output power of 29 dBm, the input must be conjugately matched. The input conjugate match is calculated using (3.2.5), namely

$$\Gamma_{SP} = (\Gamma_{IN})^* = \left[0.64\angle 153° + \frac{(0.07\angle -8°)(2.32\angle 10°)(0.57\angle 116°)}{1 - (0.51\angle -119°)(0.57\angle 116°)}\right]^*$$

$$= 0.749\angle -147.1°$$

The small-signal S parameters were used to calculate Γ_s since, for this transistor, at P_{1dB} the behavior can be assumed to be linear.

The design of the input matching network is illustrated in Fig. 4.7.14. An open-circuited shunt stub of length 0.185λ (Z_o = 50 Ω), followed by a 50-Ω series transmission line of length 3.5° (0.0097λ), were used to obtain the match. The complete ac schematic is shown in Fig. 4.7.15.

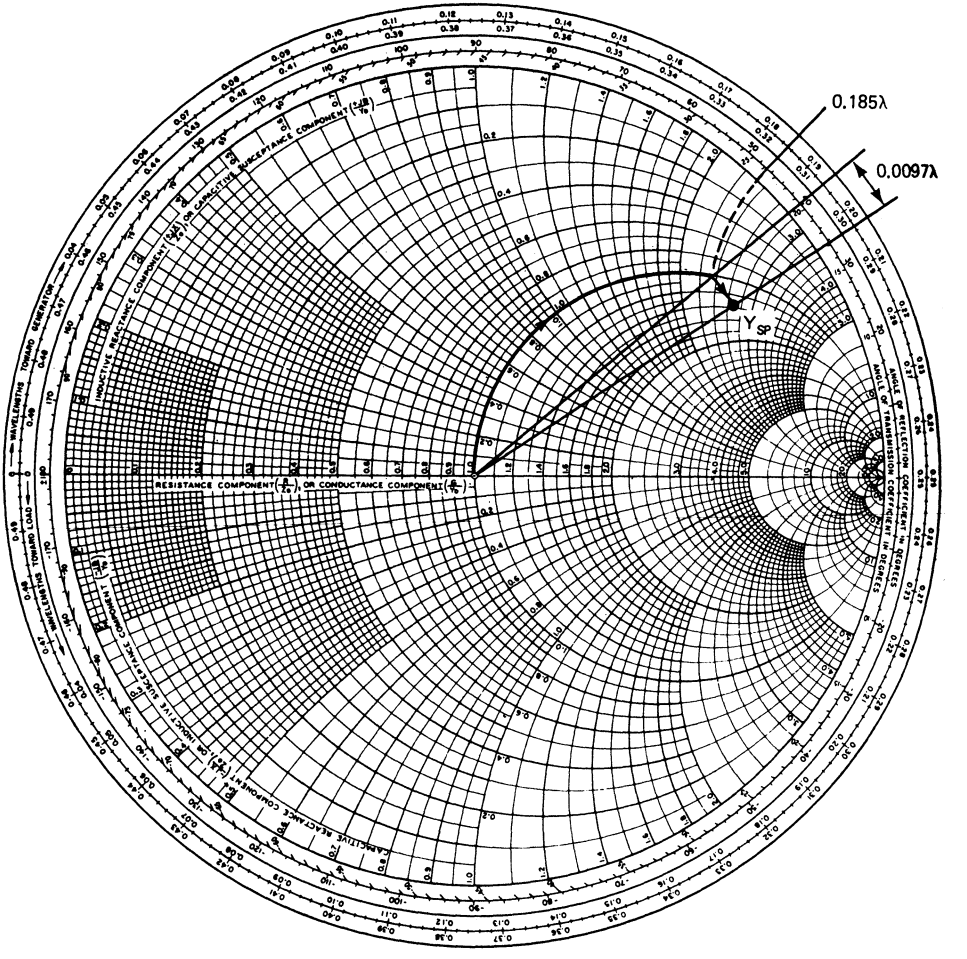


Figure 4.7.14 Design of the input matching network.

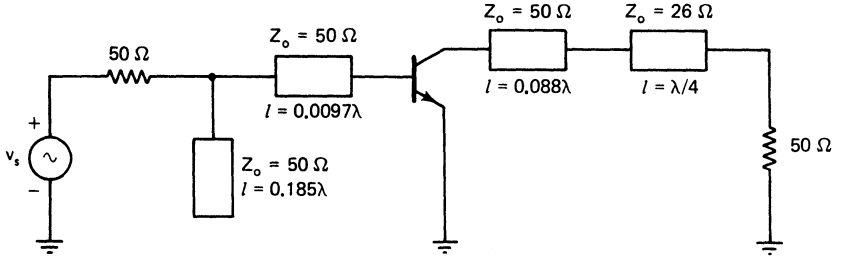


Figure 4.7.15 Schematic of the power amplifier.

4.8 TWO-STAGE AMPLIFIER DESIGN

The configuration of a two-stage microwave transistor amplifier is shown in Fig. 4.8.1. The design of a two-stage amplifier usually consists in the optimization of one of the following requirements: (1) overall high gain, (2) overall low noise figure, or (3) overall high power. In a two-stage amplifier the stability of the individual stages, as well as the overall stability, must be checked.

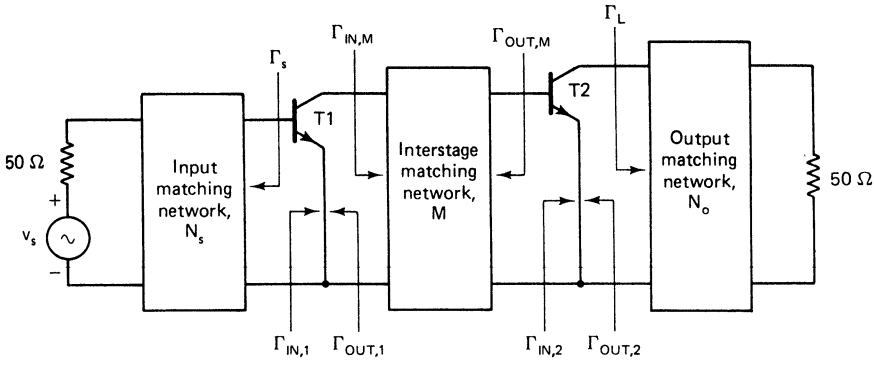


Figure 4.8.1 Diagram of a two-stage amplifier.

In a design requiring overall high gain, the reflection coefficients are selected as follows:

$$\Gamma_s = (\Gamma_{IN,1})^*$$
$$\Gamma_{IN,M} = (\Gamma_{OUT,1})^*$$
$$\Gamma_{OUT,M} = (\Gamma_{IN,2})^*$$
$$\Gamma_L = (\Gamma_{OUT,2})^*$$

In a design requiring high power the reflection coefficients are selected as follows:

$$\Gamma_s = (\Gamma_{IN,1})^*$$
$$\Gamma_{IN,M} = \Gamma_{LP,1}$$
$$\Gamma_{OUT,M} = (\Gamma_{IN,2})^*$$
$$\Gamma_L = \Gamma_{LP,2}$$

where $\Gamma_{LP,1}$ and $\Gamma_{LP,2}$ are the large-signal load reflection coefficients of $T1$ and $T2$. In other words, the design of N_o results in $\Gamma_L = \Gamma_{LP,2}$ and the design of M is for a conjugate match at its output [i.e., $\Gamma_{OUT,M} = (\Gamma_{IN,2})^*$] and at its input $\Gamma_{IN,M} = \Gamma_{LP,1}$ (i.e., to present $\Gamma_{LP,1}$ to transistor $T1$). The network N_s presents a conjugate match at the input of transistor $T1$.

In a low-noise design, the reflection coefficients are selected as follows:

$$\Gamma_s = \Gamma_{o,1}$$

$$\Gamma_{IN,M} = (\Gamma_{OUT,1})^*$$

$$\Gamma_{OUT,M} = \Gamma_{o,2}$$

$$\Gamma_L = (\Gamma_{OUT,2})^*$$

where $\Gamma_{o,1}$ and $\Gamma_{o,2}$ are the optimum noise source reflection coefficients for stages 1 and 2, respectively.

From (4.2.4), the overall noise figure of a two-stage amplifier depends on F_1, F_2, and G_{A1}. The transistor of the first stage is usually selected to have low noise figure and a higher noise figure is permitted in the second stage. Although some trade-offs between noise figure and gain are possible, usually the optimum noise match with $\Gamma_{o,1}$ and $\Gamma_{o,2}$ is used.

PROBLEMS

4.1. **(a)** Show that the noise figure for a three-stage amplifier is given by

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1}G_{A2}}$$

where F_1, F_2, and F_3 are the noise figures of the first, second, and third stages; and G_{A1} and G_{A2} are the available power gains of the first and second stages.

(b) Two cascade amplifiers have noise figures of $F_1 = 1$ dB and $F_2 = 3$ dB, and a gain of $G_{A1} = 10$ dB and $G_{A2} = 16$ dB. Calculate the overall noise figure.

4.2. The scattering and noise parameters of a GaAs FET measured at a low-noise bias point ($V_{DS} = 5$ V, $I_D = 15\% I_{DSS} = 10$ mA) at $f = 12$ GHz are

$$S_{11} = 0.75\angle -116^\circ \qquad F_{min} = 2.2 \text{ dB}$$

$$S_{12} = 0.01\angle 67^\circ \qquad \Gamma_o = 0.65\angle 120^\circ$$

$$S_{21} = 3.5\angle 64^\circ \qquad R_N = 10\ \Omega$$

$$S_{22} = 0.77\angle -65^\circ$$

Design a microwave transistor amplifier to have a minimum noise figure.

4.3. The scattering and noise parameters of a GaAs FET measured at a low-noise bias point ($V_{DS} = 3.5$ V, $I_D = 15\% I_{DSS} = 12$ mA) at $f = 2$ GHz are

$$S_{11} = 0.8\angle -51.9^\circ \qquad F_{min} = 1.25 \text{ dB}$$

$$S_{12} = 0.045\angle 54.6^\circ \qquad \Gamma_o = 0.73\angle 60^\circ$$

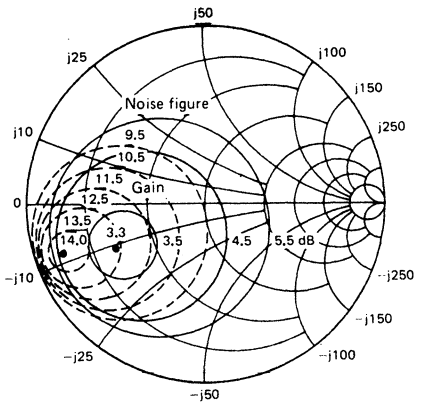
$$S_{21} = 2.15\angle 128.3^\circ \qquad R_N = 19.4\ \Omega$$

$$S_{22} = 0.73\angle -30.5^\circ$$

Design a microwave transistor amplifier to have a minimum noise figure.

4.4. **(a)** A manufacturer provides the information shown in Fig. P4.4 for two microwave transistors. Evaluate the noise parameters for each transistor. Are the constant-gain circles given for G_T, G_A, or G_p?

(b) Verify the location of the $G_A = 10.7$ dB constant-gain circle in Fig. 4.3.4.

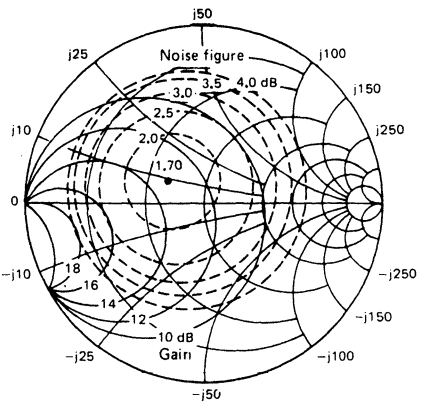


Frequency = 2 GHz, 10 V, 5 mA

$S_{11} = 0.655 \angle 162.1°$ $S_{21} = 2.286 \angle 45.8°$

$S_{12} = 0.064 \angle 23.7°$ $S_{22} = 0.569 \angle -54.6°$

(a)



Frequency = 2 GHz, 10 V, 5 mA

$S_{11} = 0.646 \angle 172°$ $S_{21} = 3.042 \angle 47.9°$

$S_{12} = 0.051 \angle 13.5°$ $S_{22} = 0.642 \angle -64°$

(b)

Figure P4.4 Two microwave transistors. (From Avantek Transistor Designers Catalog; courtesy of Avantek.)

4.5. **(a)** Design a microwave transistor amplifier at 2 GHz to have a minimum noise figure using the transistor in Fig. P4.4a. Specify the resulting G_T, G_A, and G_p.

(b) Design a microwave transistor amplifier at 2 GHz to have $F_i = 2.5$ dB using the transistor in Fig. P4.4b. Specify the resulting G_T, G_A, and G_p.

4.6. **(a)** In the network shown in Fig. P4.6, verify that $|\Gamma_a| = |\Gamma_{IN}|$, where

$$|\Gamma_a| = \left|\frac{Z_a - Z_o}{Z_a + Z_o}\right|$$

and

$$|\Gamma_{IN}| = \left|\frac{Z_{IN} - Z_s^*}{Z_{IN} + Z_s}\right|$$

(b) Show that $|\Gamma_a|$ can also be expressed in the form

$$|\Gamma_a| = \left|\frac{\Gamma_{IN} - \Gamma_s^*}{1 - \Gamma_{IN}\Gamma_s}\right|$$

4.7. Verify (4.4.1), (4.4.2), and (4.4.3).

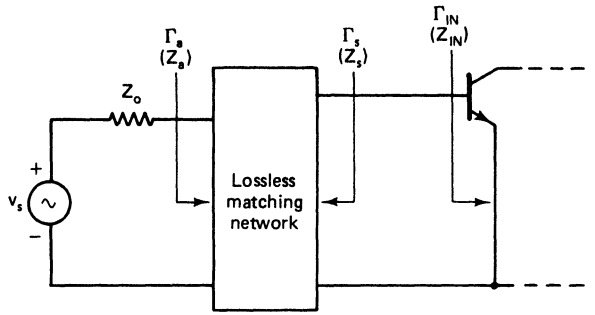


Figure P4.6

4.8. Design a broadband microwave BJT amplifier to have $G_{TU} = 12$ dB from 150 to 400 MHz. The transistor S parameters are as follows:

f (MHz)	S_{11}	S_{21}	S_{22}
150	$0.31\angle -36°$	5	$0.91\angle -6°$
250	$0.29\angle -55°$	4	$0.86\angle -15°$
400	$0.25\angle -76°$	2.82	$0.81\angle -26°$

(This problem is based on an example given in Ref. [4.13].)

Hint: G_s will be small and only G_L should be used to compensate for the variations of $|S_{21}|$ with frequency. G_s should be designed to provide a good VSWR at the input. The output matching network can be designed as in Fig. 4.4.4, or for a better match at the three frequencies an extra inductor in series with the 50-Ω load can be added.

4.9. Design a broadband microwave BJT amplifier with $G_{TU} = 10$ dB from 1 to 2 GHz with a noise figure of less than 4 dB. For this transistor S_{12} can be neglected and the scattering and noise parameters are as follows:

f (GHz)	S_{11}	S_{21}	S_{22}	Γ_o	R_N	F_{min} (dB)
1	$0.64\angle -98°$	$5.04\angle 113°$	$0.79\angle -30°$	$0.48\angle 23°$	23.3	1.45
1.5	$0.60\angle -127°$	$3.90\angle 87°$	$0.76\angle -35°$	$0.45\angle 61°$	15.6	1.49
2	$0.59\angle -149°$	$3.15\angle 71°$	$0.75\angle -43°$	$0.41\angle 88°$	15.7	1.61

In this problem, design the input and output matching networks so that $G_{TU} = 10$ dB at the band edges only, and calculate the resulting gain at 1.5 GHz. The noise figure over the band must be less than 4 dB.

4.10. **(a)** In the network shown in Fig. P4.10a, what is the best Γ_x that can be achieved in the frequency range 400 to 600 MHz?

(b) In the network shown in Fig. P4.10b, what is the best Γ_x that can be obtained in the range 6 to 12 GHz?

4.11. For the networks in Fig. 4.4.15b, c, and d, the gain–bandwidth restrictions are

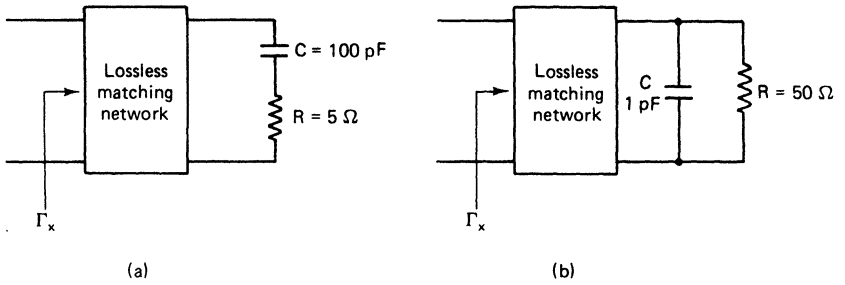


Figure P4.10

given by

$$\int_0^\infty \frac{1}{\omega^2} \ln \left|\frac{1}{\Gamma}\right| d\omega \leq \pi RC \qquad \text{(for Fig. 4.4.15b)}$$

$$\int_0^\infty \frac{1}{\omega^2} \ln \left|\frac{1}{\Gamma}\right| d\omega \leq \frac{\pi L}{R} \qquad \text{(for Fig. 4.4.15c)}$$

$$\int_0^\infty \ln \left|\frac{1}{\Gamma}\right| d\omega \leq \frac{\pi R}{L} \qquad \text{(for Fig. 4.4.15d)}$$

Show that Γ_x can be expressed in the form given in (4.4.8) when the appropriate definitions of Q_1 and Q_2 are used. These are given in Fig. 4.4.15.

4.12. **(a)** Verify the equation for δ_{IN} in (4.5.1).

(b) Verify the relation between δ_{IN} and Γ_L in (4.5.2).

(c) Derive a relation for δ_{OUT}.

4.13. **(a)** Show that K for the balance amplifier, using a 3-dB Lange coupler, is given by

$$K = \frac{1 + P^2}{2P}$$

where

$$P = |S_{21} S_{12}|$$

Show that K has a minimum value of 1 when $P = 1$ (i.e., when $|S_{21} S_{12}| = 1$) and $K > 1$ for all other values of P.

(b) The S parameters of a transistor at 2.1 GHz are

$$S_{11} = -0.699 - j0.348$$

$$S_{21} = -10.9 + j7.895$$

$$S_{22} = 0.309 + j0.459$$

$$S_{12} = 0.009 + j0.015$$

and the resulting K, $K = 0.48$, shows that the transistor is potentially unstable. If the transistor is used in a balanced amplifier configuration, calculate the resulting S parameters and K.

4.14. The S parameters of a transistor at 8 GHz are

$$S_{11} = 0.75\angle -100°$$
$$S_{21} = 2.5\angle 93°$$
$$S_{12} = 0$$
$$S_{22} = 0.7\angle -50°$$

Determine

(a) The terminations for $G_{TU,\max}$.

(b) The inherent bandwidths and Q of the input and output networks.

(c) The additional elements (C or L) that must be added to the input and/or output networks to make the bandwidth 20% of the inherent bandwidth.

(d) The optimum terminations for part (c) and the resulting G_{TU}.

4.15. In a microwave transistor amplifier it is found that $\Gamma_{Ms} = 0.476\angle 166°$ and $\Gamma_{ML} = 0.846\angle 72°$ at $f = 4$ GHz. Calculate the amplifier input and output intrinsic bandwidths. If the bandwidth is to be limited to 400 MHz, find the value of C_{OUT} or L_{OUT} that must be added to the output network.

4.16. Analyze the Wilkinson coupler shown in Fig. 4.7.8.

4.17. An amplifier has a transducer power gain of 30 dB, 800-MHz bandwidth, and a noise figure of 5 dB. The 1-dB gain compression point is given as 28 dBm. Calculate DR, DR_f, and the maximum output power for no third-order intermodulation distortion.

4.18. The specifications for two power GaAs FETs at 4 GHz are as follows:

	P_{1dB} (dBm)	G_{1dB} (dB)	G_p (dB)
FET 1	25	6	7
FET 2	20	8	9

Show that the two-way power amplifier shown in Fig. P4.18 can be used to deliver $P_{OUT} = 27.7$ dBm, at 1 dB compression, with $P_{IN} = 6.3$ dBm. The loss of the two-way combiner/divider is -0.3 dB. Specify the FET that must be used in each stage, and indicate the power and gain levels at all points.

Hint: The power at the output of the divider is 19.9 dBm.

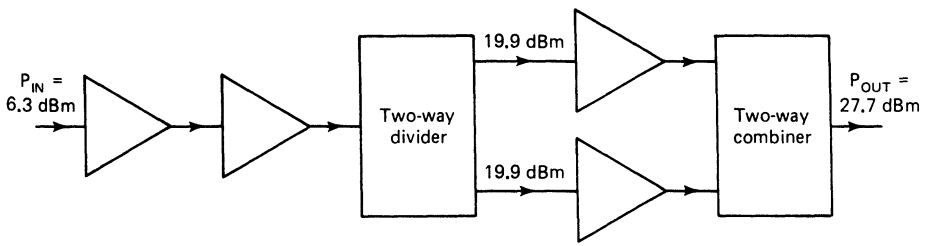


Figure P4.18

4.19. Design a power amplifier at 4 GHz using a BJT. The S parameters of the transistor and power characteristics at 4 GHz are

$$S_{11} = 0.32\angle -145^\circ$$

$$S_{21} = 1.38\angle -113^\circ$$

$$S_{12} = 0.08\angle -98^\circ$$

$$S_{22} = 0.8\angle -177^\circ$$

$$P_{1\text{dB}} = 27.5 \text{ dBm}$$

$$G_{1\text{dB}} = 7 \text{ dB}$$

$$\Gamma_{LP} = 0.1\angle 0^\circ$$

4.20. In the two-stage amplifier shown in Fig. 4.8.1, transistors $T1$ and $T2$ are potentially unstable. Can the overall amplifier be unconditionally stable?

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