CHAPTER

ELEVEN

POWER AMPLIFIERS

11.1 INTRODUCTION

Power amplifiers are those amplifiers whose design concerns are based on a combination of output power, drive level, power dissipation, distortion, size, weight, and efficiency (power output divided by power supplied). Simultaneously, the transistors used in power amplifiers have requirements based on breakdown voltage, current limitations, and maximum power dissipation. The output power of power amplifiers can range from the milliwatt region for small, portable transistor amplifiers to the megawatt region for large broadcast stations.

The power amplifier is invariably the last stage in the amplifier chain because the power level is highest at this point; no intermediate-stage amplifier would be operated with a power gain significantly less than 1. Because the signal level is the largest at this point, it results in the maximum amount of distortion due to the nonlinear characteristics of the device. These nonlinearities produce unwanted frequency components (harmonics) and intermodulation distortion (IMD) products. However, there are various methods of designing circuits, methods which lead to different levels of efficiency and create different amounts of distortion. Because various modulation techniques can tolerate different amounts of distortion, power-amplifier design depends on the type of signal (modulation) to be amplified. In the least efficient design, the maximum amount of power is dissipated in the transistor, requiring larger and more expensive transistors than would otherwise be required. However, good power-amplifier design techniques can result in more economical and reliable electronics.

Power amplifiers are classified according to their mode of operation; the most frequently used classes are discussed in this chapter. The class of operation is determined by how the transistor is biased and the nature of the output circuit.

The original classification of operating modes included class A, B, AB, and C amplifiers. A class A amplifier is a linear amplifier. Theoretically, it will produce a sine-wave output in response to a sine-wave input. The output frequency will be the same as the input frequency, and the output amplitude will be a linear function of the input amplitude. If the amplifier output is a linear function of the input over 50 percent (180°) of the input waveform, it is categorized as class B. If the linear conduction angle is less than 50 percent, it is class C; and if the conduction angle is greater than 180° but less than 360°, it is referred to as class AB.

Today, additional classes of amplifiers exist, most of them using the transistor as a switch. The more popular forms of switching amplifiers are considered after the class A, B, and C amplifiers have been described.

11.2 CLASS A AMPLIFIERS

Class A power amplifiers are no different in behavior from the linear amplifiers studied up to this point, except that their power and distortion levels are of primary importance. For class A operation the output will be a sine wave in response to a sine-wave input. The class of generation is determined by the input signal level and how the transistor is biased. Figure 11.1 describes an ac coupled amplifier which can be biased for class A, B, or C.

For the amplifier shown in Fig. 11.1 the transistor quiescent voltage (no ac collector current) is

$$V_{ce} = V_Q = V_{cc} - I_c R_E \qquad (11.1)$$

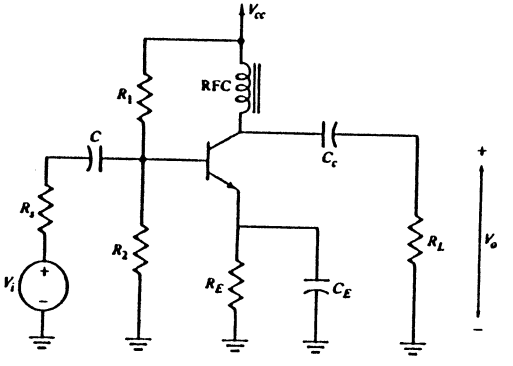

Figure 11.1 An ac coupled amplifier.

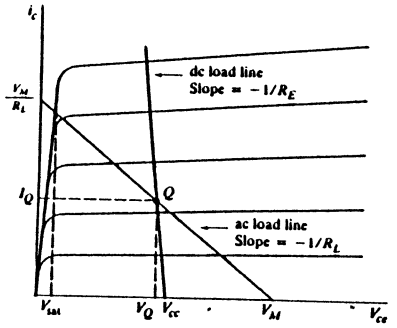

Figure 11.2 Transistor collector-emitter characteristics including the ac and dc load lines.

The slope of the dc load line dI_c/dV_{ce} is then $-1/R_E$, as illustrated in Fig. 11.2. In class A power amplifiers the dc resistance R_E will normally be much less than the ac resistance. R_E is kept small to limit the dc power dissipated in the resistor. In some designs R_E is zero, but a small R_E is often included for bias stabilization of bipolar transistor amplifiers and self-biasing of field-effect transistor amplifiers. If R_E is small, the Q (quiescent) -point voltage is

$$V_Q \approx V_{cc}$$

For ac operation the coupling and emitter bypass capacitors act as short circuits, and the ac collector current i_c is given by

$$-i_c R_L = V_o$$

The output voltage is equal to the ac voltage drop across the transistor output:

$$V_{cc} - i_c R_E + V_{ce} \approx V_Q - i_c R_L \qquad (11.2)$$

From the transistor characteristics of Fig. 11.2, it is seen that the collector-to-emitter voltage is at a maximum when the collector current is zero. This occurs when the ac component of collector current is equal in magnitude and opposite in direction to the dc collector current ($i_c = -I_C$). Likewise, the collector-to-emitter voltage is zero when the collector current is at a maximum (the alternating current component is equal in magnitude and direction to the direct current I_C). As the collector current decreases from the Q point due to the ac signal, the collector-to-emitter voltage increases from V_Q to V_M; and as the collector current increases, the collector voltage decreases from V_Q to zero.

For small-signal amplifiers it is well known that the maximum power gain is obtained by matching the load impedance to the transistor output impedance. In power amplifiers the objective is to obtain maximum output power, not maximum gain. The amplifiers are operated at less than maximum gain. This requires a large input drive signal but results in greater output power. For class A operation maximum output power is obtained by selecting the ac load

impedance such that the maximum signal swing can be obtained from the device. The output must be symmetrical to avoid distortion. In an ideal transistor $V_{sat} = 0$, the collector-to-emitter voltage can decrease from V_{cc} to zero; so for symmetrical operation it can also increase to

$$V_M = 2V_Q = 2V_{cc}$$

Likewise, the output current can decrease from I_Q to zero, so the maximum output current is

$$I_M = \frac{V_M}{R_L} = \frac{2V_{cc}}{R_L}$$

and

$$I_Q = \frac{V_{cc}}{R_L}$$

The slope of the ac load line is $-1/R_L$ and

$$-R_L^{-1} = -\frac{I_M}{V_M} = \frac{-I_Q}{V_{cc}}$$

This is the value of the load resistance that results in maximum output power.

A surprising characteristic of this amplifier is that the maximum voltage dropped across the transistor is twice the supply voltage, and the peak-to-peak output voltage is also $2V_{cc}$. How this is possible can be seen from the equivalent circuit shown in Fig. 11.3. Here the RF choke has been replaced by a constant current source since no alternating current flows through the device and the direct current is I_Q. Also, no direct current flows through the capacitor; therefore the dc voltage drop across the device is V_{cc}, and there is no ac voltage drop across the capacitor. Here the capacitor can be replaced by a battery V_{cc}. At the instant at which the load current is

$$i_L = -i_C = -I_Q = \frac{V_{cc}}{R_L}$$

the output voltage is

$$V_o = I_Q R_L = V_{ce}$$

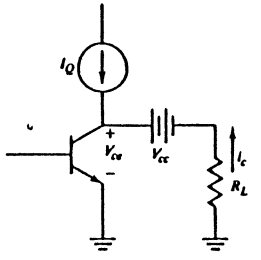

Figure 11.3 A small-signal equivalent circuit of the amplifier shown in Fig. 11.1.

If the emitter-resistor is sufficiently small,

$$V_{ce} = V_o + V_{cc}$$

so

$$(V_{ce})_{max} \approx 2V_{cc}$$

For a sinusoidal input signal the collector current consists of a dc component I_Q, which does not flow through the load, and an ac component i_L, which does flow through the load. That is,

$$i_C = I_Q + i_L$$

where $i_L = I_p \sin \omega t$. Since the collector current cannot become negative, $I_p \leq I_Q$. The average power will be

$$(P_o)_{av} = \frac{I_p^2 R_L}{2} \leq \frac{I_Q^2 R_L}{2}$$

and the power supplied by the battery will be (neglecting the small amount of power dissipated in the base bias circuitry)

$$P_{cc} = V_{cc} I_Q = \frac{V_{cc}^2}{R_L}$$

so the efficiency is

$$\eta = \frac{P_o}{P_{cc}} = \frac{I_p^2 R_L^2}{2V_{cc}^2} \tag{11.3}$$

The maximum efficiency occurs for $I_p = I_Q$ and is

$$\eta_{max} = \frac{I_Q^2 R_L^2}{2V_{cc}^2} = 50\%$$

The maximum operating efficiency for a class A ac coupled power amplifier is 50 percent and occurs with the maximum input signal. If the output signal decreases, I_p decreases and so does the efficiency.

The power dissipated in the transistor is

$$P_T = P_{cc} - P_o = \frac{V_{cc}^2}{R_L}\left(1 - \frac{I_p^2}{2I_Q^2}\right) \tag{11.4}$$

The maximum power dissipated in the transistor

$$(P_T)_{max} = \frac{V_{cc}^2}{R_L} = 2(P_o)_{max} \tag{11.5}$$

occurs when there is no input signal, and it is equal to twice the maximum power that can be delivered to the load. Also, as previously discussed, the maximum collector-to-emitter voltage is twice the supply voltage.

Example 11.1 Design a class A amplifier to deliver 5 W to a 50-Ω load.

SOLUTION For 5-W power in a 50-Ω resistor, the peak value of the sinusoidal voltage across the resistor is

$$V_p = (2 \times 5 \times 50)^{1/2} = 22.4 \text{ V}$$

Since the peak voltage cannot exceed V_{cc}, a standard supply $V_{cc} = 24$ V would be suitable. The corresponding peak value of the ac load current is

$$I_p = \frac{22.4}{50} = 0.448 \text{ A}$$

Therefore, the transistor must be biased so that

$$I_Q \geq 0.448 \text{ A}$$

For a 24-V supply with no emitter (or source) resistance,

$$I_Q = \frac{V_{cc}}{50} = 0.48 \text{ A}$$

The power supplied is then

$$P_{cc} = V_{cc} I_Q = 11.52 \text{ W}$$

and the efficiency is

$$\eta = \frac{5}{11.52} = 43.4\%$$

The transistor that is selected must be able to dissipate 11.52 W in case the input power drops to zero, and the transistor collector-to-emitter breakdown voltage must be at least 48 V ($2V_{cc}$).

The effect of the saturation voltage is to create signal distortion and reduce efficiency. The maximum value of collector current that can be applied without V_{ce} decreasing to V_{sat} has the peak value

$$(I_p)_{max} = \frac{V_{cc} - V_{sat}}{R_L}$$

Therefore, when the saturation voltage is considered, the maximum efficiency is

$$\eta_{max} = \frac{1}{2}\left(1 - \frac{V_{sat}}{V_{cc}}\right)^2 \tag{11.6}$$

Transformer-Coupled Class A Amplifiers

If a load impedance is specified, a transformer can be used to improve the power gain by transforming the load impedance to that required for maximum output power. A class A transformer-coupled FET amplifier is shown in Fig. 11.4, and the load lines for the amplifier are shown in Fig. 11.5. The characteristic curves

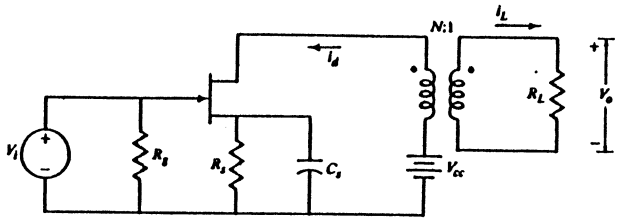

Figure 11.4 A transformer-coupled class A amplifier.

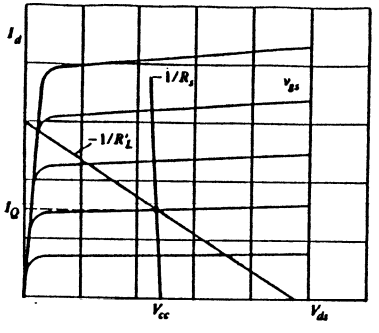

Figure 11.5 ac and dc load lines of the amplifier shown in Fig. 11.4.

are similar to those of the bipolar transistor amplifier, except that the controlling signal for the field-effect transistor is the gate-to-source voltage.

If the transformer is ideal,

$$i_L = Ni_d$$

where i_d is the ac drain current. The ac voltage across the drain-to-source junction is

$$v_d = Nv_o$$

Therefore, the ac load impedance seen by the transistor is

$$R'_L = N^2 R_L \tag{11.7}$$

The slope of the dc load line is $-1/R_S$, and if $R_S \ll R'_L$, the slope of the ac load line is $-1/R'_L$. The maximum signal swing is again $2V_{cc}$ (ignoring V_{sat}) and the peak drain current is

$$I_M = (i_d)_p = \frac{2V_{cc}}{R'_L} \tag{11.8}$$

The power calculations for the transformer-coupled load are the same as for the capacitive-coupled load. The transformer provides additional flexibility for matching the load to the source, but the power dissipated in the transformer can significantly reduce the amplifier efficiency. Transformer- or inductor-coupled bipolar transistor amplifiers are subject to a phenomenon known as *thermal runaway*.[11.1] The heating up of the transistor causes more current to flow, which causes greater self-heating, which can cause the device to self-destruct. The problem rarely occurs with resistive loads since the increased current results in a reduced collector-to-emitter voltage, and eventually the circuit will reach equilibrium. Nor does the problem arise with FET amplifiers because as their temperatures increase, their output currents decrease.

Class A Push-Pull Amplifiers

As mentioned in Chap. 12, push-pull amplifiers eliminate the even harmonic distortion present in the amplifier output. This can provide a significant improvement in the performance of linear amplifiers. Also, push-pull operation reduces the power requirements of the individual transistors. Figure 11.6 illustrates a class A transformer-coupled push-pull stage. The ac equivalent circuit is shown in Fig. 11.7. In class A operation, both transistors continuously

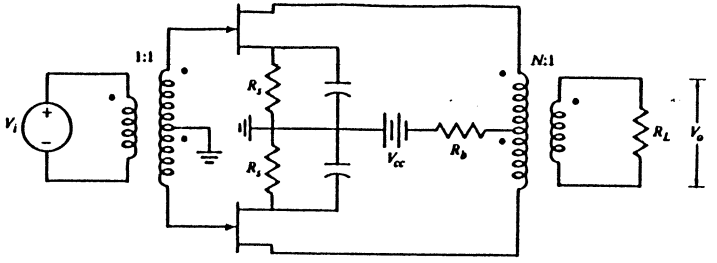

Figure 11.6 A class A transformer-coupled push-pull amplifier.

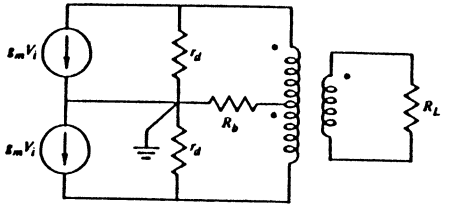

Figure 11.7 A small-signal equivalent circuit of the push-pull amplifier.

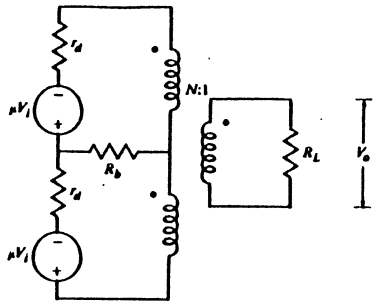

Figure 11.8 Another equivalent circuit of the push-pull amplifier shown in Fig. 11.6.

drive the output, and the transistor outputs, which are 180° out of phase, are combined in the center-tapped output transformer. The circuit of Fig. 11.7 can be redrawn as shown in Fig. 11.8 using Thévenin's theorem; the results developed for center-tapped transformers (Chap. 6) are now directly applicable. Here the amplification factor $\mu = g_m r_d$. If the dynamic drain resistances of the transistors are equal, then no current will flow through R_b and the circuit can be redrawn as shown in Fig. 11.9. The output voltage V_o is determined by

$$2\mu V_i - 2r_d i_d = -2NV_o$$

If the transformer is lossless,

$$2NV_o = -i_d(2N)^2 R_L = -2R'_L i_d$$

where $R'_L = 2N^2 R_L$, the output voltage is

$$V_o = \frac{-N\mu R_L V_i}{r_d + R'_L} = \frac{-Ng_m R_L V_i}{1 + R'_L/r_d}$$

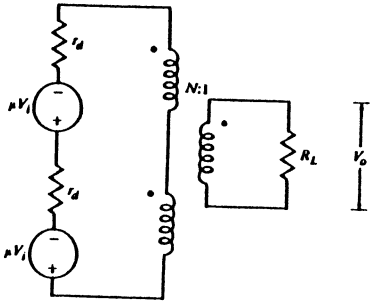

Figure 11.9 A simplified equivalent circuit of the push-pull amplifier.

Normally $r_d \gg R'_L$, so the voltage gain is

$$A_v = -g_m R_L N$$

since the load for each transistor is

$$R'_L = 2N^2 R_L$$

For maximum output power (i.e., maximum signal swing) each transistor is biased so that

$$R'_L = \frac{V_{cc}}{I_d}$$

where I_d is the dc drain current.

The maximum output power (from both transistors) is

$$P_o = \frac{2V_{cc}^2}{2R'_L} = \frac{V_{cc}^2}{(2N^2 R_L)}$$

The total output power of the class A push-pull amplifier is twice that of the single-ended class A amplifier; however, the maximum voltage drop across each transistor is the same as that of the single-ended amplifier. The power supplied to each transistor is

$$P_{cc} = I_d V_{cc} = \frac{V_{cc}^2}{R'_L}$$

The total power supplied is $2P_{cc}$, so the maximum efficiency of the class A push-pull amplifier is $\eta = 50$ percent, the same as the efficiency of the single-ended amplifier. Besides reducing even harmonic distortion, the push-pull configuration can provide twice the output power of the single-ended design.

Square-Wave Input

The efficiency of a class A amplifier depends on the input signal level and also on the signal waveshape. Consider the case of a square-wave input. If the amplifier is class A, the collector current is also a square-wave, as shown in Fig. 11.10. The dc value is I_Q and the peak current is

$$I_p \leq I_Q$$

In this case

$$P_{cc} = I_Q V_{cc} = I_Q^2 R_L$$

and

$$P_o = I_p^2 R_L$$

so the efficiency

$$\eta = \frac{P_o}{P_{cc}} = \frac{I_p^2}{I_Q^2} \qquad (11.9)$$

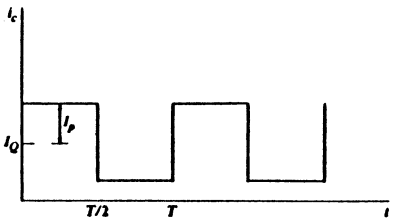

Figure 11.10 A collector-current waveform.

will approach 100 percent if I_p approaches I_Q. The efficiency of the class A amplifier depends on the waveform of the input signal.

If a tuned circuit is used as the load, as is frequently the case in order to minimize distortion, then efficiency is reduced. With a square-wave input the collector current will again be a square wave, as shown in Fig. 11.10, and the power supplied is again

$$P_{cc} = I_Q V_{cc}$$

If the tuned-circuit bandwidth is sufficiently narrow and tuned to the fundamental frequency, the output power is

$$P_o = \frac{I_1^2 R'_L}{2}$$

where I_1 is the amplitude of the fundamental frequency component of the output current

$$I_1 = \frac{4}{\pi} I_p$$

The maximum output power will be

$$(P_o)_{max} = \frac{8 I_p^2 R'_L}{\pi^2} = \frac{8 I_Q V_{cc}}{\pi^2}$$

and the maximum efficiency will be

$$\eta = \frac{(P_o)_{max}}{P_{cc}} = \frac{8}{\pi^2}$$

If the output is tuned to the nth harmonic (n-odd), the efficiency will be $\eta = 8/n^2\pi^2$, since the amplitude of the nth (odd) harmonic of a square wave is $1/n$ times that of the fundamental frequency. A tuned-circuit load decreases the efficiency, but it is frequently used since the tuned circuit reduces the output harmonic distortion.

11.3 CLASS B AMPLIFIERS

A major disadvantage of the class A amplifier is that all of the supply power is dissipated in the transistor when there is no input. It is usually advantageous to have no power supplied when there is no input signal, which is the case with a class B amplifier. A class B amplifier is biased as shown in Fig. 11.11. The quiescent collector current is zero, and the collector-to-emitter quiescent voltage is V_{cc}. It is biased just at the edge of the active region so that for a sine-wave input the transistor will conduct over 180° of the input waveform, as illustrated in Fig. 11.12.

The output current is a highly distorted sine wave, but the distortion can be removed by using a narrowband tuned circuit for the load, or what is more frequently done, by operating two class B transistor amplifiers in push-pull, as illustrated in Fig. 11.13. Ideally, each transistor conducts over alternate 180° of the input cycle, and the two outputs are summed so that an undistorted sine wave appears across the load resistor R_L. At any time, one transistor is conducting and the other is not, so the equivalent circuit can be drawn as shown in Fig. 11.14. The load seen by each transistor

$$R'_L = N^2 R_L$$

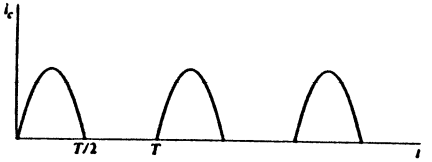

Figure 11.11 Collector-current waveform of a class B amplifier.

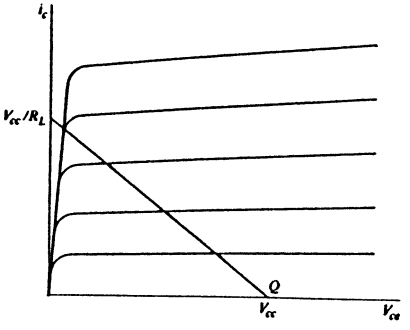

Figure 11.12 Q-point biasing for a class B amplifier.

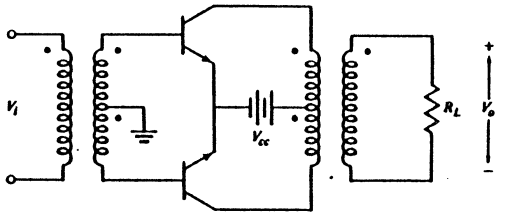

Figure 11.13 A class B push-pull amplifier.

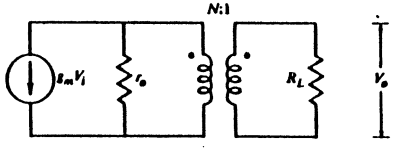

Figure 11.14 The small-signal equivalent circuit of the class B push-pull amplifier.

is one-half that of the class A push-pull amplifier. The voltage gain is

$$\frac{V_o}{V_i} = \frac{-g_m r_o N R_L}{r_o + R'_L}$$

It is usually the case that $r_o \gg R'_L$, so $A_v = -g_m R_L N$. The voltage gain of the class B stage is one-half that of the class A push-pull amplifier, so the drive requirements for the class B stage are two times as great. The increased drive requirement, however, is offset by the greater efficiency and power-handling capabilities of the class B amplifier.

The power-handling capability of each class B amplifier shown in Fig. 11.13 will now be evaluated by considering a sinusoidal input and a resistive load. The transistors are assumed to be ideal. Each transistor conducts when V_i is greater than zero, and the collector current is zero when V_i is negative. Since the load current conducts for 180° of a complete input cycle,

$$i_c(t) = I_p \sin \omega t \qquad 0 \le \omega t \le \pi$$
$$= 0 \qquad \pi \le \omega t \le 2\pi$$

The dc collector current is then

$$I_c = T^{-1} \int_0^{T/2} I_p \sin \omega t \, dt = \frac{I_p}{\pi} \tag{11.10}$$

The dc value of the base current is much less than I_c, so the dc power supplied

$$P_{cc} = I_c V_{cc} = \frac{I_p V_{cc}}{\pi}$$

The ac power delivered to the load is

$$P_o = \frac{R'_L}{T} \int_0^{T/2} (I_p \sin \omega t)^2 \, dt = \frac{I_p^2 R'_L}{4}$$

Since $I_p \le V_{cc}/R'_L$, the maximum output power from each transistor is

$$(P_o)_{max} = \frac{V_{cc}^2}{4R_L} \tag{11.11}$$

The power supplied by the input circuit will normally be much less than the dc power, so the efficiency at maximum output power is

$$\eta = \frac{V_{cc}^2}{4R_L} \frac{\pi R_L}{V_{cc}^2} = \frac{\pi}{4} = 78.5\%$$

The efficiency of a class B amplifier is much higher than that of a class A stage. In addition, the class B stage consumes no power when an input signal is not present. This is a most significant advantage in many applications (the class A amplifier has maximum power dissipation when no signal is present). The power dissipated in the transistor of the class B amplifier is

$$P_T = P_{cc} - P_o = \frac{I_p V_{cc}}{\pi} - I_p^2 \frac{R'_L}{4} \tag{11.12}$$

The maximum power dissipated in the transistor is found by differentiating Eq. (11.12) with respect to I_p. It is found that the maximum dissipation occurs for

$$I_p = \frac{2V_{cc}}{\pi R'_L}$$

and

$$(P_T)_{max} = \frac{V_{cc}^2}{\pi^2 R'_L} = (P_o)_{max} \frac{4}{\pi^2} \tag{11.13}$$

Note, however, that the maximum transistor dissipation does not occur when the output power is a maximum. The class B stage also results in less transistor power dissipation than a class A stage. This is an expected result of greater operating efficiency. Another important difference between the two is that the maximum voltage drop across the transistor in a class B amplifier is V_{cc}; it is $2V_{cc}$ for the class A amplifiers previously described. Class A amplifiers, therefore, require transistors with a higher collector-to-emitter breakdown voltage. Differences in class A and B power amplifiers are illustrated by the following example.

Example 11.2 Design a class B push-pull amplifier to deliver 5 W (maximum) to a 50-Ω load.

SOLUTION Assume that a transformer-coupled amplifier such as the one illustrated in Fig. 11.13 is used with a 1:1 turns ratio. Since a push-pull amplifier is used, each class B amplifier will supply 2.5 W. The required supply voltage can be obtained from Eq. (11.11):

$$V_{cc}^2 = 4R_L(P_o)_{max} = 500\ \text{V}^2$$

A supply voltage V_{cc} of 24 V would be a suitable choice. The power-handling requirements of the transistor can be determined from Eq. (11.13):

$$(P_T)_{max} = (P_o)_{max}\frac{4}{\pi^2} = 1\ \text{W}$$

The peak output current will be

$$I = \left(\frac{4P_o}{R_L}\right)^{1/2} = 0.45\ \text{A}$$

The voltage and/or current requirements can be modified by selecting a different turns ratio for the transformer.

Example 11.1 discussed using a class A amplifier to realize these same specifications. Note that the class A amplifier transistor dissipation is over 11 times greater than that of the class B transistor, so if a class A push-pull amplifier is used, the power-handling requirements of each transistor would be 5½ times that of the transistors used in the class B amplifier. Also, the collector-to-emitter breakdown voltage of the class A transistors must be double that of the transistors used in class B amplifiers.

While the class B amplifier also has the significant advantage of no power being dissipated when an input signal is not present, practical class A amplification does produce less distortion. All in all, if the distortion produced by class B amplification is acceptable, its benefits make it preferable to class A amplification. Large-signal distortion can be reduced with negative feedback.

Push-Pull Amplification with Complementary Transistors

Transformerless push-pull amplifiers can be realized using either bipolar or field-effect transistors with complementary symmetry. Figure 11.15 illustrates a push-pull amplifier using power MOSFETs. The current source and resistor R_b are used to bias the transistors for class B operation, and the MOSFETs do not turn on until the input voltage exceeds the threshold voltage of the device.

Power MOSFETs have several advantages over bipolar transistors. The most important is that the drain current has a negative temperature coefficient that decreases with increases in temperature, since the positive temperature

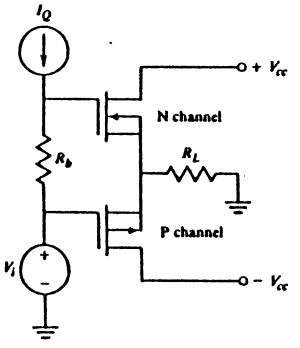

Figure 11.15 A class B push-pull amplifier using complementary MOSFETs.

coefficient of bipolar transistors can result in self-destruction unless complicated biasing circuits are used. Bipolar transistors also have an undesirable characteristic when operated at high voltages. The collector current is no longer uniform, but tends to concentrate in small areas, causing very high peak temperatures, known as *hot spots*, in these areas. The average junction temperature, measured at the transistor case, does not show the presence of hot spots, which degrade the transistor performance. The drain current of power MOSFETs is distributed uniformly, preventing the development of hot spots. The high input impedance (and hence high power gain) of the MOSFETs is another advantage. The upper frequency limits and power-handling capability of power MOSFETs have been continually increasing as manufacturing techniques have improved. Bipolar transistors are minority carrier devices that accumulate charge in the base region. This causes a problem in class B and C operation because removing the charge takes time and energy. One consequence is increasing power dissipation with increasing frequency. FETs are majority carrier devices; the charge carriers are controlled by an electric field and not by injection of minority carriers into the active region. The gate regions, therefore, contain no stored charge, and switching between the on and off states is very fast.

The first field-effect transistors were useful only at lower (less than 1 W) power levels. Their major limitation was that the FET drain-to-source channel was parallel to the chip surface, so the current density was much less than that of bipolar transistors (which utilized vertical current flow). For a given current the FET chip had to be much larger than an equivalent BJT chip, which meant a lower yield and a higher cost. Several new technologies have recently been developed that produce high-voltage, high-current FETs. The three most frequently used manufacturing technologies are VMOS (vertical MOS), V-JFET (vertical JFET) and DMOS (double-diffusion MOS).[11.2]

Power Relations in the Direct-Coupled Class B Push-Pull Amplifier

For the push-pull amplifier shown in Fig. 11.15, the maximum average ac output power in response to a sine-wave input is

$$(P_o)_{av} = \frac{V_{cc}^2}{2R_L} \tag{11.14}$$

The power delivered by each transistor is

$$(P_o)_{av} = \frac{V_{cc}^2}{4R_L} \tag{11.15}$$

The power delivered by each supply is

$$P_{cc} = V_{cc}T^{-1}\int_0^{T/2} \frac{V_{cc}}{R_L}\sin \omega t\, dt = \frac{V_{cc}^2}{\pi R_L} \tag{11.16}$$

so the efficiency of this circuit is the same as that of the transformer-coupled push-pull amplifier. The maximum power dissipated in each transistor is

$$(P_T)_{max} = \frac{V_{cc}^2}{\pi^2 R_L} \tag{11.17}$$

the same as for the transformer-coupled push-pull circuit. The only difference between the two circuits deduced from a power analysis is that the transformerless circuit requires two power supplies.

When the current requirements exceed the limitations of a single transistor, transistors can be operated in parallel. Figure 11.16 illustrates a class B amplifier containing two power MOSFETs.[11.3] It is usually easier to parallel

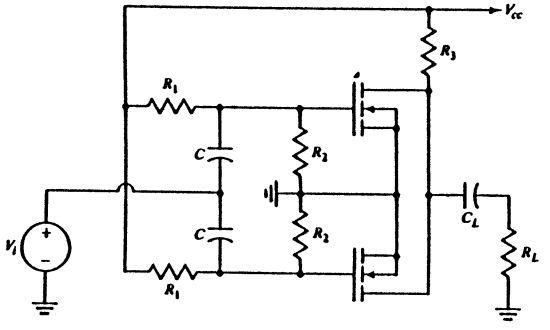

Figure 11.16 A class B amplifier using two MOSFETs in parallel.

FETs than bipolar transistors because of their larger input impedance. In this particular circuit, approximately two times as much output power could be obtained as from a class B circuit using a single transistor of the same type.

Class B amplifiers all suffer from crossover distortion, which occurs because of the nonlinear behavior of small-signal levels. The silicon BJT requires that the base-to-emitter junction be forward-biased by approximately 0.7 V before the collector current will flow. FETs also exhibit a nonlinear behavior for low signal levels. For these reasons power amplifiers are usually operated with a slight forward bias to reduce crossover distortion. This operation is often referred to as *class AB*, but it is essentially the same in that the power levels and efficiency are only slightly reduced from those of class B amplifiers.

PROBLEMS

11.1 A transistor with a peak current rating of 5 A and a maximum drain-to-source voltage of 50 V is to be used in a class A power amplifier. What is the maximum output power? If a load resistance of 50 Ω is specified, what turns ratio for a matching transformer is required?

11.2 Compare the designs of class A and class B power amplifiers to deliver 20 W to a 50-Ω load. The power supply is 24 V. Specify the maximum transistor dissipation, peak output voltage, and peak output current for each design.

11.3 Calculate the efficiency of the direct-coupled class A power amplifier shown in Fig. P11.3. What is the maximum voltage across the transistor?

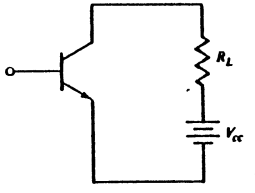

Figure P11.3 A direct-coupled class A amplifier.

11.4 Design a transformerless class B power amplifier using complementary symmetry transistors to deliver 20 W to a 50-Ω load. Specify the maximum transistor dissipation, peak output voltage, and peak output current for each transistor.

11.5 Figure P11.5 illustrates three different methods of biasing a class A amplifier. Compare the efficiency factor

$$\frac{\text{Peak output power}}{\text{Transistor dissipation with no input signal}}$$

for the three configurations.

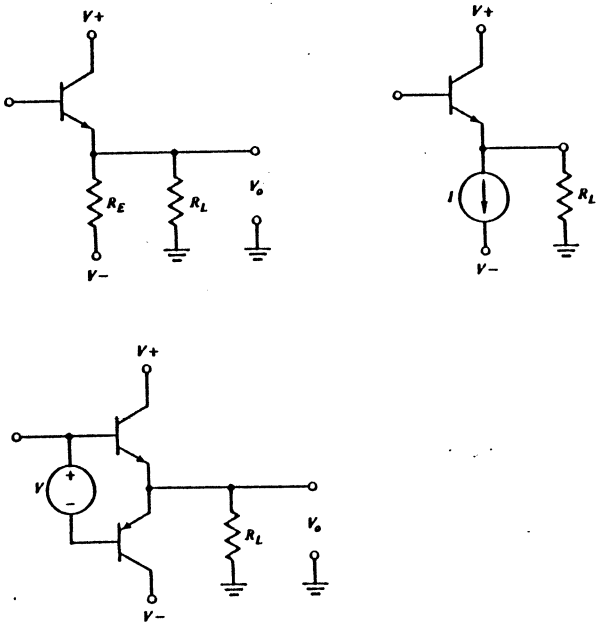

Figure P11.5 Three methods of class A biasing.

11.6 Design a power amplifier using the DV 1260T power MOSFET (see App. 1 for specification). The load resistance is 50 Ω, and is to be coupled to the transistor with a transformer (which is assumed to be 90 percent efficient). What is the maximum possible output power without exceeding the transistor maximum ratings? What are the required supply voltage and current?

11.7 Design a class A push-pull amplifier to deliver 100 W to a 50-Ω load. Use DV1260T MOSPOWER FETs. (App. 1). Specify the supply voltages, bias network, and turns ratios of any transformers used. The source resistance is 500 Ω.

11.8 Design a class C amplifier that will deliver an average power of 20 W at 1 MHz using the DV1260T MOSPOWER FET (see App. 1).

11.9 Determine the maximum output power and conduction angle of a class C amplifier using the DV1260T MOSFET and a 48-V supply voltage (see App. 1).

11.10 If a class C amplifier is to be used as a frequency tripler, what should the conduction angle be for maximum output power?

11.11 Determine the maximum output power of a frequency tripler using the DV1260T MOSFET and a 48-V supply voltage (see App. 1).

11.12 Design a complementary class D amplifier to deliver 100 W to a 50-Ω load using DV1260T transistors (see App. 1). Assume typical transistor values. A 48-V supply is to be used, and an impedance matching transformer can be used for the output.

11.13 What is the efficiency of the amplifier of Prob. 11.12? What will efficiency be if a DV1260T FET is used?

11.14 What is the maximum output power possible using DV1260T transistors in a class D amplifier? (See App. 1). What will be the maximum value of supply voltage?

11.15 Describe a technique for class S amplification that uses single-edge pulse-width modulation.

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11.4 Rowe, H. E.: *Signals and Noise in Communication Systems*, Van Nostrand, New York, 1965, p. 277.

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ADDITIONAL READING

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Furlan, J.: Preliminary Analysis of the Transistor Tuned Power Amplifier, *Proc. IEEE*, 52:311 (1964).

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The basic circuit we will analyze is shown in Figure 1 which is a complementary-symmetry class B or AB power amplifier. It is assumed that Q1 and Q2 are complementary transistors, i.e. that they have almost identical I_C-V_{CE} curves, identical β's, etc. This is a requirement for designing any class-B amplifier. The 2N2222 and 2N2907 which are used in the lab form one complementary pair; another complementary pair is the 2N3904/2N3906. Many other complementary pairs are commercially available.

The biggest problem with designing a class B amplifier is to design a bias circuit to give a stable Q point near cutoff. There are many ways to bias the class B amplifier.

The first we will examine is the simple voltage-divider we typically use to bias a class A amplifier. Figure 1 shows the circuit necessary to bias the class B complementary symmetry amplifier..

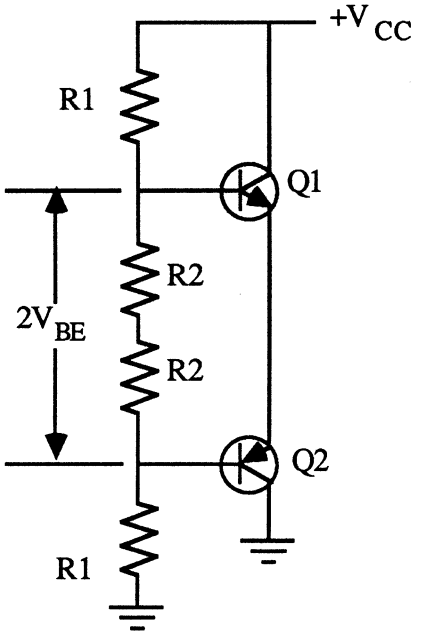


Figure 1 - Resistive-divider biasing of class B transistor amplifier

The assumptions we will make are that the collector and emitter currents are identical (Realistically, they will be very close to each other unless the transistor β is very small as may be the case with power transistors). For the transistors to be at cutoff the transistor V_{BE} must be between 0.6 and 0.7 volts (the exact voltage is a function of the specific transistor type being biased). This voltage will appear across the two resistors shown as R_2 in Figure 1. Note that R_2 will typically be a single resistor; two resistors are shown to emphasize the symmetric nature of the complementary class B amplifier. The resistor R_2 can be vary easily calculated by

$$R_2 = \frac{V_{be}}{I_D}$$

where V_{BE} is the desired base-emitter voltage and I_D is the current we choose to go through the resistive divider. The same considerations apply for picking I_D as applied earlier. Simply pick I_D large enough that the voltage drop across R_2 will not be affected by changes in the transistor

base currents. If we examine the diode equation for the base-emitter junction we see that a small change in V_{BE} creates a very large change in I_E (because of the exponential nature of the equation). Typically, a change of only 60mV in V_{BE} might change the emitter current by 1000%. The resistors needed for a particular V_{BE} can be calculated as shown above but the typical resistor tolerances preclude using a resistor for design. Typically, R_2 is a potentiometer which is adjusted for the proper bias emitter current.

The major problem with this design is the temperature dependence of the base-emitter diode. Remember that the diode equation contains a temperature dependence in the exponent. A very small change in temperature due to transistor heating (This is the temperature at the junction inside the transistor by the way—not the temperature of the case!) or variations in environmental temperature can cause drastic shifts in bias point. This process can lead to a condition called thermal runaway in which the transistor heats up due to the emitter currents. This increases the base-emitter junction temperature which increases the emitter current which further increases the junction temperature and so forth. Basically, this is a positive feedback situation and is the major reason why only cheap, low-power amplifiers use resistive biasing.

A superior way to bias the class B amplifier is to use what is known as a current mirror shown in Figure 2. This technique uses a diode (or the base-emitter junction of an identical transistor) in place of R2 in Figure 1. If the diode equation for the two semiconductor devices (the diode and the transistor base-emitter junction) is identical, they will exhibit the same junction current. Why is this? The devices are in parallel so they have the same applied voltage. If they have identical diode characteristics this means that their junction currents (the current through the diode and the current through the transistor base-emitter junction) must be the same. In practice, we set the voltage across the diode/base-emitter junction pair with a resistive voltage divider. If we assume that the junctions are biased near cutoff this means that the required junction voltage will be near 0.6 volts. So, a simple resistor to VCC as shown in Figure 2 serves to bias the transistor.

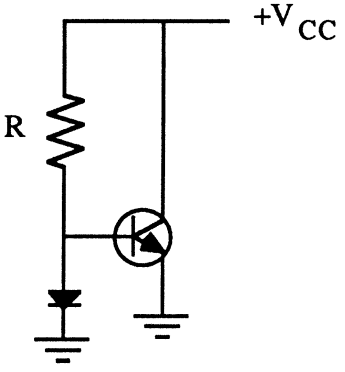


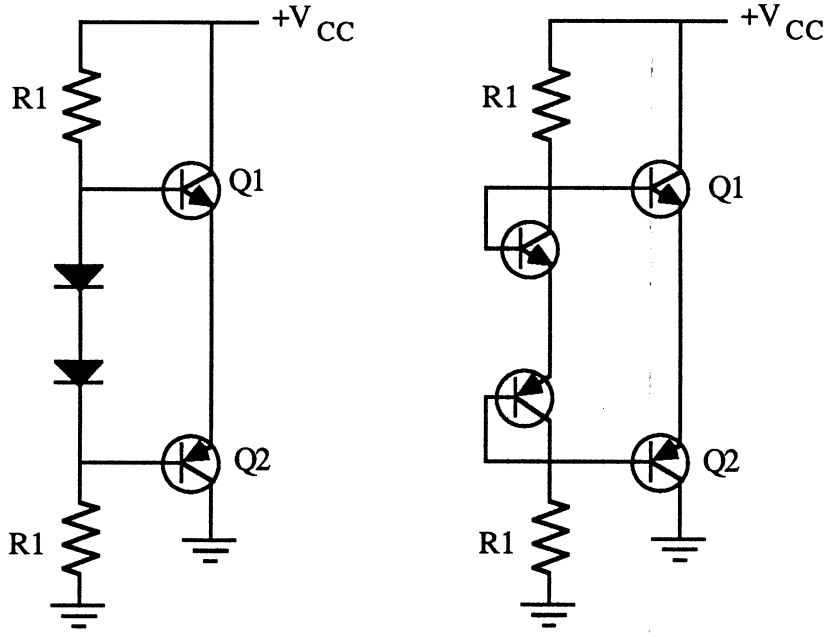
Figure 2 - current mirror

The value of the bias resistor R is chosen by

$$R = \frac{V_{CC} - V_{BE}}{I_E}$$

where IE is the desired emitter bias current. As before, the exact value of R needed depends upon the relationship between VBE and IE (the diode equation) and will be slightly different for every transistor (even if they are of the same type). In practice, it is reasonable to estimate R

using the above equation and then use a variable resistor to get the exact bias current you want. However, how about thermal runaway? Basically, the resistor R limits the current through the diode D. If the emitter current increases due to an increased junction temperature the diode current will increase since this is a current mirror. A increase in diode current, however, results in an increased voltage drop across R and a decrease in V_{BE} which lowers the diode current and, because this is a current mirror, also lowers the emitter current. This is now a situation of negative feedback and the transistor/diode pair should remain at a stable operating point even as the temperature changes. Note that this assumes that the diode and base-emitter diode characteristics match exactly. If they do not match exactly, which is reasonable for a diode and a transistor, there is the potential for thermal runaway although it may take higher temperatures to cause it. The solution is to make the diode characteristics as identical as possible. The simple solution is to replace the diode with a transistor which is identical to the transistor being biased. The base-emitter junctions are put in parallel and the bias transistor's collector is tied to the base of the bias transistor. This circuit is should possess very nearly identical diode characteristics, if the transistors are reasonable well matched, and be very immune to thermal runaway. An example of this type of circuit used to bias a class B amplifier is shown in Figure 3. As an aside this type of bias scheme is often used in integrated circuits.



(a) diode biasing

(b) equivalent use of transistors

Figure 3 - Current mirror biasing of class-B amplifier

The designer might rest at this point having overcome thermal runaway; however, the basic class B amplifier as shown possesses very little voltage gain. In fact, the class B complementary symmetry power amplifier is simple two symmetric emitter followers which have a voltage gain near 1. They can have very large current and power gains, however, which is why this type of amplifier is called a power amplifier. The typical class B power amplifier might have the signal source capacitor coupled into the resistor-diode bias network as shown in Figure 4.

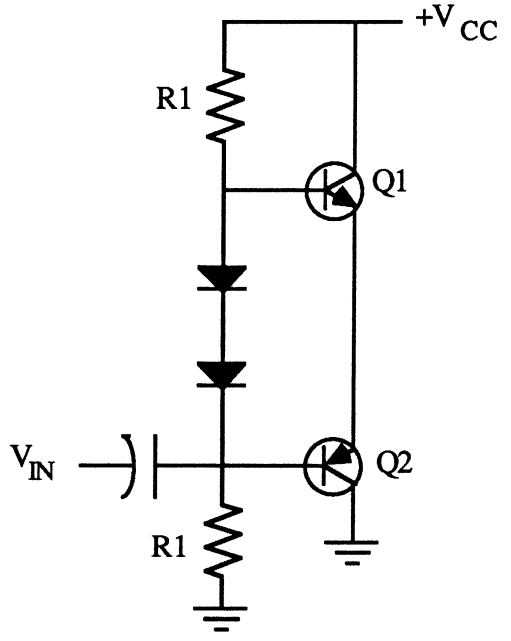


Figure 4 - Capacitor coupling to a class-B power amplifier

A more sophisticated and satisfactory (from an engineering design viewpoint) solution is the circuit shown in Figure 5.

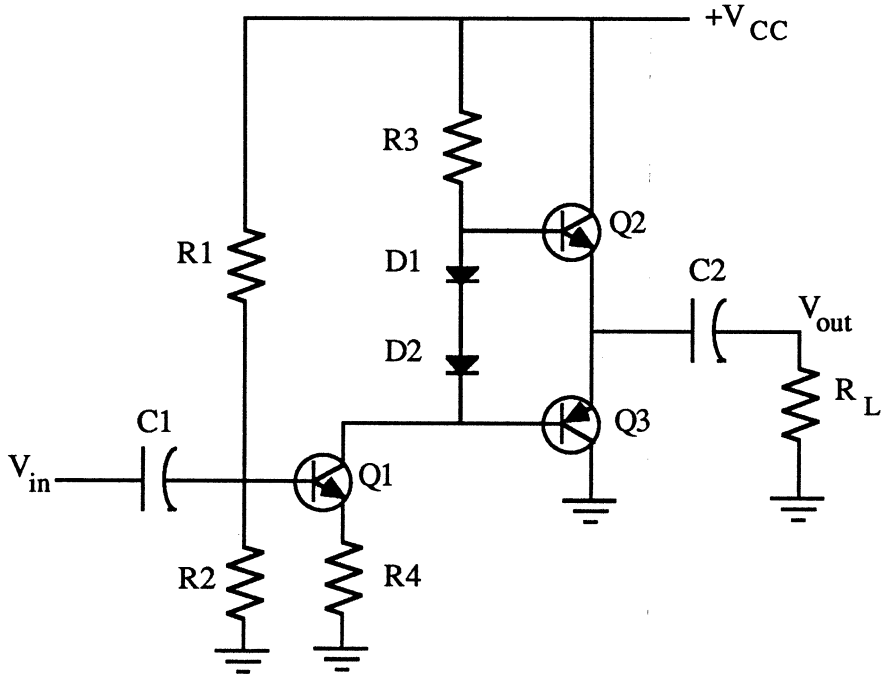


Figure 5 - Class B power amplifier with current mirror biasing and transistor driver

A direct-coupled common-emitter amplifier replaces one of the resistors used to bias the power amplifier transistors. The bias current through the driver transistor Q_1 is also the bias current through the bias diodes (or transistors) and, because the bias scheme is a current mirror, will also be the bias emitter current for the power amplifier transistors, Q_2 and Q_3. This circuit is very attractive for implementation because varying the base current of Q_1 (which is very small) can control the (typically) much larger bias currents in Q_2 and Q_3. The value of R is not very critical anymore and is typically chosen to represent a nominal value for a 0.6 volt drop across the base-emitter junctions of Q_2 and Q_3. An example of this calculation is at the end of this section.

From an ac viewpoint we now have a common-emitter amplifier driving an emitter-follower with the overall voltage gain being the product of the voltage gains of each individual amplifier stage. Since the output stages are emitter followers with voltage gains near one this means that the overall voltage gain is approximately the voltage gain of the common-emitter driver amplifier Q_1. What is the voltage gain of this stage. This is an un-bypassed common-emitter amplifier so the voltage gain is

$$A_V \approx -\frac{R_L}{R_E}$$

where R_E is the emitter resistor of Q_1. What is R_L? We might say that R_L is the other bias resistor R_1 and be approximately correct. From the small-signal viewpoint (at low audio frequencies) the bias diodes are electrically on and do not contribute any appreciable resistance or capacitance to the small-signal model. This allows us to ignore the diodes. The bias resistor R_1 is certainly in the driver collector circuit; however, the input impedance of the power amplifiers Q_2 and Q_3 is in parallel with R_1. Q_2 and Q_3 are complementary-transistor amplifiers so one is off whenever the other is on. This is not quite true in a class-AB amplifier but will be ignored here. The basic rule for a common emitter amplifier is that the input impedance is simply β times the emitter resistance and will give a reasonable approximation for our calculations. Power transistor's tend to have lower β's than small-signal transistors and the values of the amplifier loads are in the range of 5-100 ohms depending upon the amplifier application. This gives an estimate of the transistor input impedance which is on the order of several hundred to several thousand ohms. This value is not negligible when compared to the bias resistor R_1 and will significantly lower the amplifier gain. Furthermore, since the circuit is usually biased in a class-AB mode with both transistors being slightly "on" both transistors will contribute to the parallel impedance across R_1 lowering the voltage gain of Q_1 even more. A complete class-AB amplifier is analyzed in Example 1.

There are many variants of the class B amplifier. The most common is the split power supply. As shown in Figure 5 the load is capacitor coupled to the load. This is not acceptable for amplifiers which require DC (or very low-frequency) response. If the power supplies are split with a +V being applied to Q2 and a -V being applied to Q3 as shown in Figure 6 the emitters of Q2 and Q3 will be very near ground potential. If the load resistor is reasonable small the load can be DC coupled to the transistor emitter's. This is the configuration most often found in high-end audio equipment and industrial servo amplifiers. For the same power supply voltage this circuit will produce more output power (assuming that the power supplies can deliver it) because of the increased voltage across each transistor.

Sometimes the amplifier load varies considerably and we want the performance of the amplifier to remain very stable. This requires a "stiffer" output. Stiff as used here means a lower

amplifier output impedance. This can be achieved by increasing the current gain of the power amplifier stage using Darlingtons to replace the ordinary power transistors as shown in Figure 7. Note the use of additional diodes in the bias network due to the presence of additional diode drops in the bias circuit.

Assume that V_{CC}=30 volts. Because the class-B amplifier we are using is symmetric each transistor will have a V_{CE} of 15 volts and the emitter of Q_3 will be at +15 volts. Assuming that the diode voltage drop is 0.7 volts (It actually will probably be between 0.5 and 0.6 volts.) The base of Q_2 is at +15.7 volts and the base of Q_3 (which is also the collector of Q_1) is at +14.3 volts. Assume that we are to bias the output transistors at 14.3 mA. This means that the current through the diodes will also be 14.3 mA because of the current mirror. Furthermore, the current through Q_1 and R_1 will also be 14.3 mA. Let's examine R_3 first. From Ohm's Law R_3=(30-15.7 volts0/14.3 mA = 1kΩ. The only remaining unknown is R_4 which can be selected for a particular voltage gain. If Q_2 and Q_3 have a β of 120 the input impedance of the class-B amplifier (assuming only one transistor is ON) is approximately $z_{in}=\beta R_L$ = 120(100Ω) = 12kΩ. The parallel combination of z_{in} and R_3 is 923Ω. Let's assume we want to design for a voltage gain of 10, a nice round number. Then, the emitter resistor is determined by $A_V=-R_L/R_E$. In this case, $R_E=R_L/A_V$=923Ω/10=92.3Ω. The emitter voltage of Q_1 is then $I_E R_E$ = (14.3mA)(92.3Ω)=1.33 volts. The bias V_{CE} for Q_1 is then 14.3-1.33=12.97 volts. Q_1 can now be biased if we know its dc characteristics. It was assumed that V_{CC} and the bias collector current were previously chosen based upon considerations involving the desired output power and R_L.

Example 1 - Analysis of the class B amplifier of Figure 5

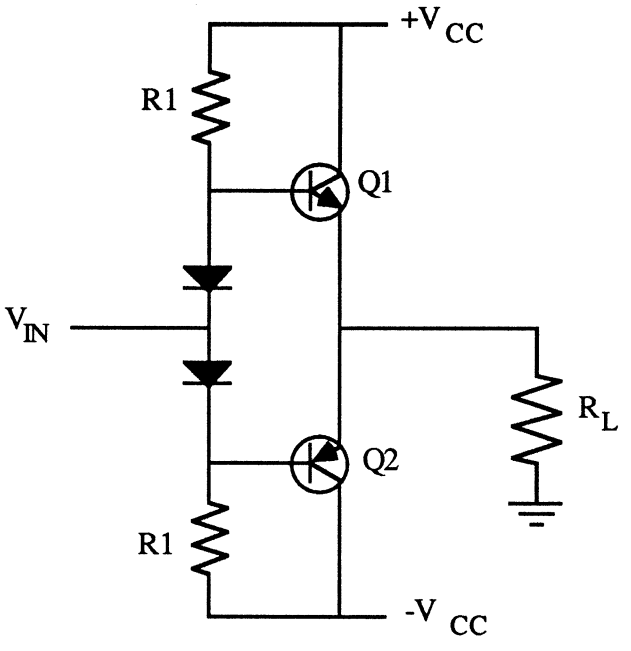


Figure 6 - Split-power supply used with class-B complementary symmetry amplifier

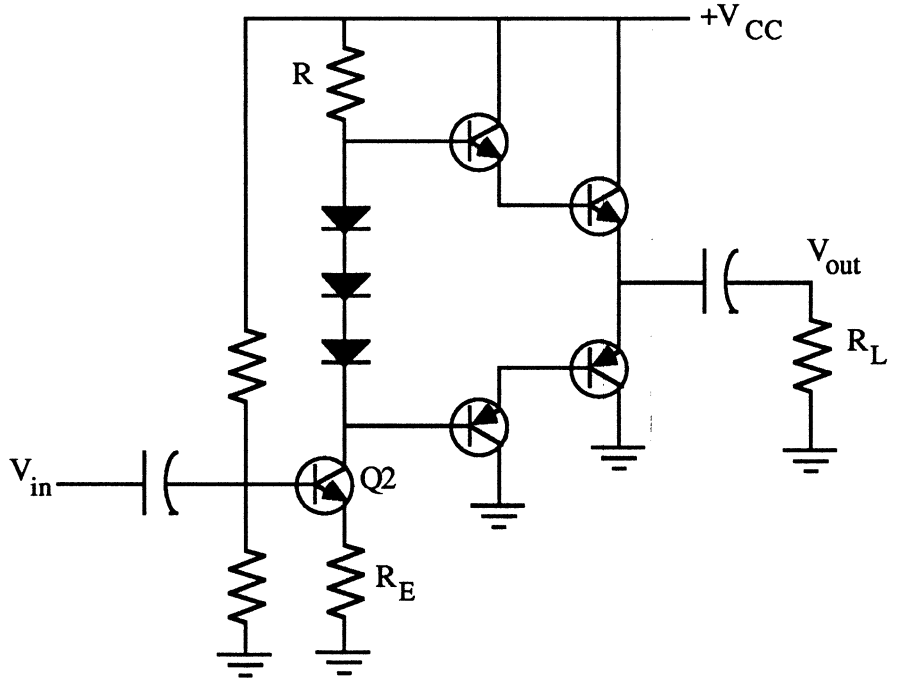


Figure 7 - Darlington complementary-symmetry power amplifier.

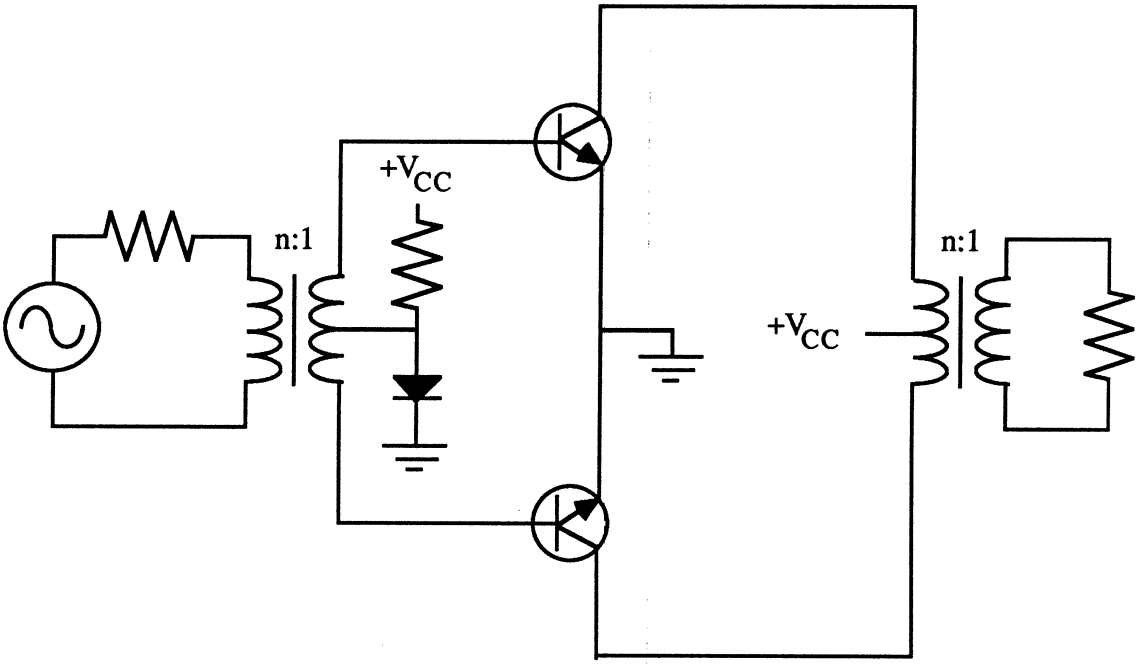


Figure 8 - Transformer-coupled class B power amplifier

The complementary symmetry power amplifier is by far the most common type of class-B power amplifier. The transformer coupled class-B power amplifier as shown in Figure 8 is still

found in many audio applications. Note that this design uses transistors of the same type with power supply and bias supplied through the transformers. This poses no problem for the bias network but the large output currents of a power amplifier may cause core saturation in the output transformer and a consequent loss of power. Furthermore, transformers designed for large currents tend to be rather large, very heavy because of the iron cores, and very expensive which are all motivations for using the complementary symmetry configuration.

The transformer-coupled class B amplifier uses transistors of the same type (either npn or pnp) and does result in easier matching of transistors. However, because both transistors are of the same type each transistor must be supplied with an input signal that is 180 degrees out of phase (i.e. inverted) with respect to the other. The input transformer accomplishes this by using a center-tap as a voltage reference. The two transformer outputs will then be 180 degrees out of phase with respect to each other since their windings are in the same direction and they are tied in series. Basically, the result is very similar to putting two batteries in series and tieing their common point to ground to achieve a split-power supply. The transistors can be biased in the same manner we have seen for the complementary symmetry power amplifier. The transistors are dc coupled through the transformer so it is convenient to supply the bias voltage through the transformer center-tap. Because there is only one diode drop from this point to ground only one diode will be used to ground. Note that this is not a very good current mirror because there are two transistor base-emitter junctions in parallel with the bias diode. As the temperature changes the currents will not compensate exactly and this amplifier configuration can be subject to thermal runaway. As the bias point is adjusted so that the amplifier is operating in class B rather than AB the performance of the current mirror will improve since only one transistor will be on at a time.

The input transformer is often replaced by a semiconductor phase splitter or other such circuit. An example of a simple circuit of this type is shown in Figure 9. This does remove one transformer but offers few significant advantages over the transformer other than the possibility of additional gain.

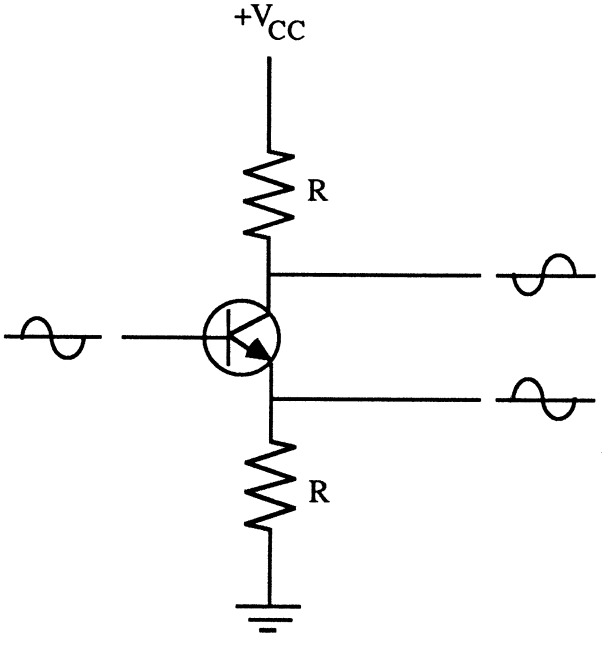


Figure 9 - Transistor phase splitter

All transistors are rated as to a maximum power dissipation they can handle before self-destructing. An overheated transistor junction can act exactly like a fuse and blow-out! Most transistor specification sheets will list a maximum power dissipation P_D and a maximum junction temperature (the critical parameter), $T_{J(max)}$. For example, the 2N3904 has a $T_{J(max)}$ of 150 degrees C and a P_D of approximately 800 mW. The P_D is specified for an ambient temperature of 25 degrees C and must be de-rated (decreased) for operation in higher ambient temperatures. This is usual practice since we want electronic equipment to operate on hot days; furthermore, the insides of electronic equipment usually is considerably hotter than 25 degrees C. The P_D that is specified on a transistor data sheet is actually $P_{D(max)}$ and must be de-rated for temperatures above 25 degrees C. This is done by the manufacturer supplying either a derating curve which lists the transistor power rating as a function of operating temperature, or a power derating factor which can be used to calculate the decrease in transistor P_D as a function of ambient temperature. Specifically,

$$\Delta P = D(T_A - 25°)$$

where ΔP is the loss in P_D, i.e. the new P_D is $P_{D(max)}$-ΔP, T_A is the ambient temperature in which the transistor is to operate, and D is the supplied derating factor.

This picture changes somewhat when transistor heat sinks are utilized. Specifically, high power transistors are designed with metal tabs or surfaces which are directly connected to the transistor collector. These allow conduction of heat away from the transistor to cool the transistor and allow operation at higher powers or in higher ambient temperatures than would be possible otherwise. In such designs both the temperature of the transistor case and the ambient air are important and the derating calculation becomes slightly more complex.

The following analysis assumes that the power transistor is heat-sinked to allow it to operate at high output powers. A slight amount of thermodynamics is in order at this point. The relationship between the transistor case temperature, the heat sink temperature, and the ambient temperature can be visualized as a series resistance circuit as shown in Figure 10.

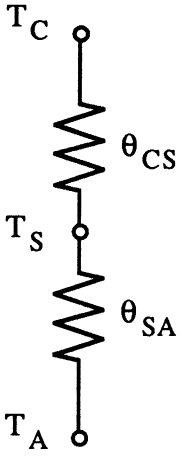


Figure 10 - Electrical equivalent circuit of case/heat sink thermodynamics

θ_{CS} is the thermal resistance between the transistor case and the heat sink, θ_{SA} is the thermal resistance between the heat sink and ambient air. Both resistances are highly dependent upon

the design of the heat sink and are usually supplied by the heat sink manufacturer since most electrical engineers are not good thermodynamicists. A typical set of values might be θ_{CS}=0.5°C/watt and θ_{SA}=1.5°C/watt. To analyze the circuit of Figure 10 we need to complete the analogy between thermodynamics and electrical circuits noting that power corresponds to current, θ corresponds to resistance and temperature corresponds to voltage. This allows us to write Ohm's Law for the resistances of Figure 10 as

$$P_D = \frac{T_C - T_A}{\theta_{CS} + \theta_{SA}}$$

where we combined the thermal resistances into a single resistance $\theta_{CS} + \theta_{SA}$, T_C is the case temperature, T_A is the ambient temperature, and P_D is the transistor power dissipation. Solving this expression for the case temperature gives

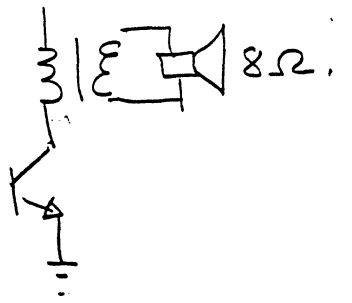
$$T_C = T_A + P_D(\theta_{CS} + \theta_{SA})$$

which can be used to calculate the case temperature of a heat-sinked transistor. The power derating calculations are then done based upon the case temperature.

REFERENCES:

Albert Malvino, ELECTRONIC PRINCIPLES, Third Edition, McGraw-Hill, 1984. Chapter 10, Class A and B Power Amplifiers.

Example class A



want $P_{OUT} = 4$ watts

$V_{cc} = +12$

speaker efficiency = 80%

impedance = 8Ω.

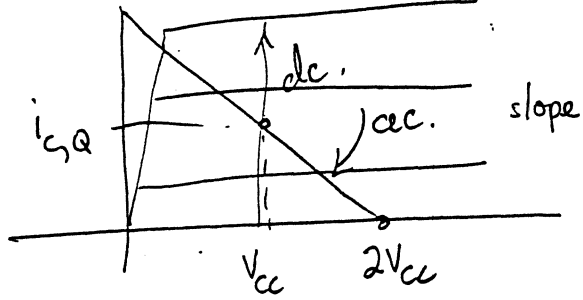
$$P_{pri} = \frac{4 \text{ watts}}{.8} = 5 \text{ watts.}$$

$$\eta = \frac{P_{AC}}{P_{DC}} = 50\% \quad \therefore P_{DC} = \frac{P_{AC}}{.5} = \frac{5 \text{ watts}}{.5} = 10 \text{ watts.}$$

$$P_{DC} = i_{c,Q} V_{cc}$$

$$10 = i_{c,Q} 12 \quad \therefore i_{c,Q} \approx 833 \text{ mA.}$$

optimum load is slope of load line.



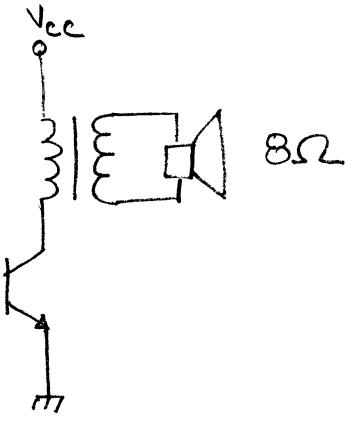
$$\text{slope} = -\frac{1}{R_L'} = -\frac{\Delta i_c}{\Delta V_{cc}} = -\frac{2\Delta i_{c,Q}}{2V_{cc}}$$

$$R_L' = \frac{V_{cc}}{\Delta i_{c,Q}} = \frac{12}{.833} = 14.4\Omega$$

$$n^2 = \frac{14.4}{8} = 1.8.$$

$n = 1.34:1$ turns ratio

Example : Class A amplifier



Design for $P_{out} = 4$ watts,
$V_{cc} = +12$ volts
speaker efficiency = 80%
impedance = 8Ω

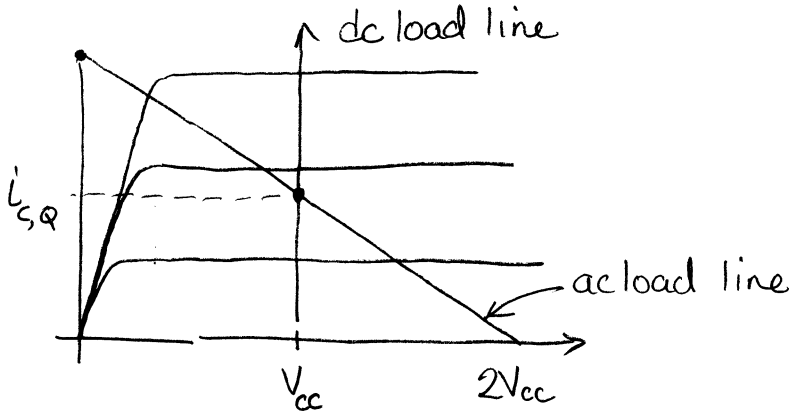
$$\text{Power}_{primary} = \frac{4 \text{ watts}}{80\%} = 5 \text{ watts}$$

$$\eta = \frac{P_{AC}}{P_{DC}} = 50\% \Rightarrow P_{DC} = \frac{P_{AC}}{50\%} = \frac{5 \text{ watts}}{.5} = 10 \text{ watts}$$

$$P_{DC} = i_{c,Q} V_{cc}$$

$$10 = i_{c,Q} 12 \Rightarrow i_{c,Q} = 833 \text{ mA}$$

The optimum load impedance for maximum ac output power is the slope of the ac load line.



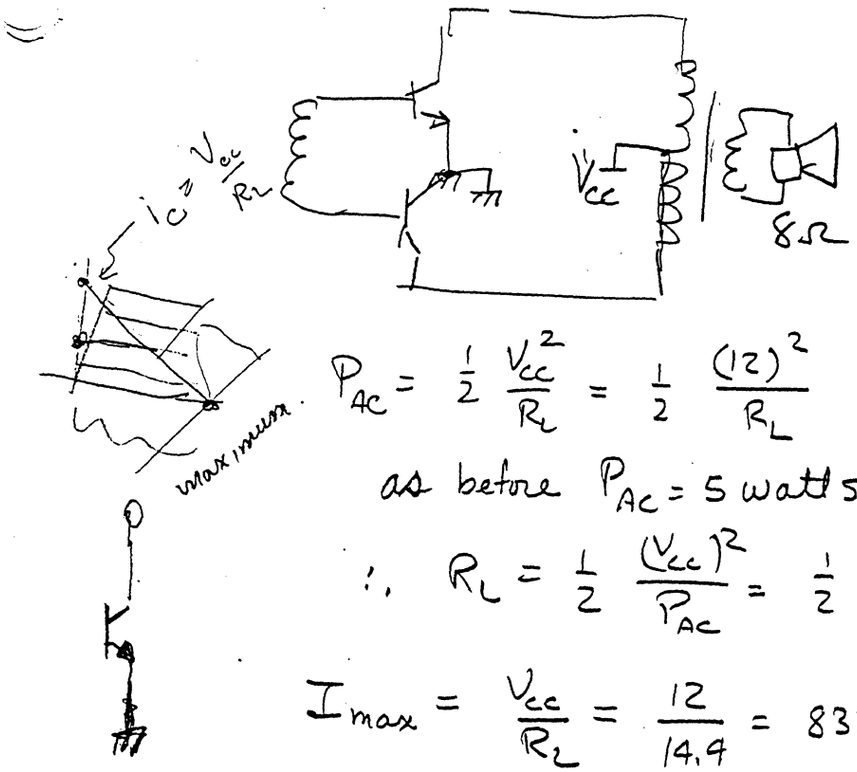
$$\text{slope} = -\frac{1}{R_L'} = -\frac{\Delta i_c}{\Delta V_{cc}} = -\frac{2\Delta i_{c,Q}}{2V_{cc}} \quad \therefore R_L' = \frac{V_{cc}}{\Delta i_{c,Q}} = \frac{12}{0.833} = 14.4\Omega$$

The transformer must then match 8Ω to 14.4Ω, or

$$n^2 = \frac{14.4}{8} = 1.8$$

The transformer must have a $n = 1.34:1$ turns ratio.

xfmr class B amplifier.



want 4 watts out
speaker = 8Ω
transformer effiency 80%
$V_{cc} = +12$

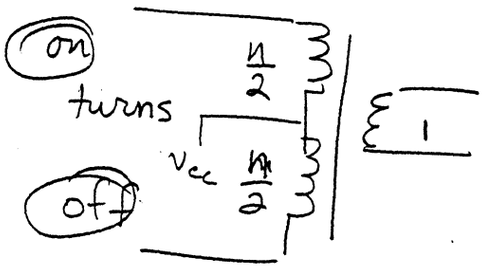
$$P_{AC} = \frac{1}{2}\frac{V_{cc}^2}{R_L} = \frac{1}{2}\frac{(12)^2}{R_L}$$ a

as before $P_{AC} = 5$ watts.

$$\therefore R_L = \frac{1}{2}\frac{(V_{cc})^2}{P_{AC}} = \frac{1}{2}\frac{(12)^2}{5} = 14.4\Omega \text{ as before.}$$

$$I_{max} = \frac{V_{cc}}{R_L} = \frac{12}{14.4} = 833\,mA \text{ as before.}$$

Transformer is different!



for on transistor $n' = \frac{n}{2}$.

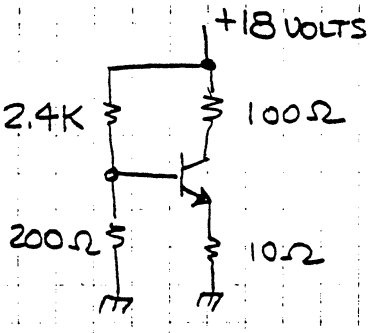
$$n'^2 = \frac{n^2}{4}$$

$$\therefore \frac{n^2}{4} = \frac{14.4}{8} = 1.8$$

$$\frac{n}{2} = 1.34.$$

$$n = 2.68. \text{ overall}$$

Problem 2



$V_{BE} = 0.6$

$\beta = 60$

(a) Calculate the no-signal power dissipated by the transistor

This is another way of saying the dc power dissipated by the transistor.

See if bias network satisfies stability criterion

$R_T = R_1 \| R_2 = 2.4K \| 200\,\Omega = 185\,\Omega$

$(\beta+1) R_E = (61)(10) = 610\,\Omega$

and since h_{ie} would add to this we can easily say that

$$R_T \ll h_{ie} + (\beta+1) R_E$$

This means that the network sets the bias

$$V_B \doteq \frac{200}{200+2400} \cdot 18 \text{ volts} = 1.385 \text{ volts}$$

$$V_E = 1.385 - 0.6 = 0.785 \text{ volts}$$

$$I_E = \frac{V_E}{10\,\Omega} = \frac{0.785}{10\,\Omega} = 0.0785 \text{ amps.}$$

$$I_C \approx I_E = 0.0785 \text{ amps.}$$

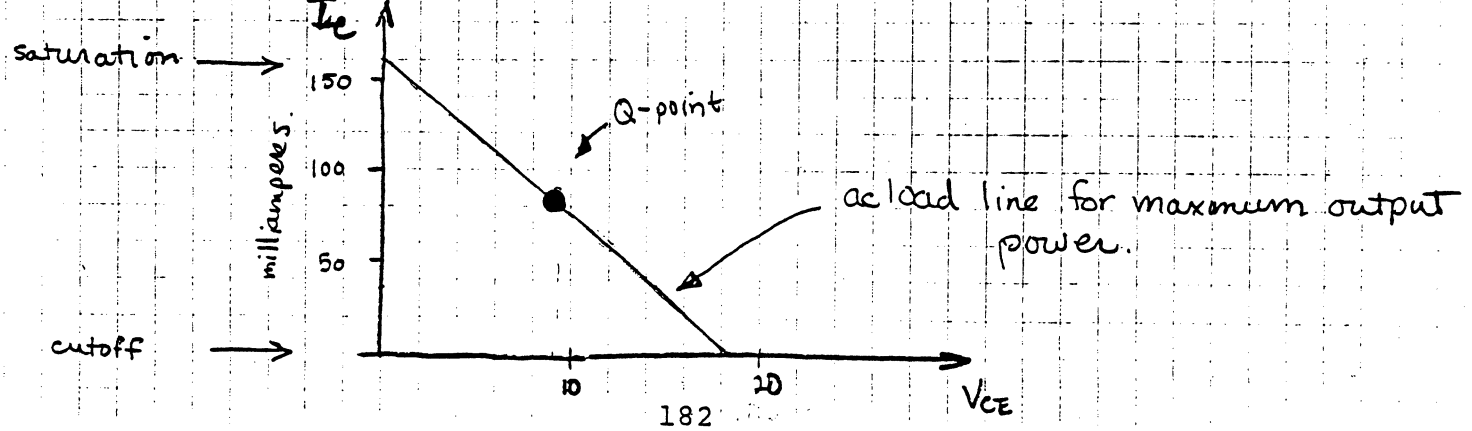
$$\therefore \quad i_{C,Q} \equiv I_C = 78.5 \text{ mA}$$

$$V_{CE,Q} = 18 - i_{C,Q}(R_L + R_E) = 18 - .0785(100+10) = 9.365 \text{ V.}$$

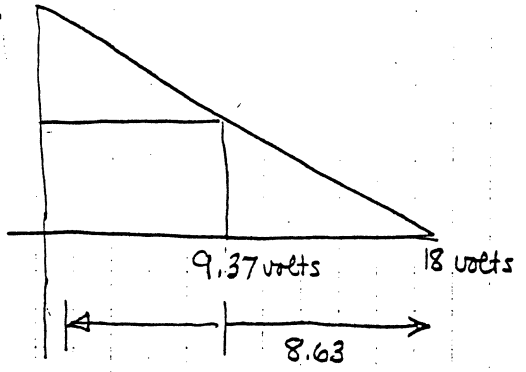
the dc power dissipated by the transistor is then

$$P_{DC,\text{transistor}} = (.0785)(9.365) = 735. \text{ milliwatts}$$

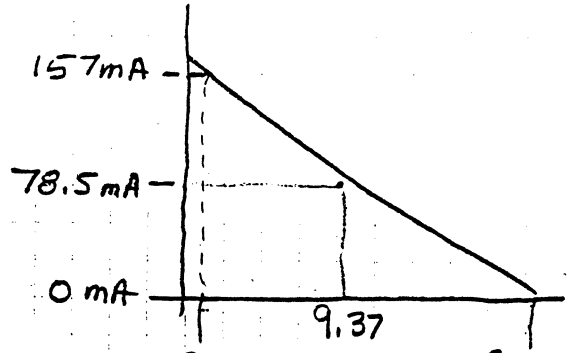
(b) The maximum ac power that can be delivered to the load before cutoff or saturation



the maximum ac voltage across the transistor can be determined from the load line.



as can be seen the maximum ac voltage is 8.63 volts peak This raises the transistor V_{CE} to 18 volts (cutoff) but not to zero (saturation), so cutoff is the limiting factor. The corresponding currents are



$9.37 - 8.63 = 0.74$ volts corresponding i_c is

$9.37 + 8.63 = 18$ volts corresponding $i_c = 0$

$(18 - 0.74)\frac{1}{110} = .157A = 157$ milliamperes

the maximum signal current is then 78.5 mA peak

the maximum ac load power is then

$$P_{AC,\,LOAD} = \left(\frac{\Delta I_c}{\sqrt{2}}\right)^2 R_L = \left(\frac{78.5}{\sqrt{2}}\right)^2 (100\,\Omega) = 308\ mW$$

(RMS)

(c) the power dissipated by the transistor when maximum ac output power occurs?

$$P_{AC,\,TRANSISTOR} = \frac{\Delta I}{\sqrt{2}}\,\frac{\Delta V_{CE}}{\sqrt{2}} = \left(\frac{78.5\,mA}{\sqrt{2}}\right)\left(\frac{8.63\,volts}{\sqrt{2}}\right) = 339m$$

(d) The power delivered by the power supply.

This is the total P_{DC}.

$$P_{DC} = V_{cc}\, i_{c,Q} = (18)(.0785) = 1.413 \text{ watts}.$$

(e) the collector efficiency of this amplifier

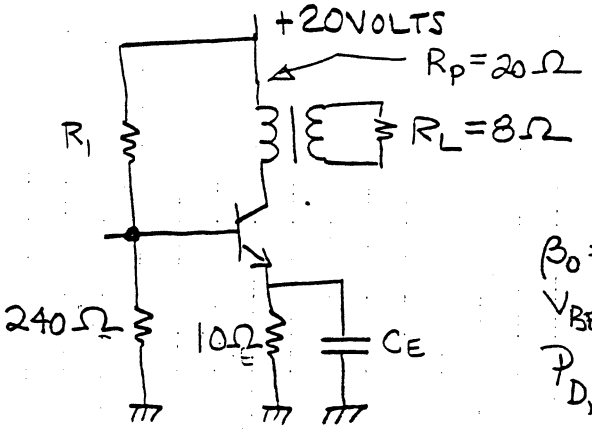
The only trick here is to recall the exact definition of η.

$$\eta = \frac{P_{AC,LOAD}}{P_{DC}} = \frac{308\,mW}{1413\,mW} = 21.8\%.$$

This is consistent with our in-class proof that

$\eta \leq 25\%$ for a resistive load class-A amp.

3.



$n:1 = 4:1$ efficiency = 80%.

$\beta_0 = 40$

$V_{BE} = 0.7$ VOLTS

$P_{D,MAX} = 2$ WATTS.

(a) The maximum power that can be delivered to the load without exceeding transistor dissipation

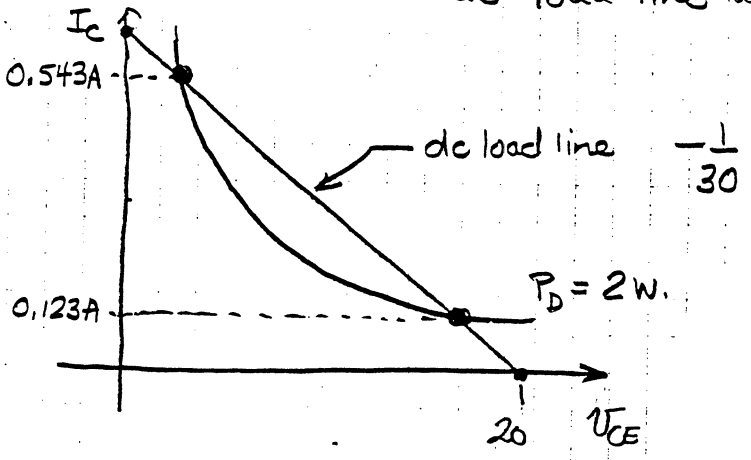
this is dc only BAD!

$$\begin{cases} P_{XSTR} = I_{CQ} V_{CQ} = I_{CQ}\left(V_{cc} - I_{CQ}(10\Omega + 20\Omega)\right) \\ P_{XSTR} = I_{CQ} V_{cc} - 30 I_{CQ}^2 \end{cases}$$

$$2.0 = I_{CQ} \cdot 20 - 30 I_{CQ}^2$$

$$I_{CQ} = \frac{+2 \pm \sqrt{4 - 4(3)(.2)}}{6} = 0.543,\ 0.123 \text{ amps.}$$

this is the intersection of the dc load line with the dissipation curve.



Either Q-point would satisfy the two watt criteria. Both will also give the same ac power out.

$$P_{LOAD} = \underbrace{\eta_t}_{\text{transformer efficiency}} \underbrace{\left(\frac{\Delta I}{\sqrt{2}}\right)^2}_{\text{rms current.}} \underbrace{n^2 R_L}_{\text{ac load transformed by transformer}}$$

$\Delta I = .123$ A both Q points

$$P_{LOAD} = 0.8 \left(\frac{.123}{\sqrt{2}}\right)^2 16.8 = 0.775 \text{ watts.}$$

This is the maximum ac power consistent with the 2-watt limit

(b) The collector current to give maximum power is given by the previous result.

We will pick $I_{CQ} = 0.123$ A since that is a lower dc current and hence higher efficiency selection

(c) the value of R_1 to give this value of collector current

$$V_E = (0.123\text{A})(10\Omega) = 1.23\text{V.}$$

$$V_B = 1.23 + 0.7 = 1.93\text{V.}$$

$$I_B = \frac{I_c}{\beta_0} = \frac{0.123}{40} = 3.08\text{ mA.}$$

$$I_{R_2} = \frac{V_B}{240\Omega} = \frac{1.93}{240} = 8.04\text{ mA.}$$

total current thru $R_1 = 11.12$ mA.

$$R_1 = \frac{20 - 1.93}{11.12\text{mA}} = 1.625\text{K}\Omega$$

(d) the collector efficiency

$$\eta_C = \frac{P_{LOAD}}{P_{DC}} = \frac{0.775 \text{ watts}}{(0.123\text{A})(20 \text{ volts})} = \frac{0.775}{2.46} = 31.5\%$$

which is consistent with our class results.