PHASE-LOCKED LOOPS[1]

Phase-locked loops (PLLs for short) go back to 1932 when deBellescizi used a tube-based phase-locked loop to synchronously demodulate radio signals. Today, PLLs are used in devices ranging from coherent analog receivers and carrier tracking filters to horizontal and vertical synchronization circuits in television sets. For those that are more digitally inclined, PLLs are also used for frequency synthesis, bit synchronization in digital data transmission, coherent FSK demodulation, and the like.

SYSTEM BEHAVIOR

We will attempt to describe the system performance in terms of observable and measurable, i.e. engineering, quantities. There are two distinct modes of phase-locked loop behavior - ACQUISITION and TRACKING. In the ACQUISITION mode, the PLL is trying to lock onto a signal; in the TRACKING mode the PLL is locked onto a signal and will retain that lock through phase and frequency variations of the signal. In general, at the basic circuits/systems level, we will be concerned with the tracking (the phase-locked) mode and over what range of frequency and phase variation the PLL can track the signal. The basic behavior of the PLL can be related to measurable steady-state quantities at each stage in the PLL. For steady-state analysis sophisticated feedback theory is NOT needed. However, before we can understand loop operation we must become familiar with the individual loop components.

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[1]The material in this section follows the development of Paul H. Young, Phase-Locked Loops: A Tutorial, Session 3548, 1984 American Society for Engineering Education Annual Conference Proceedings, p.1256-1261, also P.H.Young, Electronic Communications Techniques, Charles Merrill Publishers, Chapter 10, 1985.

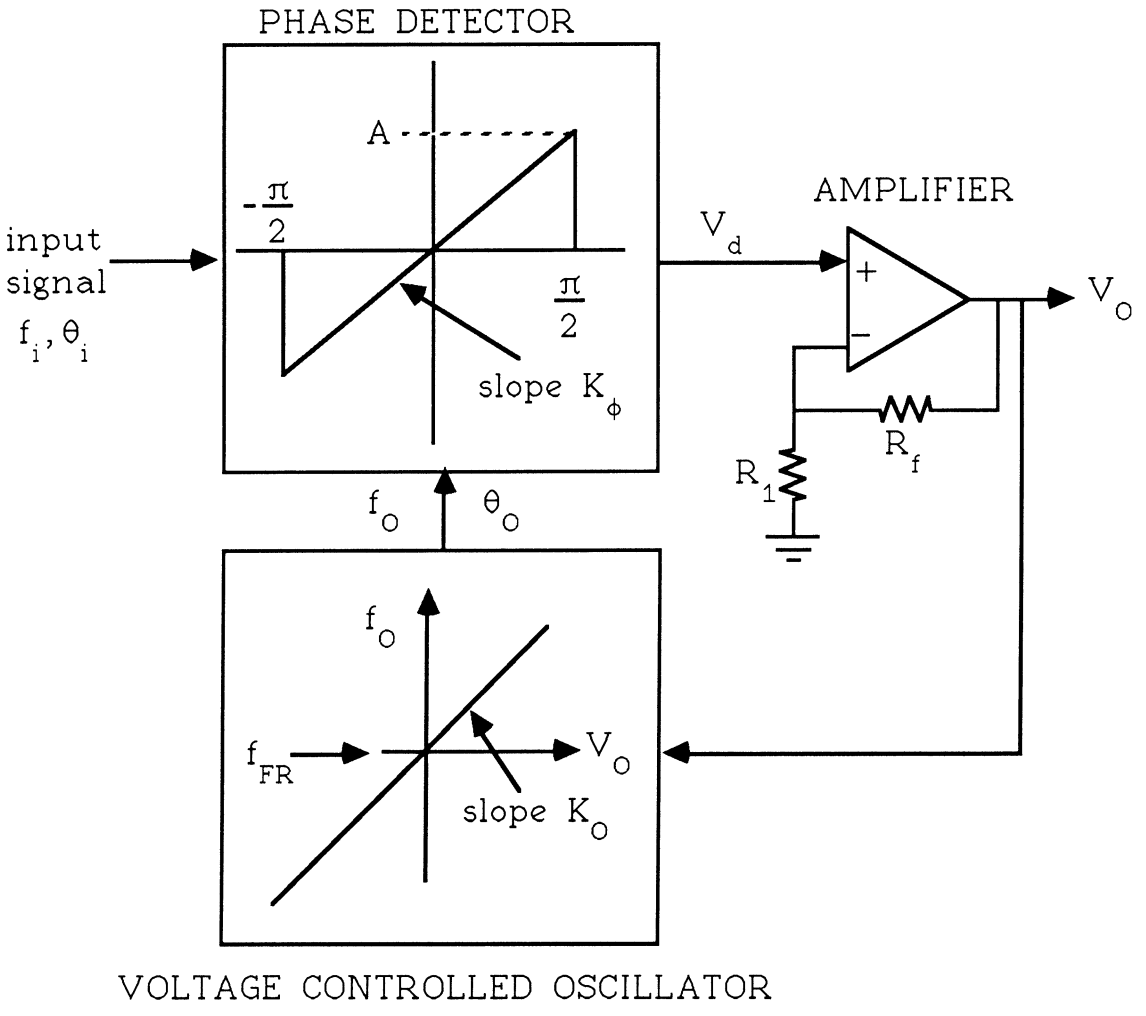


Figure 1 – Basic Phase Locked Loop Components

LOOP COMPONENTS

The PLL shown in Figure 1 consists of a phase comparator (detector), an error signal amplifier (a differential amplifier) and a voltage controlled oscillator (VCO).

The phase detector (ϕ detector) is a dc coupled mixer. In general, this behaves exactly like any other mixer producing sum and difference frequency components in its output except that its inputs and output can also have dc components. In PLL applications we are primarily concerned with the difference out. Assume that the input frequencies to the phase detector are different, the mixer will then produce sum and difference frequencies. Call the two different input frequencies f_1 and f_0. The sum frequency $f_0 + f_1$ can be removed from the mixer

output by a low-pass filter leaving a sinusoidal signal at the difference frequency $\Delta f = |f_0 - f_1|$. If the input frequencies are equal, the difference frequency output will be a dc voltage proportional to the phase difference between the input signals, i.e. $\theta_0 - \theta_1 = \theta_e$. This can be proven by simple trigonometry. The magnitude of the dc mixer output voltage (for two identical frequencies input) will be $v_d = K_\phi \theta_e$ where K_ϕ is the gain slope of the phase detector curve at the operating point, θ_e is the phase difference between the two signals and v_d is the filtered dc (in this case) mixer output voltage. For the phase detector shown in Figure 1, the gain is constant between $-90°$ and $+90°$ and is

$$K_\phi = \frac{A}{1/2\pi} = \frac{2A}{\pi} \text{ volts/radian} \qquad (1)$$

The error signal amplifier shown in Figure 1 is a non-inverting voltage amplifier (constructed using an operational amplifier) with a gain of

$$K_A = 1 + \frac{R_f}{R_1} \qquad (2)$$

The voltage-controlled oscillator (VCO) frequency is controlled by the input voltage V_O – the filtered output of the mixer. For simplicity, the operational amplifier is assumed capable of bipolar output and is ideal with no input voltage offset. The VCO is assumed to be at its free-running frequency f_{FR} when $V_O = 0$. As shown in Figure 1, the VCO characteristic is linear with slope K_O (Hz/volt) so that any change in V_O will produce a VCO output frequency change Δf_O.

ACQUISITION

Initially, the VCO is free-running at f_{FR}. A signal at frequency f_1 is input to the phase detector. If $f_1 = f_{FR}$ then the loop is instantaneously locked and $V_O = 0$. The definition of "locked" is that $f_O = f_1$ and the VCO frequency tracks f_1 exactly in the steady-state; note that there can be a phase error between f_O and f_1 in the locked state.

If f_1 is not equal to f_{FR} and the difference between these two frequencies is within the loop bandwidth, the resulting VCO

input signal will be a (usually sinusoidally) varying signal at the difference frequency. If the resulting VCO input signal $V_O = V_d K_A$ is large enough to cause the VCO to shift to f_1 then lock-up (acquisition) will occur. If the difference frequency is outside the loop bandwidth, acquisition may still occur by another process known as "pull-in."

Once acquisition occurs, the loop is locked and operating in the tracking mode.

TRACKING (LOCKED)

When the PLL is locked, $f_O = f_1$ and the VCO input voltage required to deviate the VCO from its free-running frequency is given by

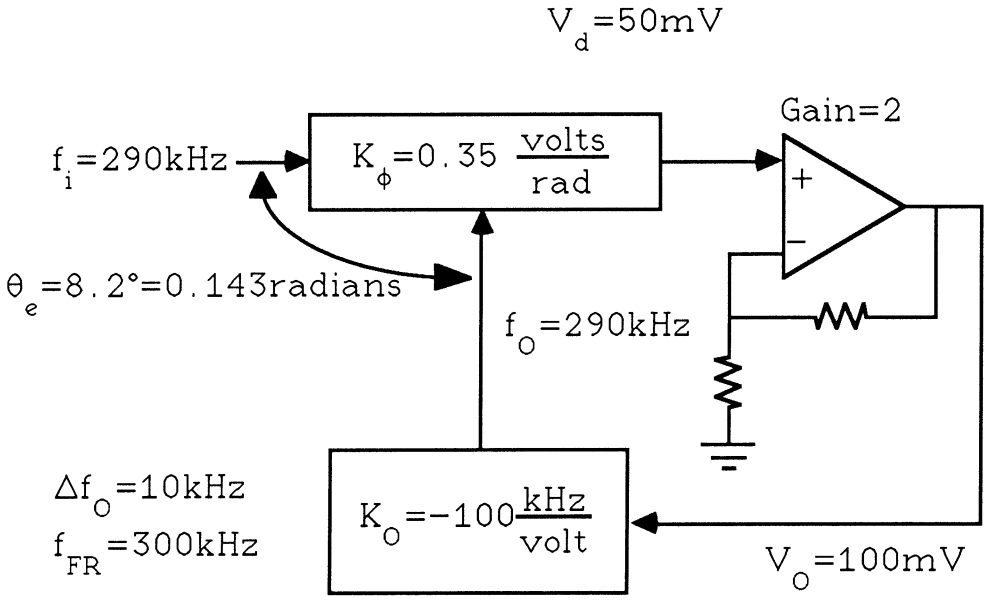
$$V_O = \frac{f_1 - f_{FR}}{K_O} = \frac{\Delta f}{K_O} \qquad (4)$$

But $V_O = K_A V_d$ so that the phase detector must produce $V_d = \Delta f / K_O K_A$. The phase detector can do this if its input is

$$\theta_e = \frac{V_d}{K_\phi} = \frac{\Delta f}{K_O K_A K_\phi} \qquad (5)$$

The phase difference between the VCO and the input signal provides the loop error signal that is required to keep the VCO tracking f_1. θ_e is called the STATIC (steady-state) PHASE ERROR and $K_L = K_O K_A K_\phi$ is called the loop gain. This is a very important result – the PLL VCO is at the exact same frequency as the input signal but there is a phase difference between the two signals. Equation (5) with loop gain K_L yields the fundamental relationship for the steady-state PLL

$$\theta_e = \frac{\Delta f}{K_L} \qquad (6)$$



$$K_L = K_O K_A K_\phi = (0.35 \frac{\text{volts}}{\text{rad}})(2)(-100 \frac{\text{kHz}}{\text{volt}}) = -70 \frac{\text{kHz}}{\text{rad}}$$

Figure 2 – Commercial PLL (NE565) in Tracking Mode Locked to 290 kHz Input Signal

To illustrate the utility of this model Figure 2 shows typical loop parameters for the most popular PLL integrated circuit, the NE 565. The voltage values that should be measured at each point in the system for $\Delta f = 10$ kHz are also shown. The analysis starts at the VCO with the question "What must V_O be in order to keep $f_O = f_1$?" Once you have answered this question using $\Delta f = K_O V_O$, V_d is determined and the static phase error is specified. Basically, you must evaluate Equation (6) every time you solve a PLL problem.

HOLD-IN RANGE AND LOSS OF LOCK

Once locked, the VCO tracks slow changes in f_{in} and $V_O(t)$ is an exact replica of f_1 deviations as long as Δf remains well within the loop's bandwidth and the system remains linear. This is the basis for PLLs in linear FM demodulation, i.e. stereo tuners. Given the modulation waveform $m(t)$ and the FM peak deviation, $V_O(t)$ can be determined from Equation (4).

The hold-in range is the total frequency range over which the loop can maintain phase lock. It can be predicted from the loop component characteristics. Typically, the operational amplifier saturation level and the VCO control range far exceed phase detector limitations. Notice the particular phase detector characteristic of Figure 1. This triangular phase detector characteristic is typical of phase detectors implemented with EXCLUSIVE-OR gates. A similar characteristic, but with a sinusoidal curve, is typical of analog multipliers. A saw-tooth characteristic with a θ_e range of up to 2π can be realized with edge-triggered flip-flops.

As the astute reader might note, PLLs can incorporate digital integrated circuits which makes PLLs ideal candidates for an all-digital implementation. In fact, all-digital PLLs are available commercially (the CD4046) and software PLLs have been implemented.

The total range over which the loop can maintain phase lock is limited to the maximum phase detector output, $V_d(max) = \pm A$. Thus, a frequency variation for which the loop error θ_e exceeds $\pm\pi/2$ will result in loss of lock.

From Equation (6) with $\Delta f_H = f_i(max) - f_i(min)$

$$\Delta f_H = \pi K_L \qquad (7)$$

is the total Hold-In frequency range. The loop of Figure 2 will maintain lock for input frequencies down to 190 kHz and up to 410 kHz before loss of lock occurs. Also, noise in the loop or ringing in an under-damped second-order loop that causes V_O to exceed $\pm 110\,kHz/K_O = \pm 1.1$ volts peak, will cause a loss of lock until the transient subsides to within the acquisition range of the system.

FREQUENCY RESPONSE AND BANDWIDTH

The PLL of Figure 3 will be used to illustrate the frequency response and dynamic behavior for a typical application – demodulation of analog FM and digital FSK (Frequency Shift Keyed) signals. The results have wide applications in PLL design and analysis.

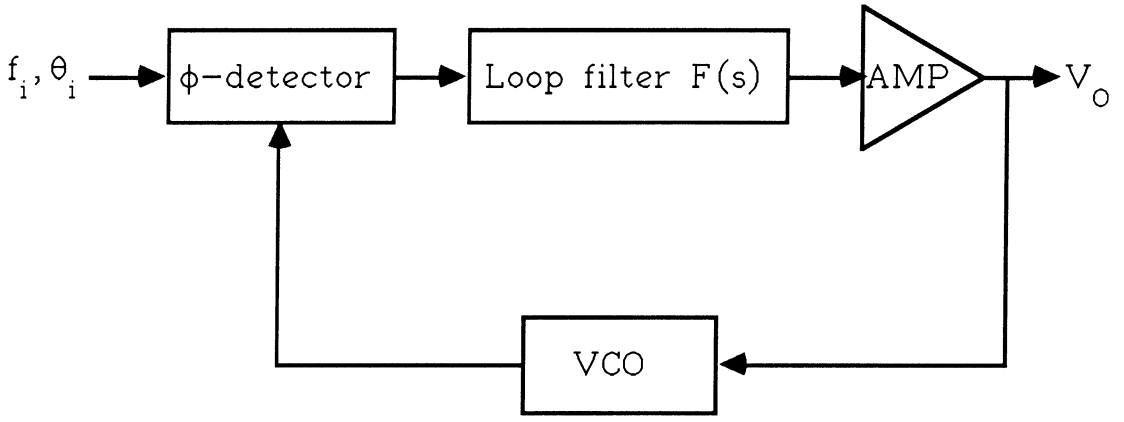


Figure 3 – PLL Block Diagram

(some typical loop parameters are shown)[2]

When used as a demodulator, the PLL must be designed for an appropriate frequency response and bandwidth. The bandwidth and response of the loop to sudden changes of the input frequency or phase (step response) are determined by the use of Bode plots and well established reference data and graphs. Such simple graphical techniques allow the design of phase-locked systems including the loop compensation necessary for specific applications.

The Bode plot of the open-loop gain is based upon the fact that the VCO transfer function (see Figure 1) is that of an integrator[3]. The phase detector and amplifier are presumed to be broadband for at least an order of magnitude above the uncompensated loop bandwidth.

2

[3]The VCO frequency can be written as

$$f_O = \frac{1}{2\pi} \frac{d\theta_O(t)}{dt}$$

Consequently.

$$\theta_O(t) = 2\pi \int f_O dt = 2\pi f_O t + \theta_O$$

for a constant f_O. For a linear VCO characteristic, $\Delta f_O = K_O V_O(t)$, $\Delta f_O = K_O V_O(t)$ and the instantaneous VCO phase is

$$\theta_O(t) = 2\pi f_O t + 2\pi K_O \int V_O(t) dt + \theta_O$$

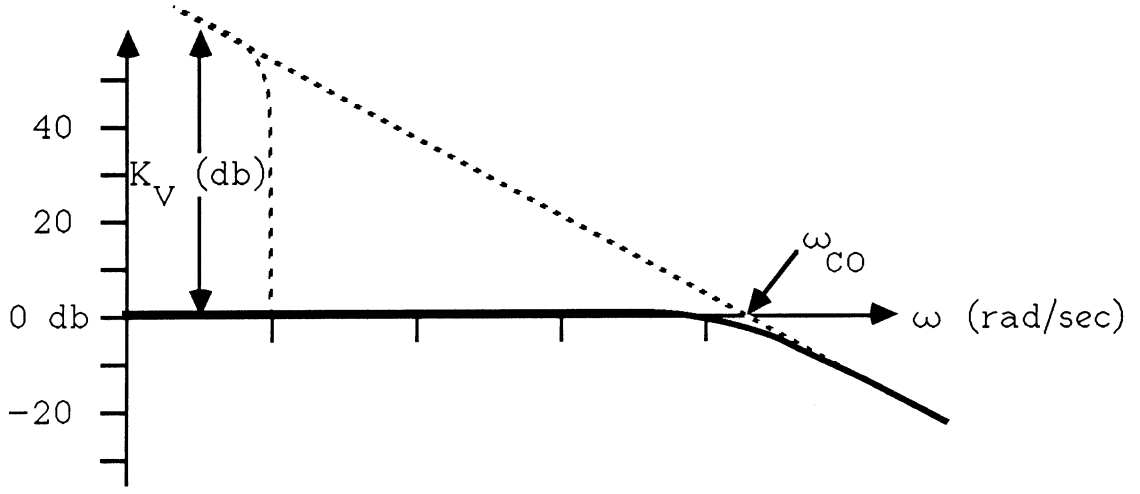


Figure 4 – Open-loop (dashed line) and Closed-Loop Bode Plot for Uncompensated Loop

Figure 4 shows the open-loop (dashed) and closed loop frequency response for the uncompensated PLL of Figure 3. The required loop gain for a given application is determined primarily from the allowable steady-state error based upon hold-in range and minimum bandwidth. The closed loop frequency response indicates that, compared to a typical voltage amplifier feedback system, there is 100% feedback for the PLL. The closed loop response could also be labeled $V_O(\omega)$ since it follows the relative output amplitude versus frequency for the input signal frequency modulated by a sinusoid of frequency ω_O. Notice that the sinusoidal response is flat for low frequencies, is down 3 db at ω_{CO} (the loop crossover frequency), and rolls off at 6 db/octave for high loop frequencies. The uncompensated PLL is seen to behave much like a 1st order low-pass filter that tracks an input carrier – hence, its application as a "tracking filter." Finally, you must realize that the VCO will track frequencies above as well as below its free-running frequency so, for noise bandwidth considerations, the Bode plots of Figure 4 are one-sided only.

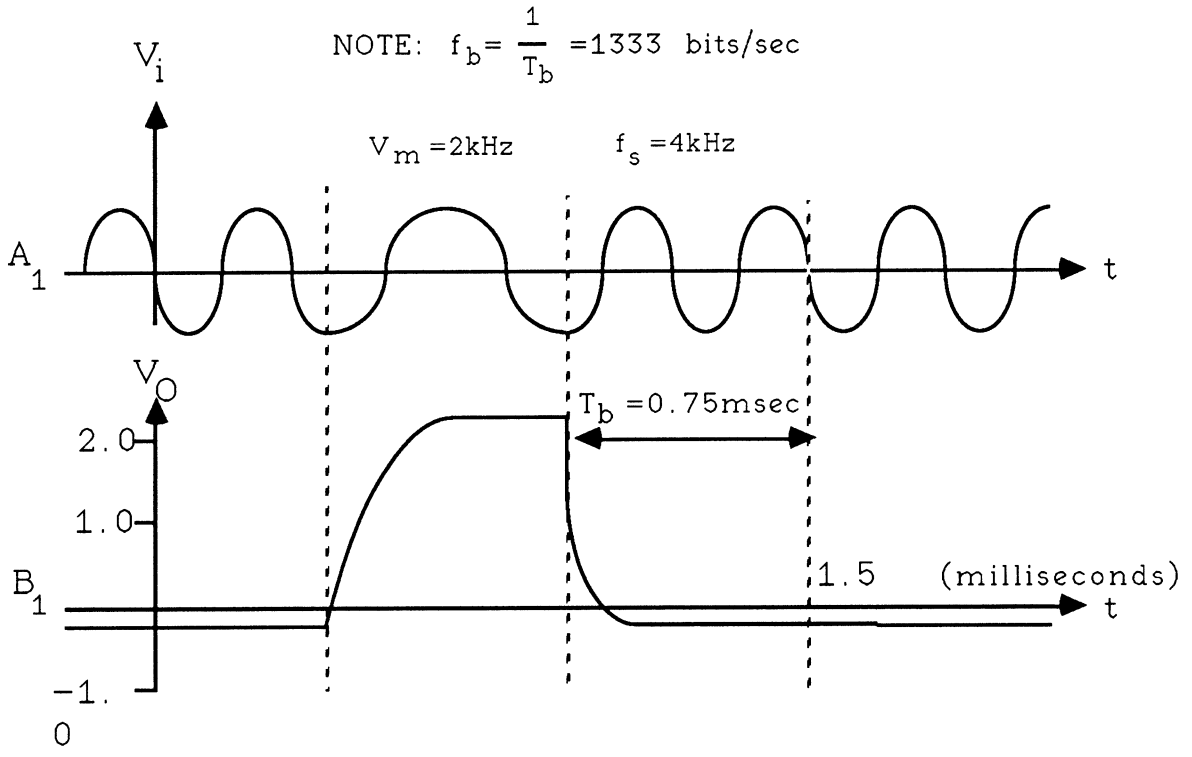
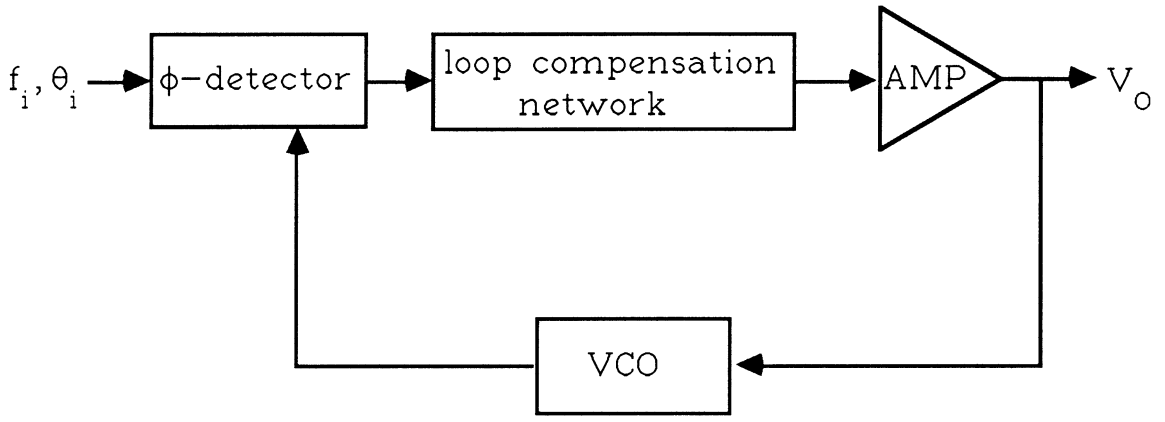


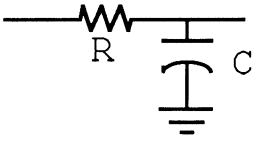
Figure 5 - Frequency Shift Key PLL Demodulation

A. FSK Input to PLL B. Demodulated Output

The response of the uncompensated PLL of Figure 3 to a digital FSK signal is shown in Figure 5. Figure 5(a) shows the 1333 bit/sec baud rate FSK signal and Figure 5(b) shows the demodulated output $V_O(t)$. Since the VCO can be used to modulate such an FSK signal, the PLL integrated circuit is usually a vital component of data MODEMs. Notice that in Figure 5(b) the first-order low-pass filter type of response to the input frequency step change. The time constant is $\tau = 1/K_V$ because the closed loop 3 db frequency and open loop crossover frequencies are both equal to K_V for the uncompensated PLL.



A. Lag compensation network



B. Lead-lag compensation network

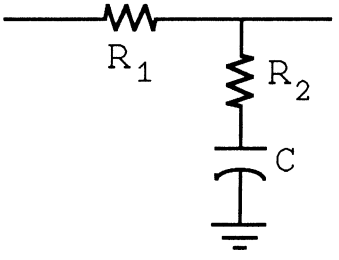


Figure 6 – Block Diagram of the Compensated PLL

For many applications, the first order system response is inadequate or undesirable. In this case, the loop can be made second-order by inserting an RC lag or lead-lag network at the output of the phase detector. These compensation networks (filters) are shown in Figure 6. Also shown in Figure 6 is the block diagram for the compensated PLL. For lag compensation, the location of the RC corner frequency,

$$\omega_C = \frac{1}{RC} \qquad (9)$$

determines the actual amount by which the phase margin (PM) is reduced, thus reducing the loop damping factor δ. The RC corner frequency and phase margin are related by

$$\text{Phase margin} = 180° - [90° + \tan^{-1}(\frac{\omega_{CO}}{\omega_C})] \quad (10)$$

where ω_{CO} is the open-loop crossover frequency (See Figure 7) and the 90° represents the phase lag due to the integrating effect of the VCO.

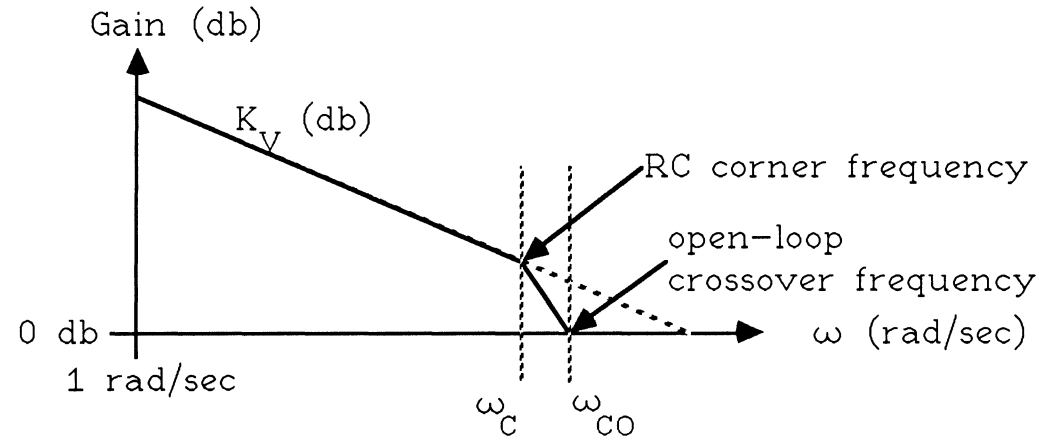


Figure 7 – Bode Plot for Lag Compensated PLL

The loop damping factor can be determined from the universal second-order system curves of Figure 8 using the calculated value of phase margin, or it can be calculated directly from

$$\delta = \tfrac{1}{2}\sqrt{\frac{\omega_C}{K_V}} \quad (11)$$

when lag compensation is used. Equation (10) gives the Bode asymptotic approximation to the phase margin. The actual phase margin is greater than that calculated and is determined from the closed loop crossover frequency.

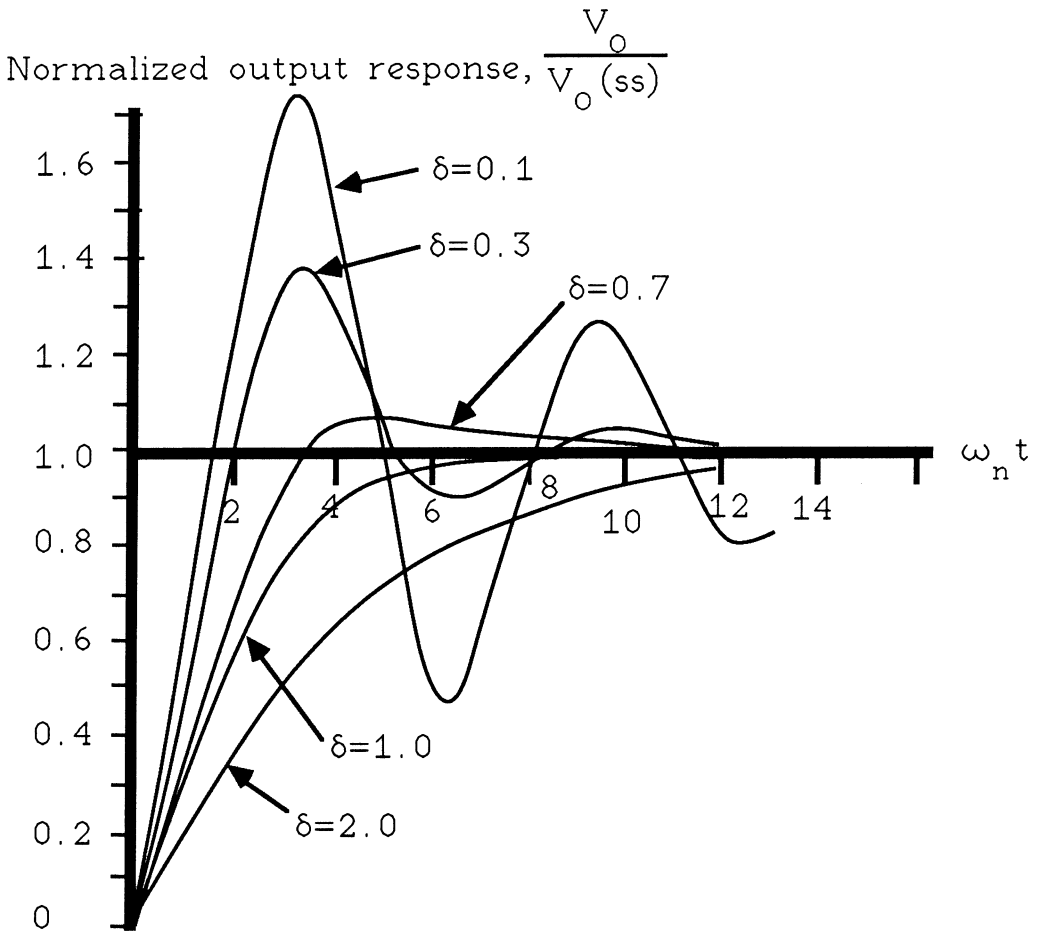


Figure 8 – Second-order loop response to step-change in input frequency.

Equation (11) clearly indicates how loop damping is determined by the relative relationship of ω_C to the uncompensated loop crossover frequency. As determined from Equation (11), by setting the RC time constant so that ω_C is one octave above K_V, the loop will be compensated for $\delta = 0.707$. This is optimum damping for most PLL applications.

Loop compensation changes the first-order PLL system to a second-order system. The closed loop frequency response and bandwidth are no longer as simple as that shown in Figure 4. For second-order systems, the universal curves of Figure 9 can be used.

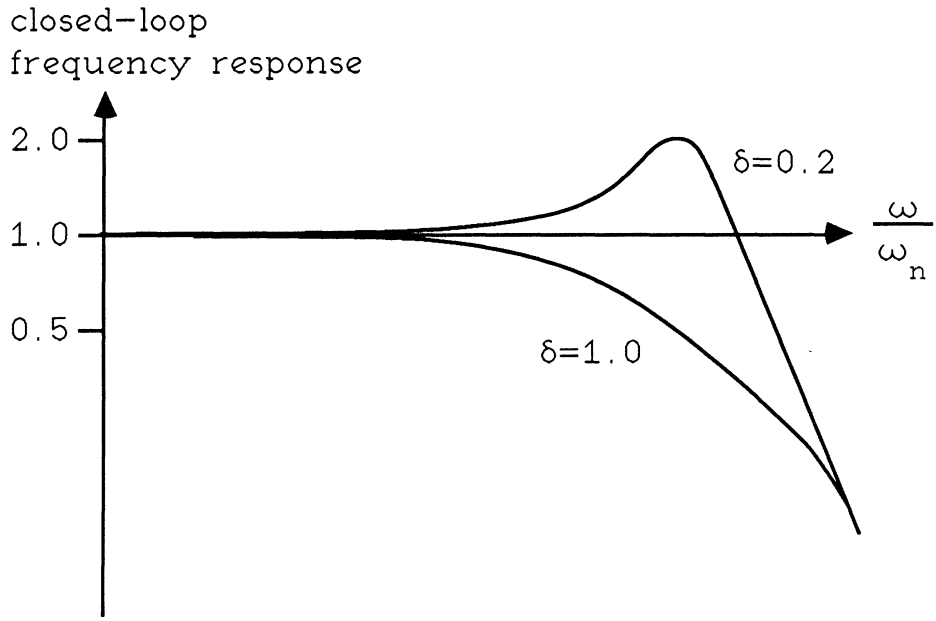


Figure 9 – Closed-loop response of Second Order PLL

When using the curves of Figures 8 and 9, the time axis must be de-normalized for the particular loop dynamics by the use of ω_n, the undamped natural frequency of the loop. This is calculated for the PLL with lag compensation from

$$\omega_n = \sqrt{\omega_c K_v} \qquad (12)$$

Equation (12) indicates that the undamped frequency of the loop oscillations is the geometric mean of the loop filter corner frequency and the loop gain (in radians/second).

The FM/FSK demodulator of Figure 3 with a lag compensation network consisting of $R = 3\,k\Omega$ and $C = 0.068\,\mu F$ was analyzed using the techniques described above. Figure 10 shows the open and closed loop frequency response. Figure 11 shows the step response for input frequency shifts of 3.5 kHz representing FSK demodulation of 1,0 bits being sent at a baud rate of 470 bits/second.

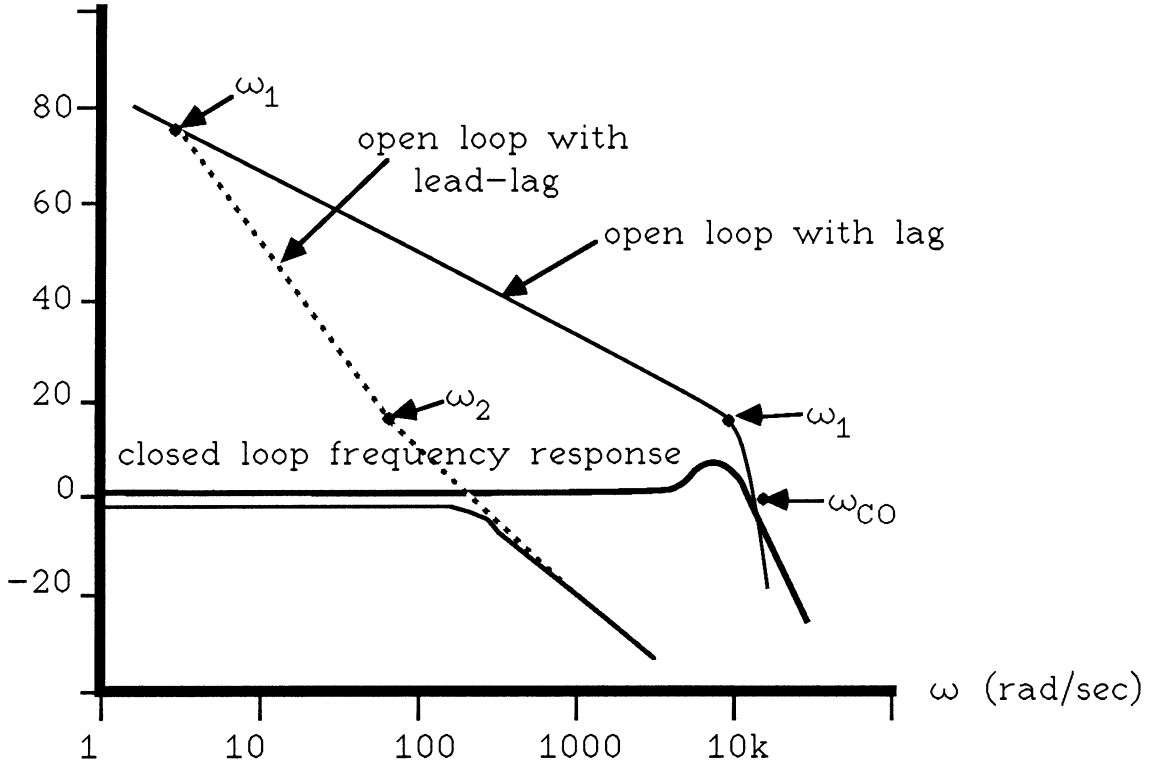


Figure 10 – Bode plot of Figure 3 loop with two types of frequency compensation

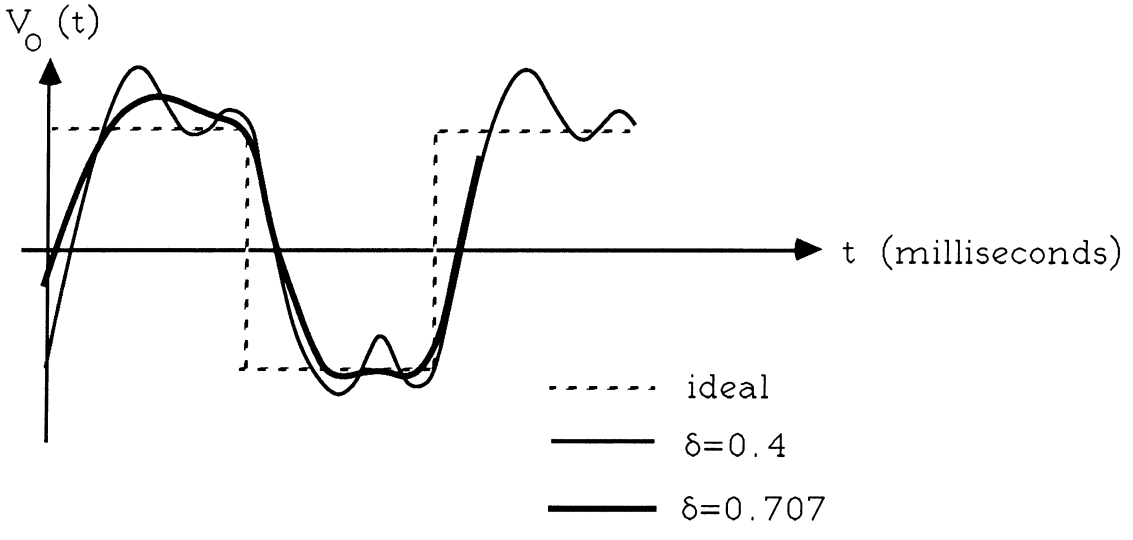


Figure 11 – Response of second-order loop to input frequency step.

The response for $\delta = 0.707$ is also shown as the dotted line in Figure 11. Note that the horizontal axis of Figure 8 is

denormalized with Equation 12 and the vertical axis is denormalized with

$$V_{O(\text{steady state})} = \frac{\Delta f}{K_O} \qquad (13)$$

Figure 8 also allows for the determination of percentage overshoot and settling time.

LEAD-LAG COMPENSATION

Lag compensation allows the designer to set the loop gain and damping (amount of overshoot, ringing and settling time) independently. However, the system bandwidth is fixed without alteration once the above parameters are set.

If a lead-lag network is used for loop compensation, all three system parameters – loop gain, damping and bandwidth – can be set independently. Resistor R_2 with capacitor C of Figure 6b provides a "zero" of leading phase shift that improves the phase margin at the same time that the loop (one-sided) bandwidth is fixed at B in Figure 10.

The procedure for lead-lag compensation for $\delta = 0.707$ is as follows: (refer to the dotted lines in Figure 10). The uncompensated open loop Bode plot is made. Then the desired bandwidth B is marked on the 0 db axis. A 6 db/octave line is drawn through the bandwidth point and a point $\omega_2 = \frac{1}{2}B$ is placed on this line at the + 6 db open-loop gain. This will set the damping factor to $\delta = 0.707$ for a high gain loop. A -12 db/octave line is drawn through ω_2 until it intersects the uncompensated Bode plot line at ω_1. With capacitor C arbitrarily chosen, R_2 is determined from

$$\omega_2 = \frac{1}{R_2 C} \qquad (15)$$

and

$$\omega_1 = \frac{1}{(R_1+R_2)C} \qquad (16)$$

will yield R_1 where

$$R_1 = \frac{1}{\omega_1 C} - R_2$$

The loop is thus compensated for $\delta = 0.707$ with bandwidth B and loop gain K_V. The exact values for δ and ω_n (used to denormalize the universal second-order response curves), for the lead-lag compensated PLL are

$$\delta = \tfrac{1}{2}\omega_n\left(\frac{1}{\omega_2} + \frac{1}{K_V}\right) \qquad (17)$$

and

$$\omega_n = \sqrt{\frac{K_V \omega_1 \omega_2}{\omega_1 + \omega_2}} \qquad (18)$$

or for $\omega_2 >> \omega_1$, $\omega_n = \sqrt{K_V \omega_2}$

AN-535
Application Note

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

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Applications Engineering

The fundamental design concepts for phase locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.

MOTOROLA Semiconductor Products Inc.

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.

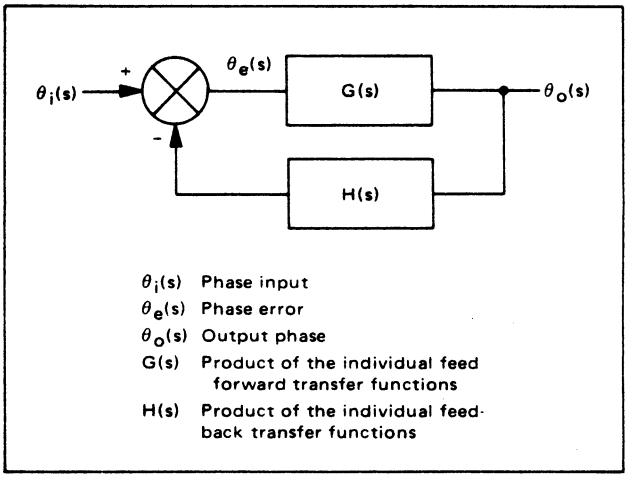

FIGURE 1 – Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

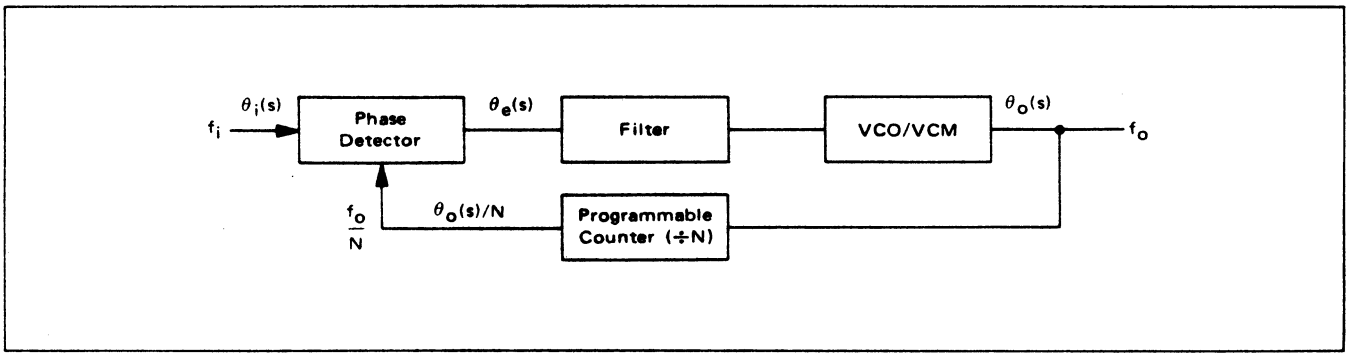

FIGURE 2 – Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \tag{3}$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \qquad G(s)\,H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\,H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.
Example:

$$G(s)\,H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)\,H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

therefore

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

ERROR CONSTANTS

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to o} [s\,\theta_e(s)] \tag{10}$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\,\theta_i(s) \tag{11}$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:} \qquad \theta_i(t) = C_p \quad t \geqslant 0 \tag{12}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_p}{s} \tag{13}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity:} \qquad \theta_i(t) = C_v t \quad t \geqslant 0 \tag{14}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_v}{s^2} \tag{15}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputing a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:} \qquad \theta_i(t) = C_a t^2 \quad t \geqslant 0 \tag{16}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{2\,C_a}{s^3} \tag{17}$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \quad G(s)\,H(s) = \frac{K}{s(s+a)} \tag{18}$$

$$\text{Type 2} \quad G(s)\,H(s) = \frac{K(s+a)}{s^2} \tag{19}$$

$$\text{Type 3} \quad G(s)\,H(s) = \frac{K(s+a)(s+b)}{s^3} \tag{20}$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1 + \frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s+a)C_p}{(s^2 + as + K)} \tag{21}$$

$$\theta_e(t=\infty) = \lim_{s \to o}\left[s\left(\frac{s+a}{s^2 + as + K}\right)C_p\right] = 0 \tag{22}$$

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

TABLE I – Steady State Phase Errors for Various System Types

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table I the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

STABILITY

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 - The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞). Where K is loop gain.

Rule 2 - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 - The root locus contour is bounded by asymptotes whose angular position is given by

$$\frac{(2n+1)}{\#P - \#Z}\pi;\ n = 0, 1, 2, \ldots \tag{23}$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 - The intersection of the asymptotes is positioned at the center of gravity C. G.

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \tag{24}$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 - On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 - Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \tag{25}$$

Again where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\,H(s) = \frac{K}{s(s+4)} \tag{26}$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = –4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

$$\frac{2n+1}{2}\pi = \begin{cases} \frac{\pi}{2} & \text{for } n = 0 \\ \frac{3\pi}{2} & \text{for } n = 1 \end{cases} \tag{27}$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4-0)-(0)}{2-0}$$

$$s = -2 \tag{28}$$

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

$$\text{C.E.} = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \tag{29}$$

Now solving for K yields

$$K = -s^2 - 4s \tag{30}$$

Taking the derivative with respect to s and setting it equal to zero then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \tag{31}$$

$$\frac{dK}{ds} = -2s - 4 = 0 \tag{32}$$

or

$$s = -2 \tag{33}$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form[2]

$$s^2 + 2\zeta\,\omega_n s + \omega^2_n \tag{34}$$

where the damping ratio $\zeta = \text{Cos}\,\phi\ (0^o \leqslant \phi \leqslant 90^o)$ and ω_n is the natural frequency as shown in Figure 3.

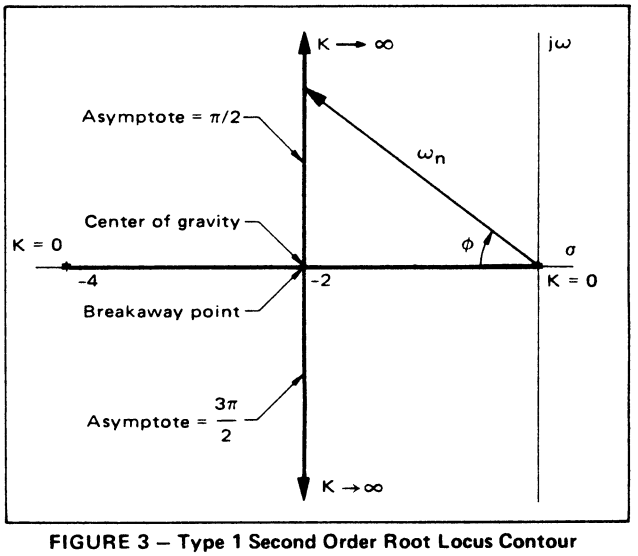

FIGURE 3 – Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

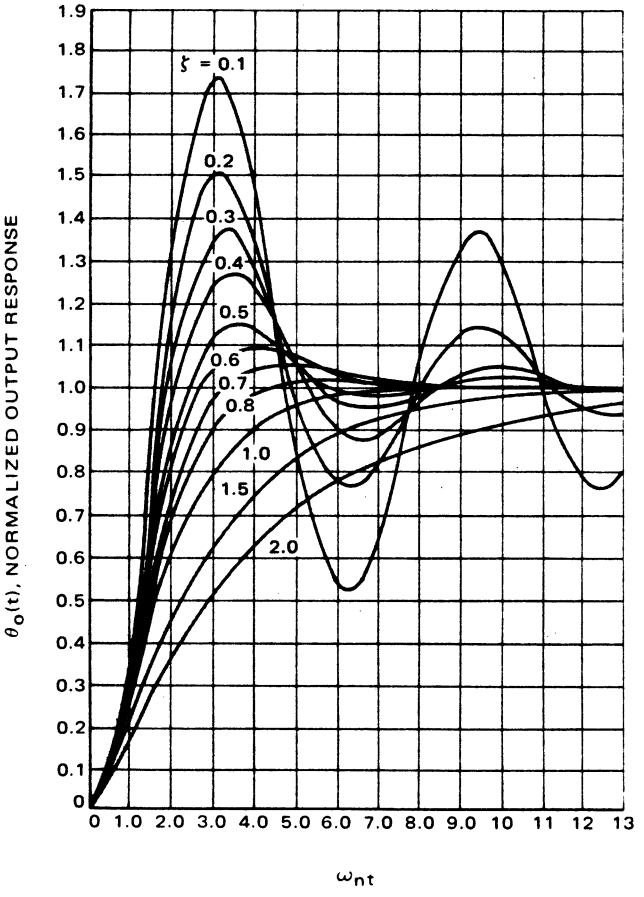

FIGURE 4 – Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ζ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ζ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\zeta = 0.5$
error $< 10\%$
for $t > 1$ ms

From $\zeta = 0.5$ curve the error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \tag{35}$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \tag{36}$$

ζ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form

$$G(s)\,H(s) = \frac{(s+a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at s = -a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = -2a.

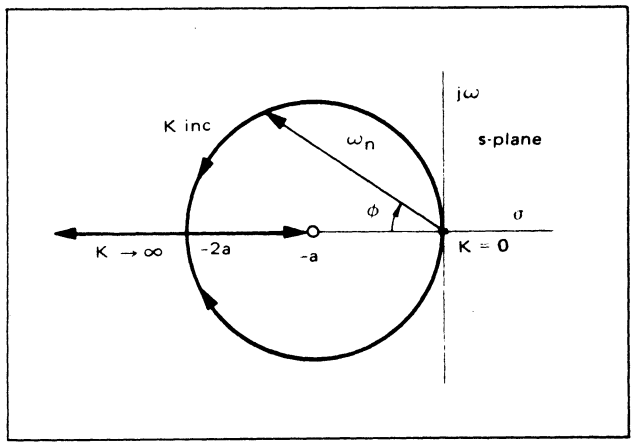

FIGURE 5 – Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required ω_n can be determined by the use of the graph when ζ and the lock up time are given.

BANDWIDTH

The -3 dB bandwidth of the PLL is given by

$$\omega_{-3\,dB} = \omega_n\left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by

$$\omega_{-3\,dB} = \omega_n\left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

PHASE-LOCKED LOOP DESIGN EXAMPLE

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach

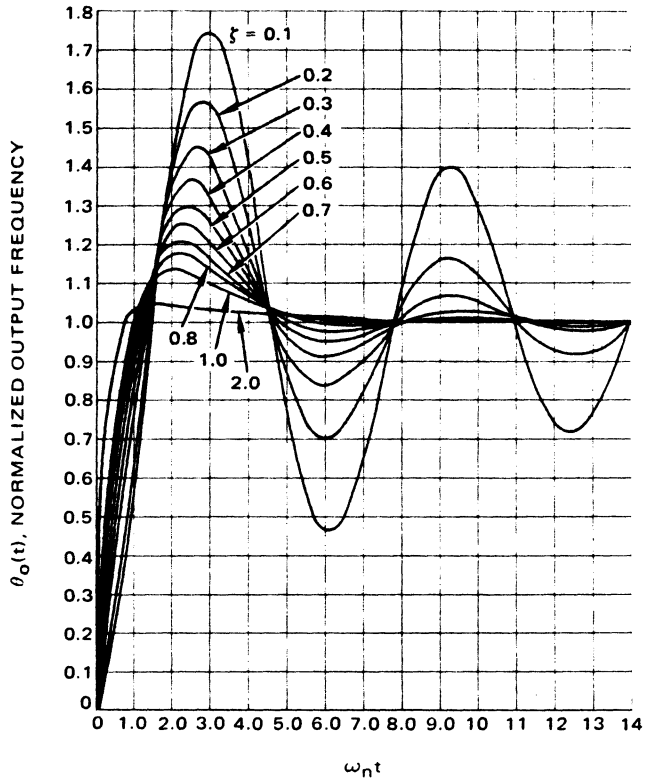

FIGURE 6 – Type 2 Second Order Step Response

to these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output frequency	2.0 MHz to 3.0 MHz
Frequency steps	100 kHz
Phase coherent frequency output	–
Lock-up time between channels	1 ms
Overshoot	< 20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p\,K_f\,K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

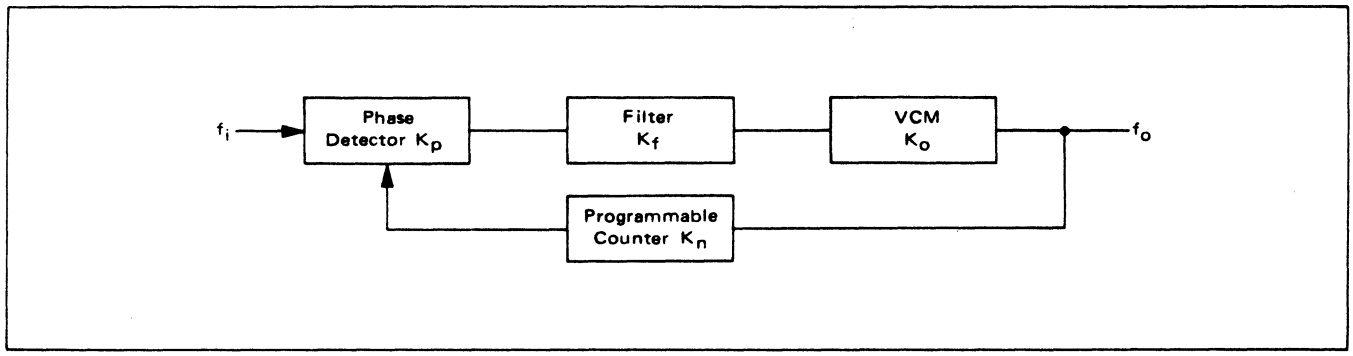

FIGURE 7 – Phase Locked Loop Circuit Parameters

The programmable counter divide ratio K_n can be found from Equation 3.

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2\text{ MHz}}{100\text{ kHz}} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3\text{ MHz}}{100\text{ kHz}} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100 pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

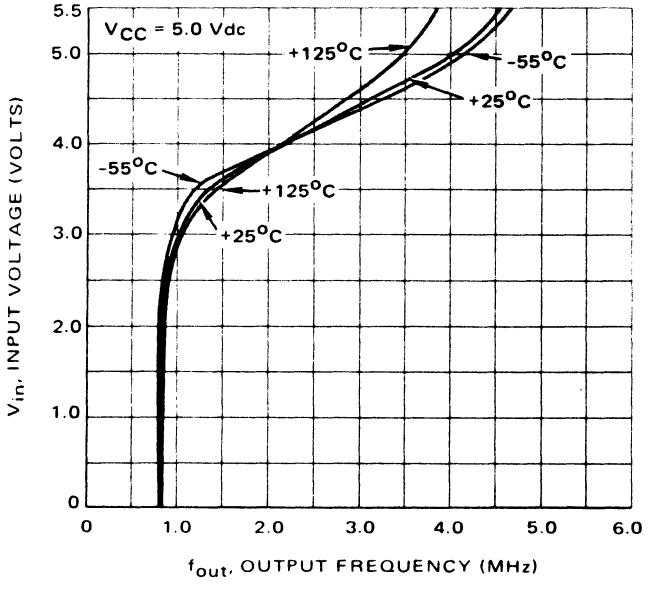

FIGURE 8 – MC4324 Input Voltage versus Output Frequency (100 pF Feedback Capacitor)

The transfer function of the VCM is given by

$$K_O = \frac{K_V}{s} \qquad (45)$$

Where K_V is the sensitivity in radians per second per volt. From the curve in Figure 8, K_V is found by taking the reciprocal of the slope.

$$K_V = \frac{4\text{ MHz} - 1.5\text{ MHz}}{5\text{ V} - 3.6\text{ V}}\ 2\pi \text{ rad/s/V}$$

$$K_V = 11.2 \text{ X } 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_O = \frac{11.2 \text{ X } 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by [5]

$$K_p = \frac{\text{DF High - UF Low}}{2(2\pi)} = \frac{2.3\text{ V} - 0.9\text{ V}}{4\pi} = 0.111\text{ V/rad} \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_O, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)\,H(s) = \frac{K_p\,K_V\,K_n\,K_f}{s} = \frac{K(s+a)}{s^2} \qquad (49)$$

Thus K_f must take the form

$$K_f = \frac{s+a}{s} \qquad (50)$$

in order to provide all the necessary poles and zeroes for

the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \quad \text{for large A} \tag{51}$$

where A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter K_f. An additional low current high β buffering device or FET can be used to boost the input impedance thus minimizing the leakage current from the capacitor C between sample updates. As a result longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs} \right) \tag{52}$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its Laplace representation in Figure 11.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \tag{53}$$

$$G(s)\,H(s) = K_p (0.5) \left(\frac{R_2Cs + 1}{R_1Cs} \right) \left(\frac{K_v}{s} \right) \left(\frac{1}{N} \right) \tag{54}$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5\,K_p K_v R_2}{R_1 N} s + \frac{0.5\,K_p K_v}{R_1 CN} \tag{55}$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5\,K_p K_v R_2}{R_1 N} s + \frac{0.5\,K_p K_v}{R_1 CN}$$

$$= s^2 + 2\zeta \omega_n s + \omega_n^2 \tag{56}$$

Equating like coefficients yields

$$\frac{0.5\,K_p K_v}{R_1 CN} = \omega_n^2 \tag{57}$$

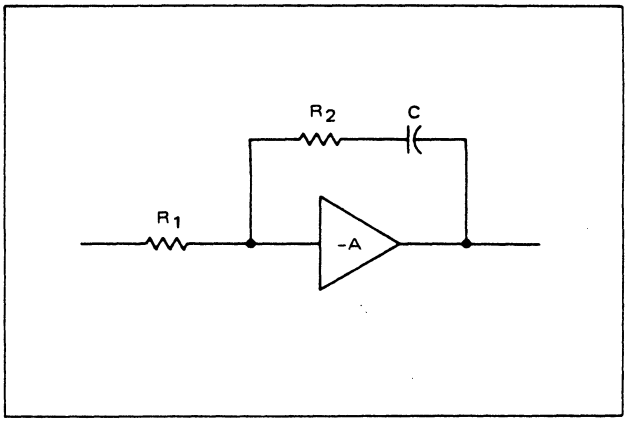

FIGURE 9 – Active Filter Design

$$\text{and} \quad \frac{0.5\,K_p K_v R_2}{R_1 N} = 2\zeta \omega_n \tag{58}$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p K_v}{R_1 CN} = \omega_n^2 \tag{59}$$

$$\frac{K_p K_v R_2}{R_1 N} = 2\zeta \omega_n \tag{60}$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6 it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle to within 5% at $\omega_n t = 4.5$. The required lock-up time is 1 ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \tag{61}$$

Rewriting Equation 57

$$R_1 C = \frac{0.5\,K_p K_v}{\omega_n^2 N} \tag{62}$$

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1 C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\ \mu F$

Then $R_1 = \dfrac{0.00102}{0.5 \times 10^{-6}} = 2.04\ k\Omega$

Use $R_1 = 2\ k\Omega$

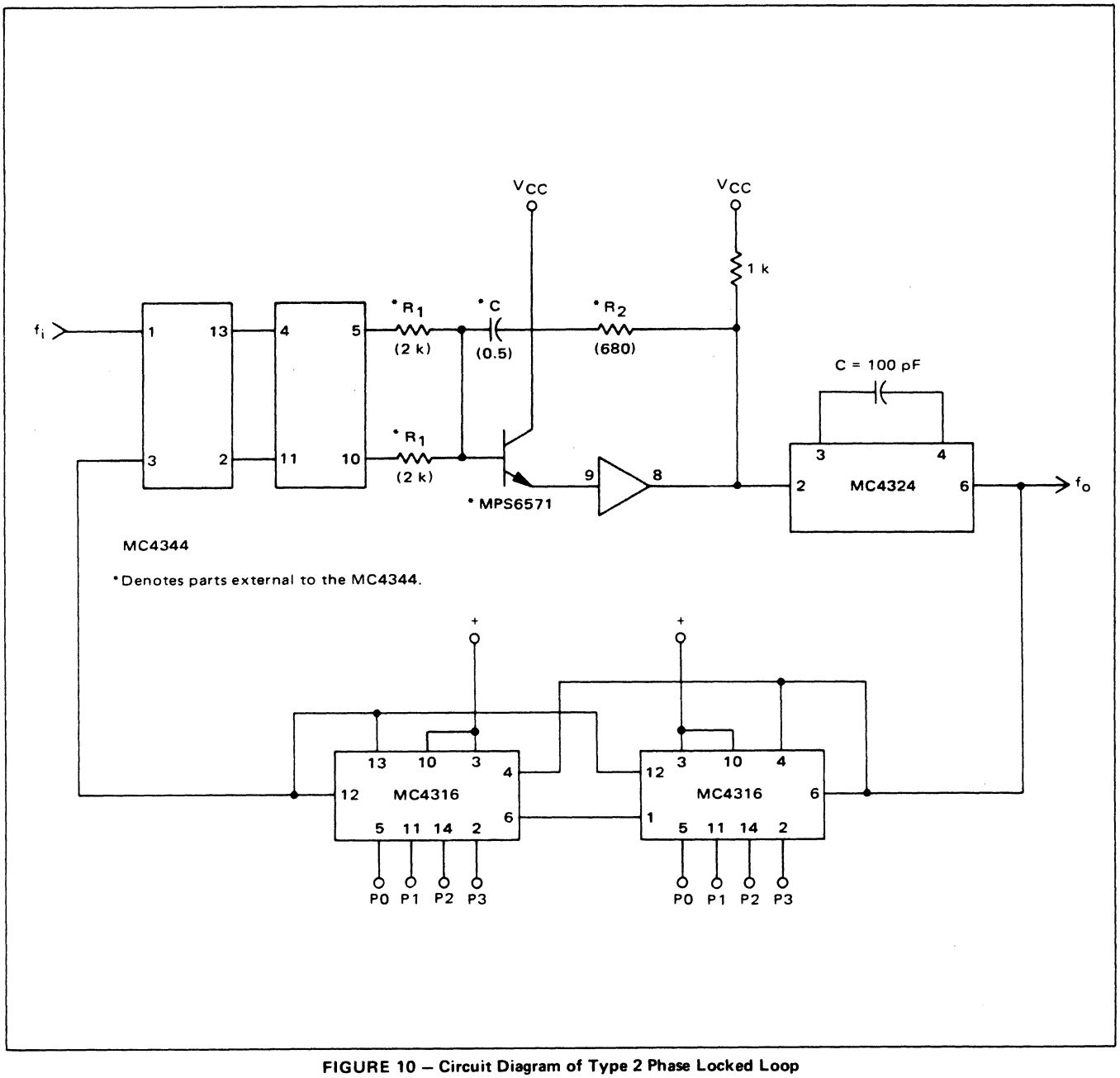

FIGURE 10 – Circuit Diagram of Type 2 Phase Locked Loop

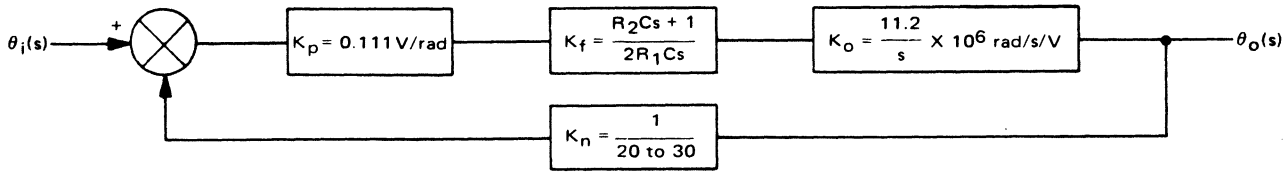

FIGURE 11 – Laplace Representation of Diagram in Figure 10

R_1 is typically selected greater than 1 kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta\,\omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\zeta}{C\,\omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5\text{ k})}$$

$$= 711\ \Omega$$

use $R_2 = 680\ \Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary is position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

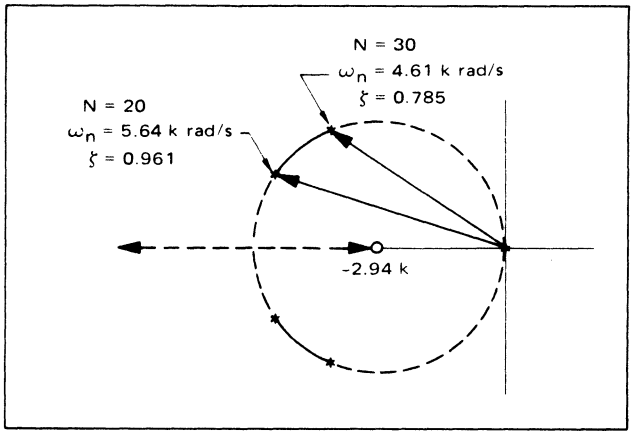

FIGURE 12 – Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design.

EXPERIMENTAL RESULTS

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

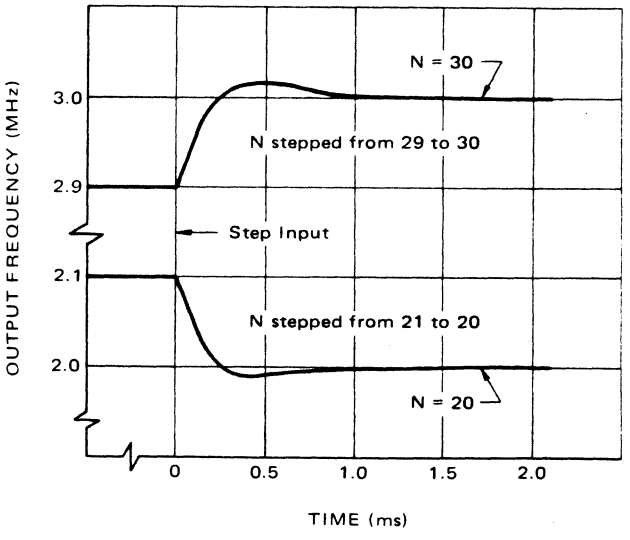

FIGURE 13 – Frequency-Time Response

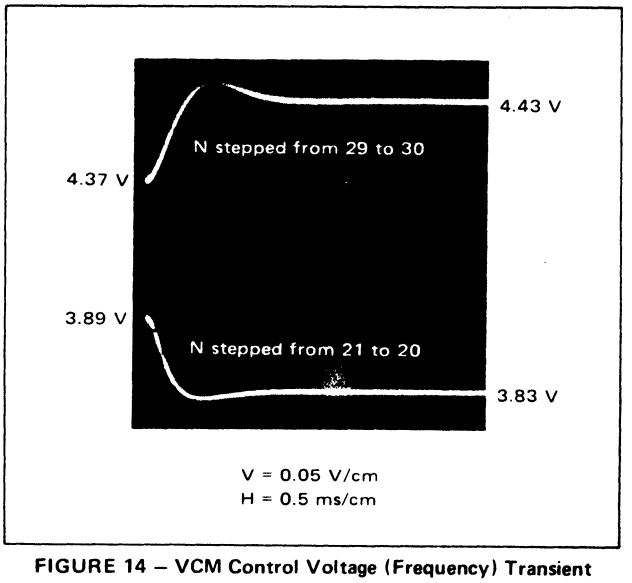

FIGURE 14 – VCM Control Voltage (Frequency) Transient

*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 =	0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 =	1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 =	3900 OHMS ($R1_c$ = 2 k)
FILTER FEEDBACK RESISTOR	R2 =	680 OHMS
FILTER CAPACITOR	C1 =	0.5 MICROFARADS
DIVIDER VALUE	N1-N2 =	29 - 30
REFERENCE FREQUENCY	F1 =	100000 CPS
OUTPUT FREQUENCY CHANGE	F5 =	100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3 - N4 = 21 - 20
R3 = 3900 ($R1_c$ = 2 k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS *

(NOTE: Y(T) IS PLOTTED '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.00005
FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

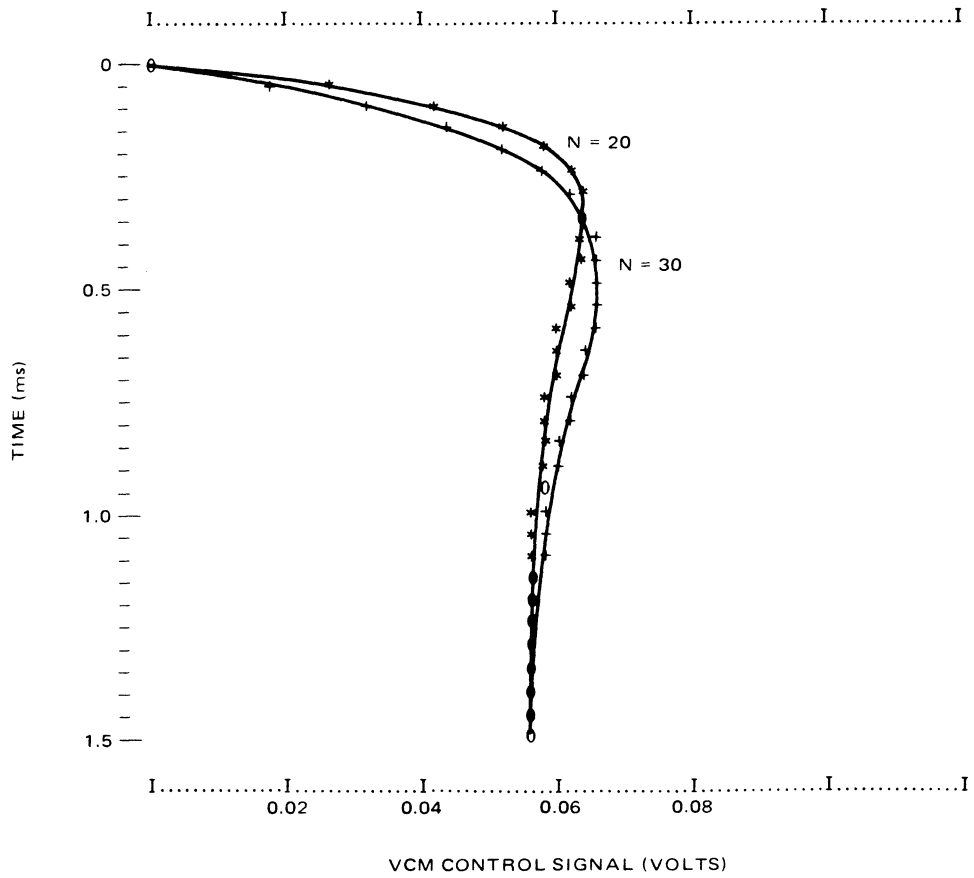

FIGURE 15 – VCM Control Signal Transient

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leqslant 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

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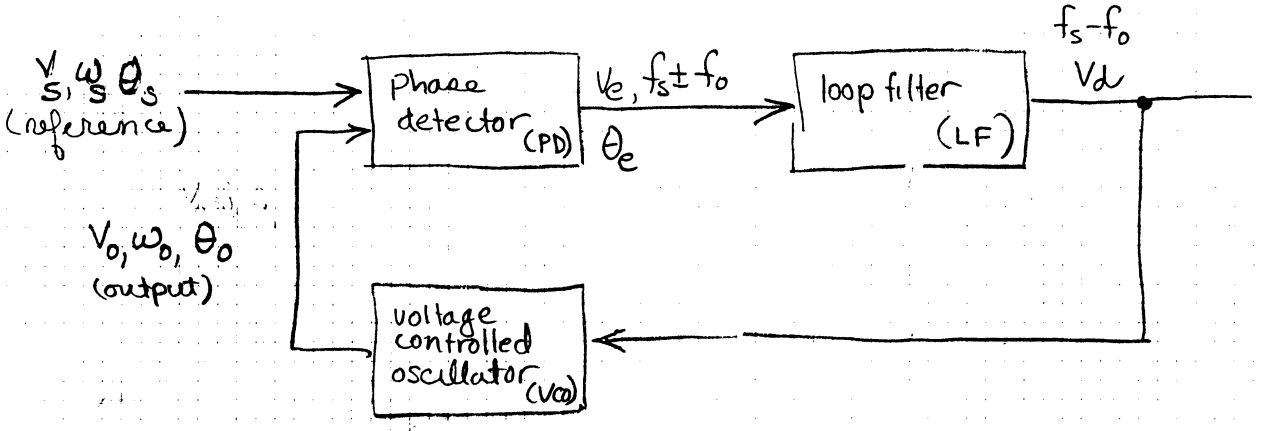
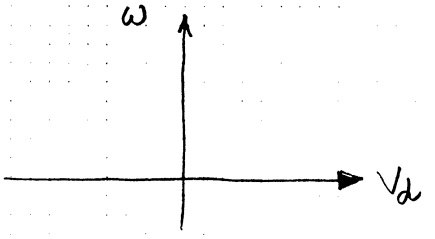
Phase-locked loops (PLL's)

A PLL is a circuit which synchronizes an output signal (generated by an oscillator) with a reference (or input) signal in frequency and in phase. In the synchronized (locked) mode the phase error between the oscillator's output and the reference signal is very small (essentially zero). If any phase difference develops the control mechanism in the PLL acts on the oscillator to reduce the phase error to a minimum.



VCO

- operates at an angular frequency ω_2 determined by V_d
- $\omega_2(t) = \omega_f + K_o V_d(t)$
- ω_o is the center frequency of the loop
- K_o is the VCO gain in $\frac{rad/sec}{volt}$ or $\frac{rad}{sec\text{-}volts}$



PD (phase detector or phase comparator)

- compares the phase of the output signal $V_o(t)$ with the phase of the reference signal $V_s(t)$ and develops an output signal $V_e(t)$ which is (usually only approximately) proportional to the phase error θ_e
- $V_e(t) = K_d \theta_e(t)$
- K_d has units $\frac{volts}{radian}$
- output signal is usually a dc component + superimposed ac component

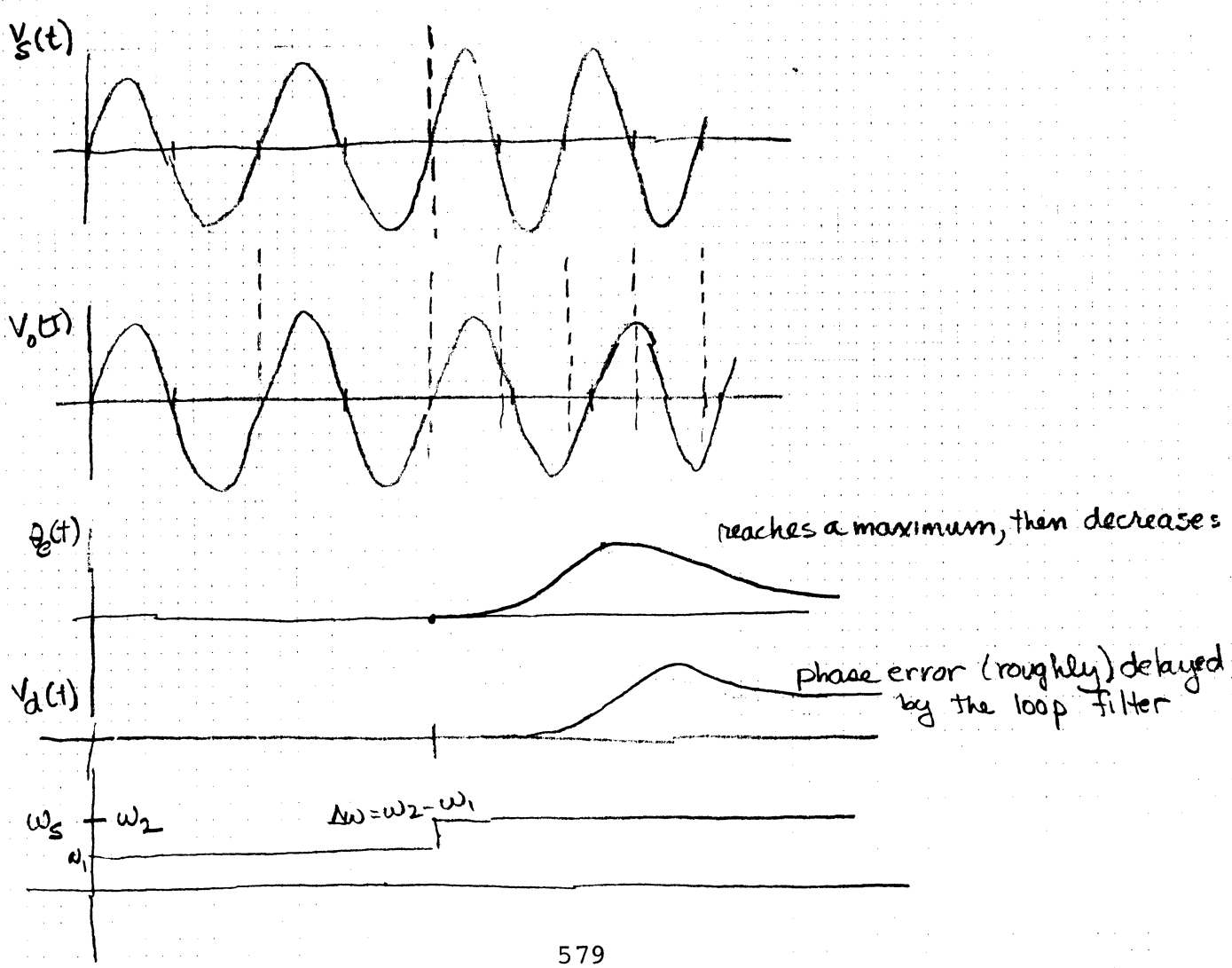
loop filter

- usually a simple low pass filter
- removes the a.c. component from the PD output

How does a PLL work?

1. If $\omega_s = \omega_o$ the VCO must be at its center frequency. This implies that θ_e (the phase error) $= 0$ and $V_d = 0$. This is a stable, locked PLL.
2. If $\theta_e \neq 0$ initially, then $V_d \neq 0$. This would cause the VCO to change its operating frequency ω_o in such a way that the phase error finally vanishes. This is the acquisition mode of a PLL.

response of a PLL to a step change in frequency



Assume ω_s suddenly jumps from ω_1 to ω_2. The phase of the input signal now leads the oscillator frequency creating a phase error which increases with time. The VCO control voltage $V_d(t)$ will also rise (with a delay given by the loop filter) with time. This causes the VCO to increase its frequency which decreases the phase error. After some time interval the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending on the type of loop filter used, the final θ_e will either be zero or a finite value.

The VCO is now locked at a frequency ω_2 which is greater than ω_1 by $\Delta\omega$. This means that $V_d(t)$ increased by a value $\frac{\Delta\omega}{K_0}$. If the center frequency of the input signal is frequency modulated by a low-frequency signal the output signal V_d is the demodulated signal. Thus, the PLL can operate as an FM detector.

Another major application of the PLL is to remove noise from signals. Suppose V_s has a lot of noise. Then the PD output will be a random signal with some average value. If the loop filter is low enough in frequency there will be almost no noise on the loop output $V_d(t)$.

If $\Delta\omega$ is too large the PLL will become "unlocked". The control mechanism will attempt to lock but may not be able to.

There are only several basic types of PD's, VCO's, and loop filters which will be discussed.

types of phase detectors

type 1 (four-quadrant multiplier)

$$v_s = V_s \sin(\omega_s t + \theta_s)$$

$$v_o = V_o \cos(\omega_o t + \theta_o)$$

the four quadrant multiplier is actually a mixer with output

$$V_d(t) = k\, v_s(t)\, v_o(t) = k\, V_s V_t \sin(\omega_s t + \theta_s)\cos(\omega_o t + \theta_o)$$

$$= \frac{k V_s V_t}{2}\left[\underbrace{\sin(\theta_s - \theta_o)}_{\text{dc term}} + \underbrace{\sin(2\omega_s t + \theta_s + \theta_o)}_{\text{ac term}}\right.$$

The loop filter removes the ac component. Note that if $\omega_s \neq \omega_o$ there is no dc component.

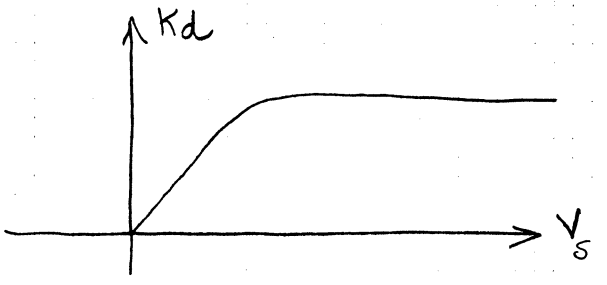
$$\therefore \quad V_d(t) = \frac{k V_s V_o}{2} \sin(\theta_s - \theta_o)$$

$\theta_e = \theta_s - \theta_o$ and if $\theta_e \ll 1$ then

$$V_d(t) \approx \frac{k V_s V_o}{2}\, \theta_e$$

$$\text{so} \quad K_d = \frac{k V_s V_o}{2}$$

This is as long as V_s and V_o are small. As V_s and/or V_o increase in amplitude the type 1 PD eventually saturates.



A type 1 PD operating in the presence of noise is an excellent filter.

Note in most PLL's the VCO is a square wave so that only odd harmonics are generated and can be easily filtered.

type 2, 3 and 4 PD's are digital circuits requiring analog signal processing to use them in non-digital circuits

type 2 - XOR circuit

if in phase output is always zero.
if exactly out of phase output is always 1
if $\pm \frac{\pi}{2}$ out of phase output is a square wave at $2\omega_s$.
if $v_s(t)$ or $v_o(t)$ are not symmetrical the PD characteristic becomes clipped

type 3 - edge triggered JK flip-flop.

average PD output is defined by a weighted output.

MC4024 usually implemented by something called a <u>charge pump</u>, i.e. an integrator with a switched sign.

not dependent on duty cycle
frequency error signal when $|\omega_s - \omega_o|$ is large

type 4 - phase / frequency detector.

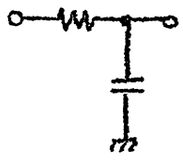
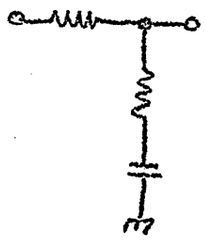
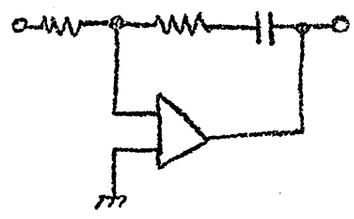
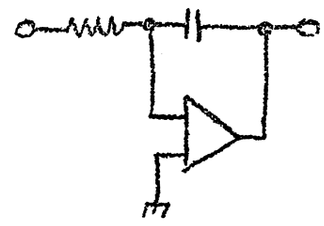
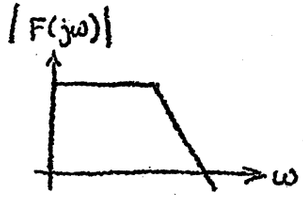
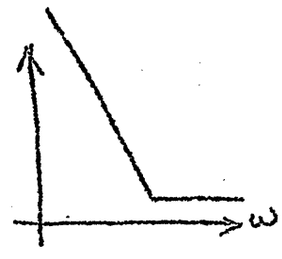
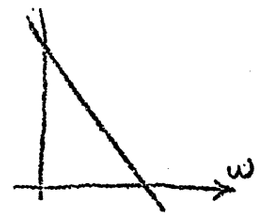
frequency sensitive for any $|\omega_s - \omega_o|$

The type of PD used is the most important criteria in determining loop performance; however, the PLL dynamic performance is also effected by the loop filter.

The general form of a first-order LPF

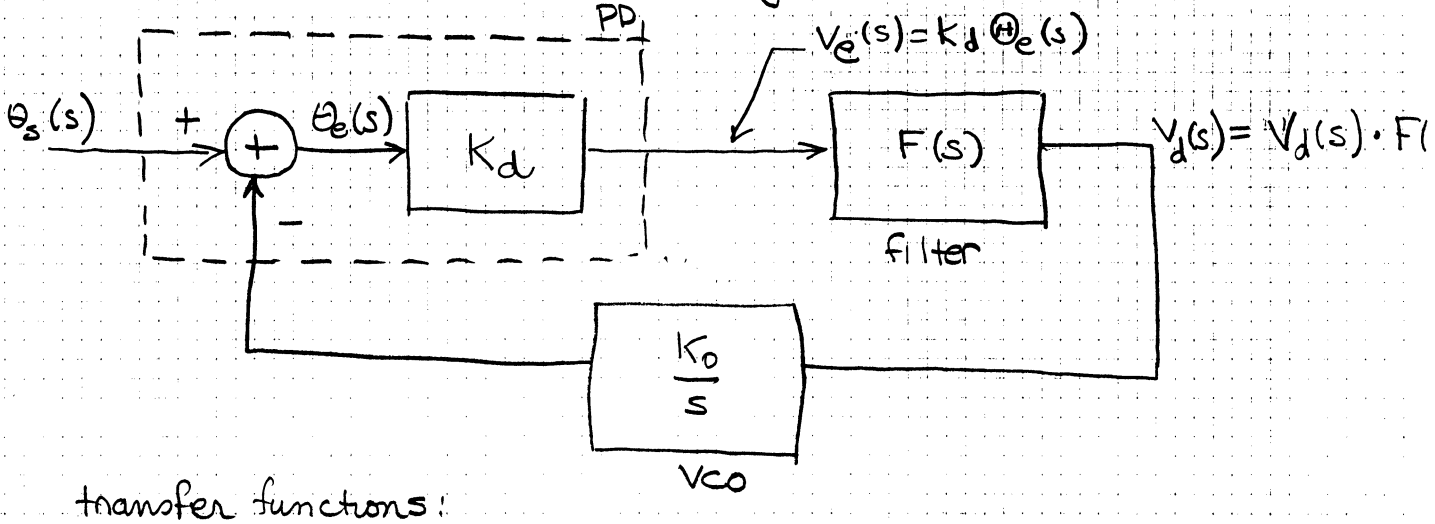
$$F(j\omega) = \frac{a + b(j\omega)}{c + d(j\omega)}$$

POSSIBLE PLL FIRST-ORDER LOW-PASS FILTERS

	PASSIVE		ACTIVE	
TYPE	1	2	3	4
CIRCUIT				
TRANSFER FUNCTION				
$F(j\omega)$	$\frac{1}{1+j\omega T_1}$	$\frac{1+j\omega T_2}{1+j\omega(T_1+T_2)}$	$\frac{1+j\omega T_2}{j\omega T_1}$	$\frac{1}{j\omega T_1}$

TYPES OF PHASE DETECTORS
1
2
3
4
4-quadrant multiplier
Exclusive or
Edge-triggered JK master-slave flip-flop
sine or square wave
V_s
V_o can also be a square wave
given by phase error only $\omega_s - \omega_o$
undefined
UP
DOWN

write the PLL in the s-domain using Laplace transforms.



transfer functions:

phase detector: $\frac{V_e(s)}{\Theta_e(s)} = K_d$ independent of frequency

loop filter $\frac{V_d(s)}{V_e(s)} = F(s)$

VCO $\frac{\Theta_0(s)}{V_d(s)} = \frac{K_0}{s}$ looks like an integrator

transfer function of the VCO

$$\omega_0(t) = \omega_f + K_0 V_d(t)$$

integrate to get phase signal

$$\omega_f t + \theta_0(t) = \omega_f t + K_0 \int_0^t V_d(\tau)\, d\tau$$

applying the Laplace transform $\downarrow$

$$\frac{K_0 V_d(s)}{s}$$

We can now write the loop transfer functions

phase transfer function $H(s) = \dfrac{\Theta_o(s)}{\Theta_s(s)}$

$$\Theta_o(s) = \frac{K_o}{s} V_d(s) = \frac{K_o}{s} F(s)\,\Theta_e(s) = \frac{K_o}{s} F(s) K_d \left[\Theta_s(s) - (\right.$$

$$\therefore \quad \Theta_o(s)\left[1 + \frac{K_o}{s} F(s) K_d\right] = \frac{K_o}{s} F(s) K_d\, \Theta_s(s)$$

$$H(s) \quad \frac{\Theta_o(s)}{\Theta_s(s)} = \frac{K_o K_d\, F(s)}{s + K_o K_d\, F(s)}$$

error transfer function $H_e(s) = \dfrac{\Theta_e(s)}{\Theta_o(s)}$

$$\Theta_e(s) = \Theta_s(s) - \Theta_o(s) = \frac{\Theta_o(s)}{H(s)} - \Theta_o(s) = \Theta_o(s)\left[\frac{1 - H(s)}{H(s)}\right]$$

$$\therefore H_e(s) = \frac{\Theta_e(s)}{\Theta_o(s)} = \frac{1 - H(s)}{H(s)} = \frac{1 - \dfrac{K_o K_d\, F(s)}{s + K_o K_d\, F(s)}}{\dfrac{K_o K_d\, F(s)}{s + K_o K_d\, F(s)}} = \frac{s}{s + K_o K_d\, F(s)}$$

We define the order of a PLL = order of loop filter + 1

because the order of the denominators of H_s and H_e are of that order. For example, if $F(s) = \frac{1}{s}$ which is first order

then both $H(s)$ and $H_e(s) \sim \dfrac{1}{s^2 + as + 1}$ i.e. second order

theory of the linear PLL:

linear means that the PD is linear, i.e. type 1

The PLL control system is <u>not</u> linear.

tracking can be simplified to a linear system

acquisition is NEVER linear.

represent input signals as phase signals

$$v_s(t) = V_s \sin\left[\omega_f t + \theta_s(t)\right]$$

phase step $\theta = \begin{cases} 0 & t \le 0 \\ \Delta\Phi & t > 0 \end{cases}$

$\therefore \theta_i(t) = \Delta\Phi\, u(t)$

} this is phase modulation

frequency step $\sin[\omega_0 t] \quad t \le 0$

$\sin[\omega_f t + \Delta\omega t] \quad t > 0$

$\therefore \theta_s(t) = \Delta\omega\, t$

} frequency step

the phase signal is a ramp

in general, $\omega_s(t) = \omega_f t + \Delta\dot{\omega} t$

where $\Delta\dot{\omega} = \frac{\partial}{\partial t}(\Delta\omega)$

or $\sin \int_0^t \left[\omega_f + \Delta\dot{\omega}\,\tau\right] d\tau$

$\therefore \theta_s(t) = \int_0^t (\Delta\dot{\omega})\,\tau\, d\tau = (\Delta\dot{\omega})\frac{t^2}{2}$

} frequency ramp

in its most general form.

we used a sine and a cosine because a type 1 PD has an intrinsic phase shift of $\frac{\pi}{2}$ (90°) between the reference and output signals. Use of a sine and cosine makes this difference zero. Otherwise, we would need to subtract or add $\pi/2$.

normalized loop variables

since we have only a few variations of loop components we can substitute the filter expressions into $H(s)$ and $H_e(s)$.

Note type 1 filter is a type 2 with $\tau_2 = 0$ } type 2 is general passive $\frac{1+j\omega\tau_1}{1+j\omega(\tau_1+\tau_2)}$

type 4 filter is a type 3 with $\tau_2 = 0$ } type 3 is general active $\frac{1+j\omega\tau_2}{j\omega\tau_1}$

passive loop filter

$$H(s) = \frac{K_0 K_d F(s)}{s + K_0 K_d F(s)} = \frac{K_0 K_d \frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}}{s + K_0 K_d \frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}}$$

$$= \frac{K_0 K_d \; 1+s\tau_2}{s + s^2(\tau_1+\tau_2) + K_0 K_d + s K_0 K_d \tau_2}$$

$$= \frac{K_0 K_d (1+s\tau_2)}{s^2(\tau_1+\tau_2) + s(1+K_0 K_d \tau_2) + K_0 K_d}$$

$$= \frac{K_0 K_d \left(\frac{1+s\tau_2}{\tau_1+\tau_2}\right)}{s^2 + s\,\frac{1+K_0 K_d \tau_2)}{\tau_1+\tau_2} + \frac{K_0 K_d}{\tau_1+\tau_2}}$$

active loop filter:

$$H(s) = \frac{K_0 K_d \frac{1+s\tau_2}{s\tau_1}}{s + K_0 K_d \frac{1+s\tau_2}{s\tau_1}} = \frac{K_0 K_d (1+s\tau_2)}{s^2\tau_1 + K_0 K_d (1+s\tau_2)}$$

$$= \frac{K_0 K_d \left(\frac{1+s\tau_2}{\tau_1}\right)}{s^2 + K_0 K_d \frac{\tau_2}{\tau_1} s + \frac{K_0 K_d}{\tau_1}}$$

note denominators of form $s^2 + 2\zeta\omega_n s + \omega_n^2$

where ω_n = natural frequency

ζ = damping factor

for the passive loop

$$\omega_n = \sqrt{\frac{K_0 K_d}{\tau_1 + \tau_2}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K_0 K_d}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_0 K_d}\right)$$

active loop

$$\omega_n = \sqrt{\frac{K_0 K_d}{\tau_1}}$$

$$\zeta = \frac{\tau_2}{2}\sqrt{\frac{K_0 K_d}{\tau_1}}$$

ω_n is <u>NOT</u> the center frequency of the VCO

this reduces the PLL transfer function to a simple form

$$H(s) = \frac{s\omega_n\left(2\zeta - \frac{\omega_n}{K_0 K_d}\right) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

if we calculate ω_n and ζ only unknown left is $K_0 K_d$ which is called to <u>loop gain</u>.

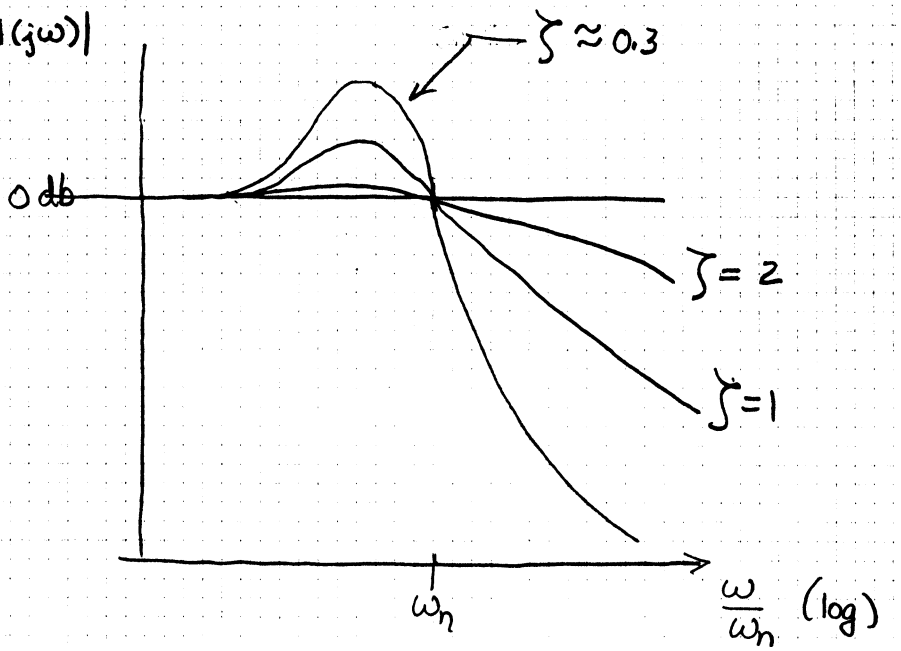
If $K_0 K_d \gg \omega_n$ high gain loop (usually true)

$K_0 K_d \ll \omega_n$ low gain loop

for a high-gain passive loop $H(s) \approx \dfrac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$

(the same as an active loop)

transient response.



this graph is valid for every second order PLL

a PLL is a low pass filter for <u>phase</u> signals $\Theta_s(t)$ whose frequency spectrum is less than ω_n

i.e. the loop will track as long as the modulation frequency of $\Theta_s(t)$ lies in $[0, \omega_n)$

ζ determines the system overshoot

$\zeta < 1$ oscillatory

$\zeta = 1$ critically damped

$\zeta > 1$ dynamic response becomes sluggish

$\zeta = 0.707$ is an optimally flat transfer function

the description of the lock-in process must be done in the time domain. The linear model is invalid so the Laplace transform cannot be used.

use $v_e(t) = K_d \sin\theta_e$

$$F(j\omega) = \frac{1+j\omega\tau_2}{1+j\omega(\tau_1+\tau_2)} = \frac{V_d(j\omega)}{V_e(j\omega)}$$

transform back to time domain

$$v_d(t) + \frac{dv_d}{dt}(\tau_1+\tau_2) = v_e(t) + \frac{dv_e}{dt}\tau_2$$

The transfer function of the VCO is

$$\frac{\Theta_0(s)}{V_d(s)} = \frac{K_0}{s}$$

which after being inverse transformed is $\theta_0(t) = K_0 \int_0^t v_d(t)\,dt$.

If we combine all these equations we get the non-linear differential equation for the phase error θ_e

$$\frac{d^2\theta_e}{dt^2} + \frac{d\theta_e}{dt}\,\frac{1+K_0K_d\tau_2\cos\theta_e}{\tau_1+\tau_2} + \frac{K_0K_d}{\tau_1+\tau_2}\sin\theta_e$$

$$= \frac{d^2\theta_s}{dt^2} + \frac{d\theta_s}{dt}\,\frac{1}{\tau_1+\tau_2}$$

which is a very hairy non-linear differential equation

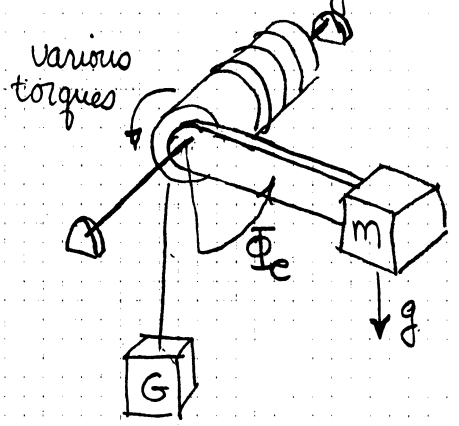
usually $K_0K_d \gg \frac{1}{\tau_2}$ so that

$$\frac{d^2\theta_e}{dt^2} + 2\zeta\omega_n\frac{d\theta_e}{dt}\cos\theta_e + \omega_n^2\sin\theta_e = \frac{d^2\theta_s}{dt^2} + \frac{d\theta_s}{dt}\,\frac{\omega_n^2}{K_0K_d}$$

nonlinearities

we can computer solve this equator or

we can solve analogous mechanical systems



J_E – due to gravitation of mass m

J_R – friction of cylinder rotating on bearings

J_A – torque generated by weight on arm.

PLL

phase error θ_e $\longleftrightarrow$ angle of deflection Φ_e

ω_n $\longleftrightarrow$ ω_n'

ζ $\longleftrightarrow$ ζ' due to viscous friction

reference phase disturbance

$$\ddot{\theta}_s + \dot{\theta}_s \frac{\omega_n^2}{K_o K_d} \longleftrightarrow \text{weight } G$$

↑ rate of change of frequency offset. $\ddot{\theta}_s(t) = \Delta\dot{\omega}$

↑ frequency offset $\dot{\theta}_s(t) = \Delta\omega(t)$

So, by analogy, putting different weights at different rates on G

case I – $G=0$, $\Phi_e=0$ pendulum is vertically resting

corresponds to PLL operating at center frequency ω_c with zero offset $\Delta\omega=0$

Zero phase error $\theta_e=0$

case II — reference signal θ_s is changed slowly

then $\ddot{\theta}_s(t)$ can be neglected

mechanically G slowly increases causing increased deflection of pendulum, if G causes Φ_e to increase beyond 90° the system will tip over i.e. this is is static limit of stability

the critical value of Δw is called to hold range

case III step change of $\theta_s(t)$

$\therefore \quad \ddot{\theta}_2 = \Delta w\, \delta(t)$

we have a step $\Delta w\, u(t)$

plus an impulse $\Delta w\, \delta(t)$

corresponds to dropping a weight ΔG onto G

if the ΔG is small, we will simply have a smooth move (oscillatory)

If the ΔG is moderate the swing can momentarily go beyond 90° but less than 180° and will oscillate back to a final $\Phi_e < 90°$

$\Rightarrow$ there is a frequency step which causes the PLL to unlock. This frequency step is called the pull-out range. Pull-out range is markedly smaller smaller than hold range.

Pull-out range is dynamic range of stability

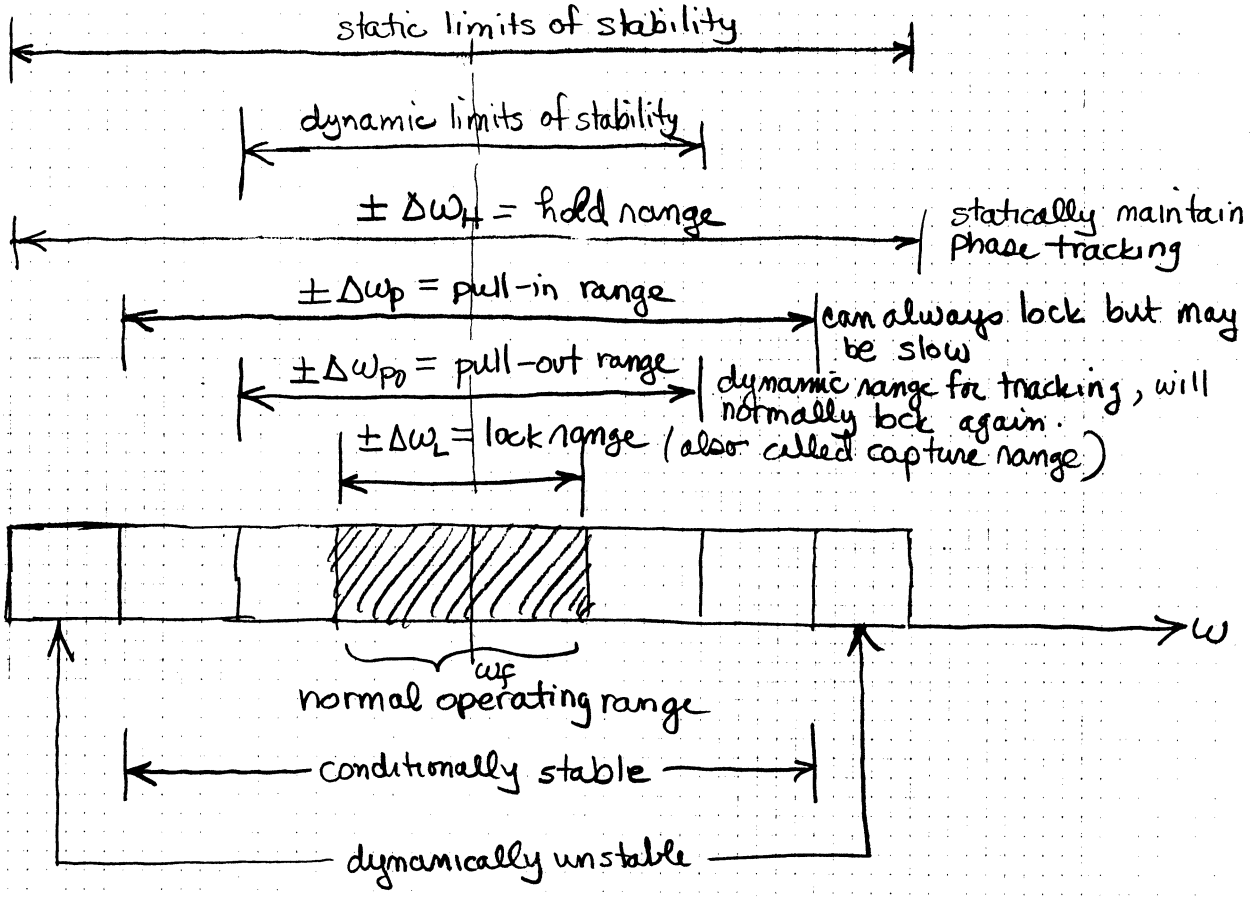
Case IV – $\Delta\omega$ increases linearly

too rapid an increase $\Delta\omega$ will cause system to become unstable.

always need $\Delta\dot{\omega} < \omega_n^2$

conditions for stability in phase tracking

1. angular frequency of $\theta_s(t)$ must be in the hold range
2. maximum frequency step $\Delta\omega$ must be smaller than pull-out range
3. rate of change of $\theta_s(t)$ $\Delta\dot{\omega}$ must be less than ω_n^2



linear second-order PLL

The hold range

$$\omega_s = \omega_f + \Delta\omega_H$$

want to calculate the $\Delta\omega_H$ which will cause a phase error of $\frac{\pi}{2}$.

$$\theta_s(t) = \Delta\omega_H t$$

$$\Theta_s(s) = \frac{\Delta\omega}{s^2}$$

$$\Theta_e(s) = \Theta_s(s) H_e(s) = \left[\frac{\Delta\omega}{s^2}\right] \frac{K_o K_d F(s)}{s + K_o K_d F(s)}$$

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\Theta_e(s) = \lim_{s\to 0} \left[\frac{\Delta\omega}{s^2}\right] \frac{s K_o K_d F(s)}{(s + K_o K_d F(s))}$$??

$$\lim_{t\to\infty} \sin\theta_e(t) = \frac{\Delta\omega}{K_o K_d F(\phi)}$$

at limit of stability $\theta_e = \frac{\pi}{2}$ and $\sin\frac{\pi}{2} = 1$

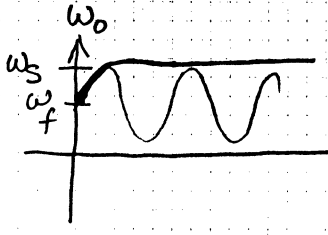
$$\therefore \quad \Delta\omega_H = K_o K_d F(\phi) = \begin{cases} \infty & \text{active loop} \\ K_o K_d F(\phi) & \text{passive loop} \end{cases}$$

limits of loop filter

$K_o K_d F(\phi)$ limited to $\pi/2$ for type 1 & 2, π for type 4.

the lock range

phase detector output for non-locked PLL, $\omega_o = \omega_f + \Delta\omega$



$$\therefore \quad v_e(t) = K_d \left[\sin(\Delta\omega)t + \underbrace{\sin\{(2\omega_f + \Delta\omega)t + \phi\}}_{\text{filtered out}} \right]$$

$$v_d(t) \approx K_d \left| F(j\Delta\omega) \right| \sin(\Delta\omega t + \phi)$$

ϕ due to filter, not same ϕ

For locking want $|K_o v_d(t)| \geq \Delta\omega$, i.e. the loop will quickly go thru the desired frequency.

$$\Delta\omega_L = K_o K_d \left| F(j\Delta\omega) \right|$$

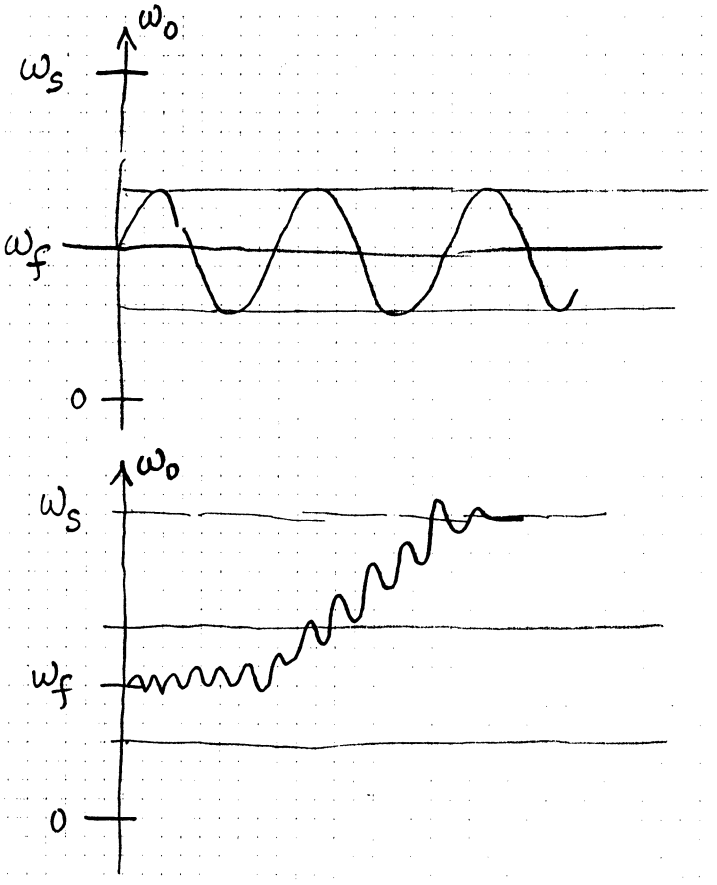
approximate $|F(j\Delta\omega)| = \begin{cases} \frac{1}{\omega\tau_1} & \text{for type 1 \& 4 filters} \\ \frac{\tau_2}{\tau_1 + \tau_2} & \text{for type 2} \\ \tau_2/\tau_1 & \text{for type 3} \end{cases}$

we can apply some approximations to get

$$\Delta\omega_L \approx \omega_n \quad \text{for} \quad \text{Type 1 and 4 filters}$$

$$\approx 2\zeta\omega_n \quad \text{for} \quad \text{type 2 and 3 filters}$$

The pull-in range



$$\Delta\omega_p \approx \frac{8}{\pi}\sqrt{\zeta\omega_n K_0 K_d - \omega_n^2}$$

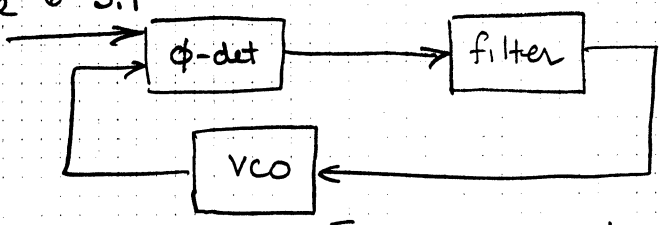
for high gain loops this reduces t

$$\Delta\omega_p \approx \frac{8}{\pi}\sqrt{\zeta\omega_n K_0 K_d}$$

The pull out range

from analog computer simulation $\Delta\omega_{po} = 1.8\,\omega_n\,(\zeta+1)$

Example 6-3.1



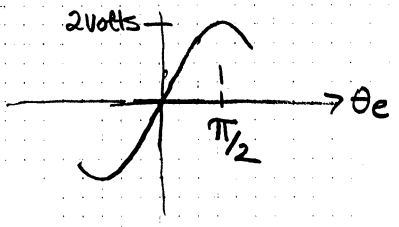
$f_f = 10^5$ Hz $= 100$ kHz

$K_o = 2\pi \times 100 \frac{\text{rad}}{\text{s}} = 100 \text{ Hz/V}$.

filter has $K_a = 10$.

use a type 1 sinusoidal phase detector with

$V_{e,max} = 2$ Volts @ $\theta_e = \frac{\pi}{2}$.



for a sinusoidal detector

$V_e = K_d \sin\theta_e$ (evaluated at $\theta_e = \pi/2$, $V_e = 2$)

$\therefore K_d = \frac{2}{1} = 2$

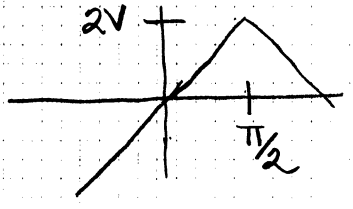
the open loop gain $K_v = K_o K_d \underbrace{F(\phi)}_{\text{don't neglect this}} = 200\pi \frac{\text{rad/sec}}{\text{V}} \cdot \frac{2\text{V}}{\text{rad}}$

$= 4000\pi$

hold-in range $\Delta\omega_H \approx \pm K_v = \pm 4000\pi$ rad/sec.

or $\Delta f_H \approx \pm 2000$ Hz

Example 6-3.2 use a triangular PD (type 2) with



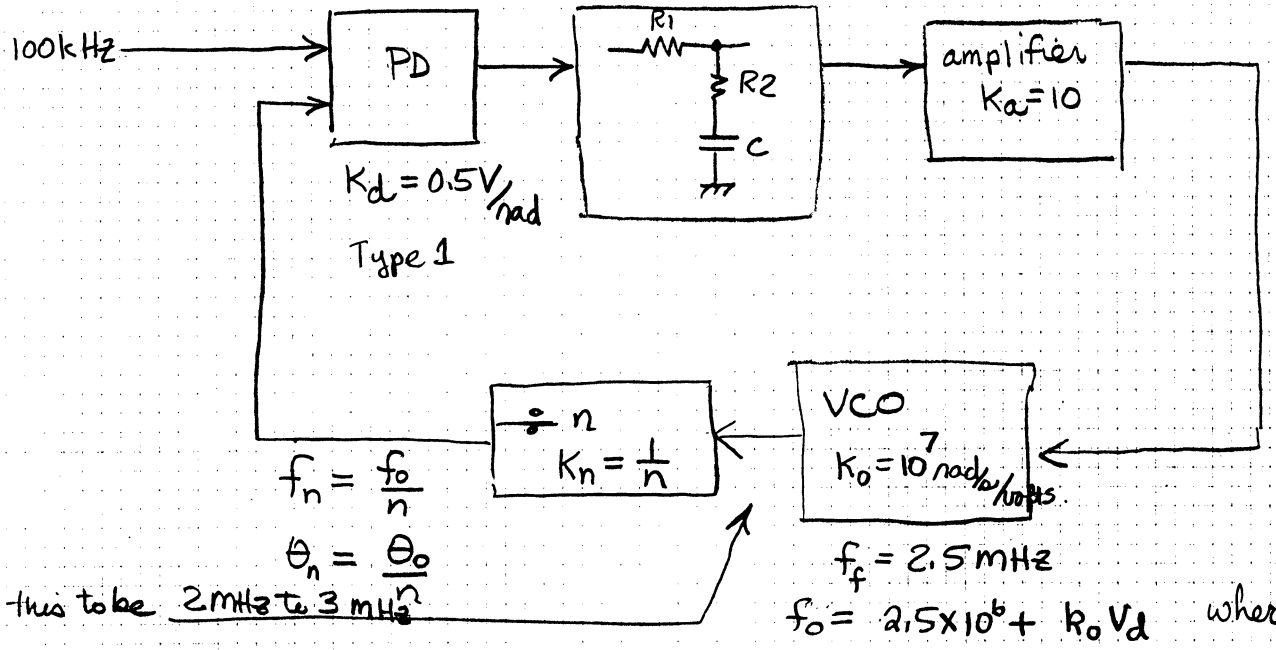
for a triangular PD $K_d = \frac{2\text{V}}{\pi/2} = \frac{4}{\pi}$

open loop gain $K_v = K_o K_d F(\phi) = \frac{4}{\pi} \cdot 200\pi \cdot 10$

$= 8000$

$\Delta\omega_H \approx \pm K_v \theta_{e,max} = \pm 8000 \cdot \frac{\pi}{2} = \pm 4000\pi$

Overall, PLL design



what must the dc input to the VCO be?

@ $n = 20$ $\quad V_d = \dfrac{f_o - f_f}{K_o} = \dfrac{2.0 - 2.5}{1.6} = -0.3125$ volt

$$\therefore V_e = \frac{V_d}{K_a} = \frac{-.3125}{10} = -.03125 \text{ volts.}$$

$$\theta_e = \frac{V_e}{K_d} = \frac{-.03125}{.5} = -.0625 \text{ radians}$$

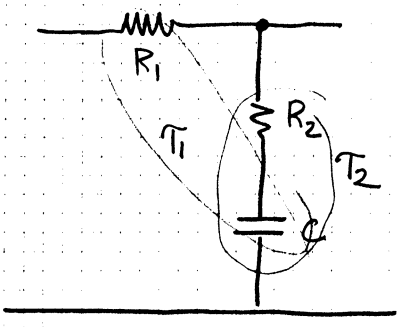
this is the phase shift needed to shift from the value at f_f, i.e: $V_e = 0$

$$\Delta\theta_o = n\Delta\theta_n = 20(-.0625) = -1.25 \text{ radians}$$

we now need to design only the filter

$$K_\gamma = (0.5)(1)(10)(10^7)\left(\frac{1}{20}\right) = 2.5 \times 10^6$$

It remains to pick ω_n and ζ. ζ is picked simply to be reasonably smooth → pick $\zeta = 0.8$. ω_n determines the modulation (max) for the loop. In this case it determines the frequency of the transient. Pick $\omega_n = 10^4$ rad/sec. (Determines lock-up time $\approx \frac{1}{\omega_n} = 0.1$ msec)



$$\omega_n = \frac{K_v}{\tau_1 + \tau_2}$$

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_v}\right)$$

$$\tau_1 + \tau_2 = \frac{K_v}{\omega_n} = \frac{2.5 \times 10^6}{10^4} = .025 \text{ sec.}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_v} = \frac{2(0.8)}{10^4} - \frac{1}{2.5 \times 10^6} = 1.596 \times 10^{-4} \text{ sec.}$$

$$\tau_1 = 250 \times 10^{-4} - 1.596 \times 10^{-4} \approx .025 \text{ sec.}$$

If we arbitrarily pick $C = 0.5\,\mu f$

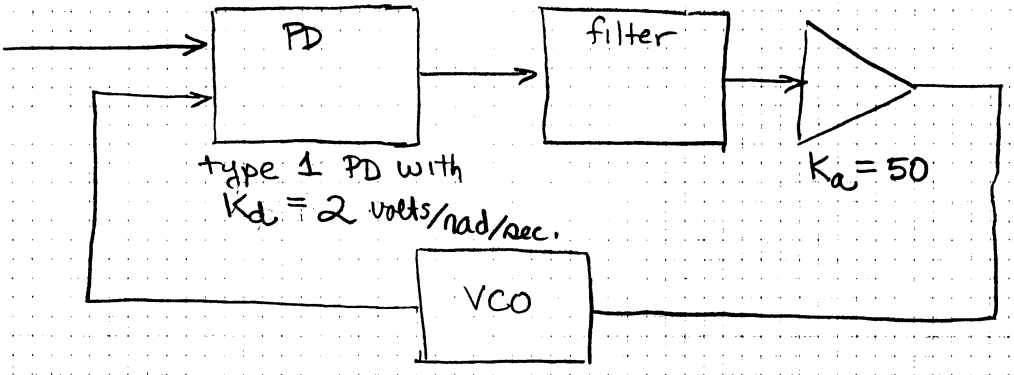
$$R_2 = \frac{\tau_2}{C} = \frac{1.596 \times 10^{-4}}{.5 \times 10^{-6}} = 319\,\Omega$$

$$R_1 = \frac{\tau_1}{C} = \frac{.025}{.5 \times 10^{-6}} \approx 50\,k\Omega.$$

6-3.1 Use the data of example 6-3.1

(a) Find the hold-in range if the amplifier gain is increased to $K_a = 50$.

(b) Find the values of θ_e, V_e and V_d if the input-signal frequency is $f_s = 100.5$ kHz.



$f_f = 10^5$

$K_o = 100\,\text{Hz/volt} = 200\pi\ \text{rad/sec/volt}$.

(a) $K_v = K_o K_d F(\phi) = 200\pi \frac{\text{rad/sec}}{\text{volt}} \cdot 2\frac{\text{rad}}{\text{V}}\, 50 = 20{,}000\pi$

$\Delta\omega_H = \pm K_v = \pm 20{,}000\pi$ ⋯ $\Delta f_H = \pm \frac{20{,}000\pi}{2\pi} = \pm 10$ kHz

(b) $f_s = 100.5$ kHz

$$V_d = \frac{f_o - f_f}{k_o} = \frac{100{,}500 - 100{,}000}{100} = \frac{500}{100} = 5 \text{ volts.}$$

$$V_e = \frac{V_d}{K_a F(\phi)} = \frac{5}{50} = 0.1$$

$$\theta_e = \frac{V_e}{K_d} = \frac{0.1}{2} = 0.05 \text{ volts.}$$

Note: usually linearize here because V_e is small

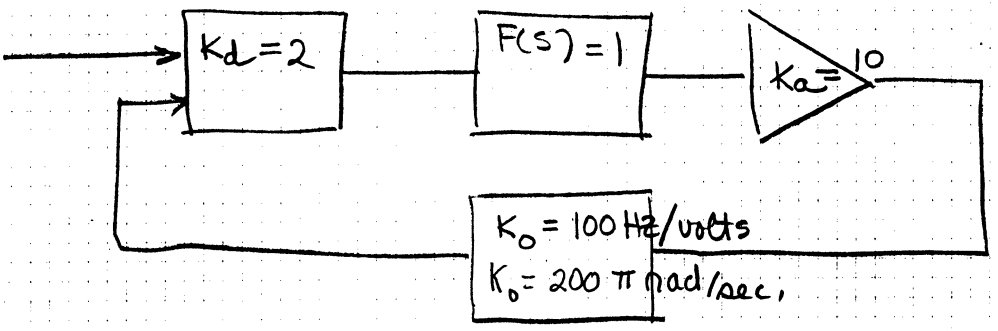
i.e. instead of $V_e = K_d \sin\theta_e$

use the approximation

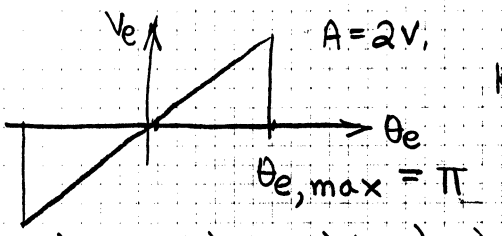
$$V_e \approx K_d \theta_e$$

as long as θ_e is in radians

6-3.2 Use the PLL components of example 6-3.1, but use a saw-tooth phase detector with A = 2V. Show that the hold in range is the same as those found in examples 6-3.1 and 6-3.2.



saw-tooth phase detector



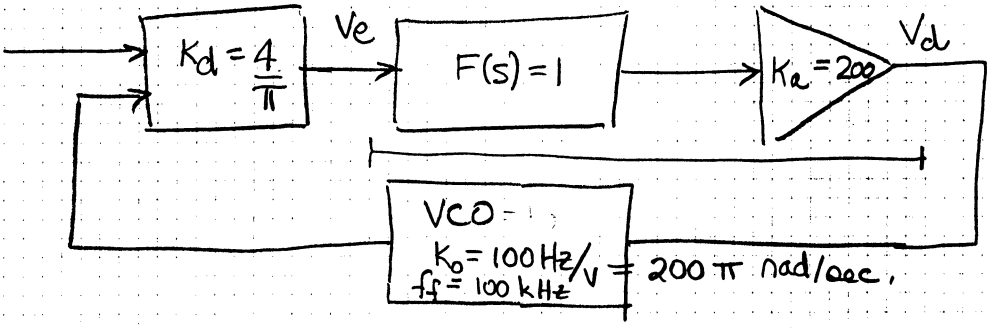
$$K_d = \frac{2}{\pi} = \frac{2}{\pi}$$

$$K_v = K_d K_o K_a F(\phi) = \left(\frac{2}{\pi}\right)(200\pi)(10)(1) = 4000$$

$$\left[\frac{\text{volt}}{\text{rad}}\right]\left[\frac{\text{rad}}{\text{sec}}\right]\left[\frac{\text{sec}}{\text{volt}}\right]$$

$$\Delta\omega_H = \pm K_v \theta_{e,max} = \pm 4000 \cdot \pi = \pm 4000\pi$$

6-3.3 Use the data of Example 6-3.2, except that the amplifier has $K_a = 200$ and it will saturate if its output exceeds 15 volts. What is the maximum phase error θ_e and steady state frequency deviation Δf that the loop can tolerate if the amplifier voltage is the limiting factor?



$V_d = \pm 15$ volts max

$$f = f_f \pm V_d K_o = 100\ kHz \pm \left(15V\right)\left(100\ \frac{Hz}{V}\right)$$

$$\therefore \quad \Delta f = 1500\ Hz.$$

maximum phase error: $\quad V_{e,max} = \frac{V_d}{K_a F(s)} = \frac{15\ volts}{200} = \boxed{.0750}$

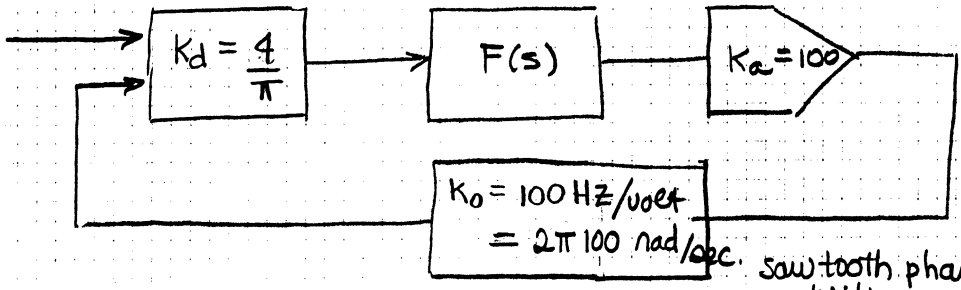
$$K_d = \frac{V_e}{\theta_e}$$

$$\theta_e = \frac{V_e}{K_d} = \frac{.0750}{4/\pi} = \boxed{.0589\ radians}$$

6-3.4 The PLL of example 6-3.2 is modified to use an amplifier with gain $K_a = 100$. The loop filter parameters are chosen to give $\omega_n = 5000$ rad/sec. and $\zeta = 0.7$

(a) Find the hold-in range.

(b) Find the approximate pull-in range.



$\omega = 2\pi f$

$f = \frac{\omega}{2\pi}$

$\omega_n = 5000$ rad/sec, $\zeta = 0.7$

(a) $K_v = K_d F(\phi) K_a K_o = \frac{4}{\pi} \cdot 1 \cdot 100 \cdot 200\pi = 80{,}000$

$\Delta\omega_H = \pm K_v \theta_{e,max} = \pm 80{,}000 \left(\frac{\pi}{2}\right) = \pm 40{,}000\pi$

$\Delta f_H = \frac{\Delta\omega_H}{2\pi} = \pm 20$ kHz

(b) $\Delta\omega_p \approx \pm \sqrt{2}\sqrt{2\zeta\omega_n K_v - \omega_n^2}$

$2(0.7)(5000)(80{,}000) = 560 \times 10^6$

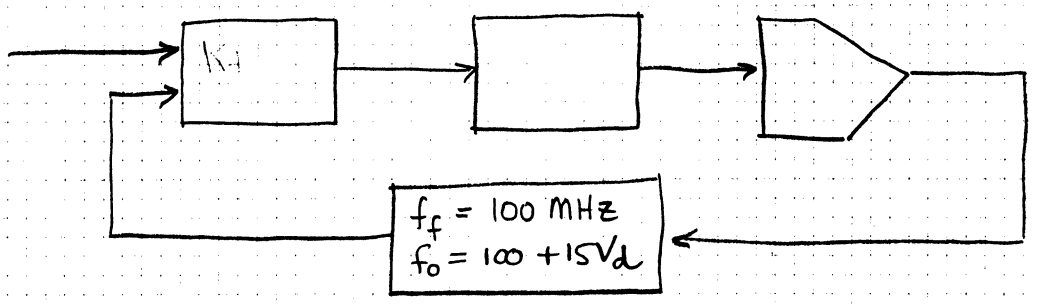
$\omega_n^2 = 25 \times 10^6$

$\Delta\omega_p \approx \pm \sqrt{4(560 - 25) \times 10^6} = \pm 46.26 \times 10^3$

$\Delta f_p = \frac{\Delta\omega_p}{2\pi} = \pm \frac{46.26}{2\pi} \times 10^3 = \pm 7.4$ kHz.

6-3.5 A phase-locked loop as shown in Fig. 6-2 is to be designed around the following elements: (1) a phase detector of the "triangular" type, Fig. 6-3b, with maximum output voltage of 300 mV, and (2) a VCO with the characteristic of Fig. 6-5 with $f_f = 100$ MHz, and $f_o = (100 + 15 V_d)$ MHz.

(a) The loop is to be designed to have a hold-in range $\pm \Delta f_H = \pm 5$ MHz. Determine the values of K_v, K_d, K_o and K_a



$$K_d = \frac{0.300 \text{ volts}}{\pi \text{ rad/sec}} = \frac{0.3}{\pi} \text{ volts/rad/sec} = .095 \text{ volts/rad/sec}$$

$$f_o = f_f + k_o V_d$$

$$2\pi f_o = 2\pi f_f + \underline{2\pi k_o} V_d$$

$$\therefore K_o = 2\pi k_o = 2\pi (15 \times 10^6) = 30\pi \times 10^6 = 94.25 \times 10^6$$

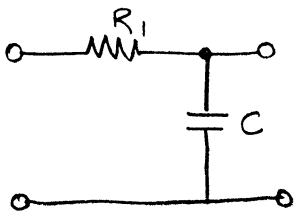
$$K_v = K_o K_d K_a F(\phi)$$

sawtooth $$K_v = \pm \frac{\Delta \omega_H}{\theta_{e,max}} = \pm \frac{2\pi \ 5 \times 10^6}{\pi} = 10 \times 10^6$$

$$\therefore \quad K_a = \frac{K_v}{K_o K_d \cdot F(\phi)} = \frac{10 \times 10^6}{(30\pi \times 10^6)\left(\frac{0.3}{\pi}\right)(1)} = \frac{10}{30(.3)}$$

$$= 1.11$$

(b) If the loop contains a low-pass filter like that of Fig 6-4a with $R_1 = 1000\ \Omega$, what is the value of C necessary to yield a 3-db bandwidth of 0.1 MHz for the filter?



$$\tau_1 = R_1 C$$

$$\frac{1}{2\pi\,(0.1\times10^{6})} = (1000)\,C$$

$$C = \frac{1}{2\pi\,(0.1)\,10^{9}} = \frac{1}{628\times10^{6}} = 1.59\ nF = .0015\ \mu f$$

(c) If $f_s = 99$ mHz, find the values of V_d, V_e and θ_e?

$$99 = f_o = 100 + 15V_d$$

$$-1 = 15V_d \qquad \therefore\ V_d = -\tfrac{1}{15} = -0.067 \text{ Volts.}$$

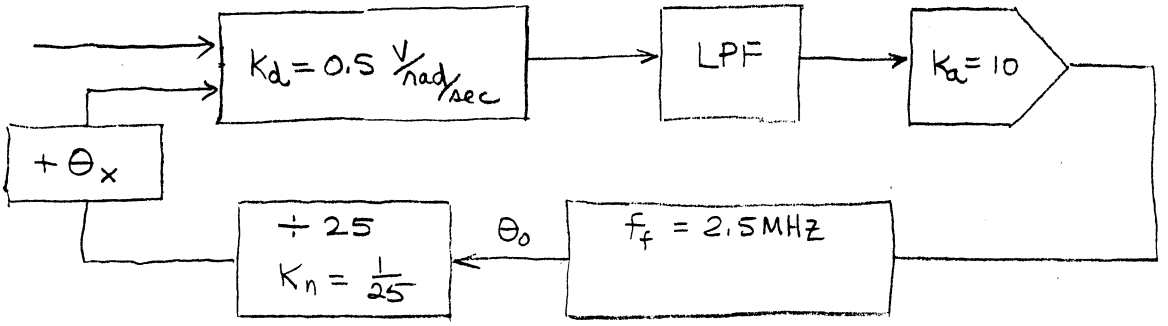
$$V_e = \frac{-.067 \text{ volts}}{1.11} = .060 \text{ volts.}$$

$$V_e = K_d\,\theta_e$$

$$.060 = \frac{0.3}{\pi}\,\theta_e$$

$$\theta_e = \frac{.060\,\pi}{.3} = 0.2\pi = 0.628 \text{ radians}$$

6-7.1 The PLL of Fig 6-16 is set up with $n = 25$ so that $f_o = f_f = 2.5$ MHz, $V_e = 0$, $\Delta\theta_o$ and $\Delta\theta_n = 0$. Then a linear, voltage-controlled phase shifter is inserted between the frequency divider and the phase detector. If the phase shifter introduces a steady state phase shift $+\theta_x$, explain in detail what effect this will have on the phase angles θ_e, θ_n (at the divider) output, and θ_o. How will this affect the VCO frequency f_o?



This corresponds to a phase step $\theta_x\, u(t)$. It is immaterial whether the shift occurs in the signal or reference port of the phase detector. A second order PLL will always return θ_e to zero (or its previous value) in response to a phase step. To prove this consider the laplace transform of the phase error transfer funct

$$H_e(s) = \frac{\Theta_e(s)}{\Theta_o(s)} = \frac{s}{s + K_o K_d F(s)}$$

originally, we wrote $\Theta_o(s)$ as the output from the oscillator. We can include the divider in the expression for K_o, i.e. $K_o' = K_o K_n = K_o/25$

Then, $$\theta_e(s) = \frac{s}{s + K_o K_n K_d F(s)} \cdot \underbrace{\frac{\theta_x}{s}}_{\text{Laplace transform of } \theta_x u(t)} = \frac{\theta_x}{s + K_o K_n K_d F(s)}$$

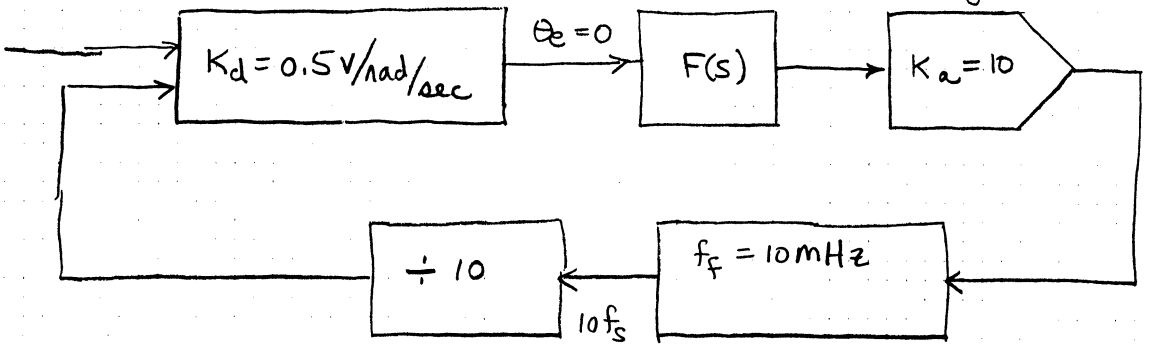
Using the final value theorem

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\,\Theta_e(s) = \lim_{s\to 0} s\,\frac{\theta_x}{s + K_o K_n K_d F(s)} = 0.$$

This could also be seen from the mechanical model $\ddot{\theta}_s + \dot{\theta}_s$

$\frac{d\theta_s}{dt} = \theta_x\,\delta(t)$, $\frac{d^2\theta_s}{dt^2} = \theta_x\,\delta'(t)$. The driving function is an impulse in response to which the phase error goes thru several oscillations and will return to zero if the loop did not unlock.

6-7.2 A PLL uses a frequency divider circuit (see Fig. 6-16) between the VCO and the phase detector so that the VCO operates at $f_o = 10 f_s$. The free-running frequency of the VCO is $f_f = 10\,MHz$. If $f_s = 1\,MHz$ θ_e at the phase detector is zero. Now suppose that f_s is changed by an amount Δf which results in $\theta_e = 0.1$ radian. What is the change in the phase angle θ_o at the output of the VCO?



This problem is unlike 6-7.1 which applied a phase step. The input is now a frequency step $\Delta f\, u(t)$. In terms of the mechanical model: recall that $\theta_s(t)$ is the integral of $\omega_s(t)$, i.e. $\omega_s(t) = \omega_o + \Delta\omega\, u(t)$. Since $\theta_s(t) = \int_0^t \Delta\omega(\tau)\, d\tau$ we have $\frac{d\theta_s(t)}{dt} = \Delta\omega\, u(t)$, $\frac{d^2\theta_s(t)}{dt^2} = \Delta\omega\, \delta(t)$. This means that the frequency step will generate a permanent non-zero θ_e, with some oscillatory behavior as the loop error settles to a final value.

$\theta_e = 0.1$ radian.

The constant θ_e is necessary to put the loop at its offset frequency. Because of the divider this corresponds to a phase shift of 1 radian at the oscillator. Hence, the VCO has changed its phase angle by 57.3° (1 radian)