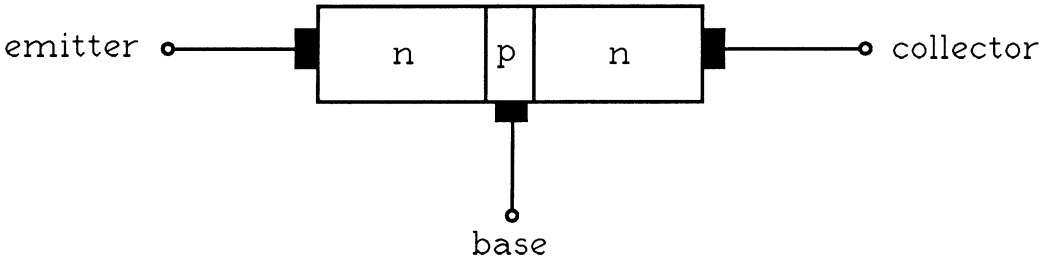
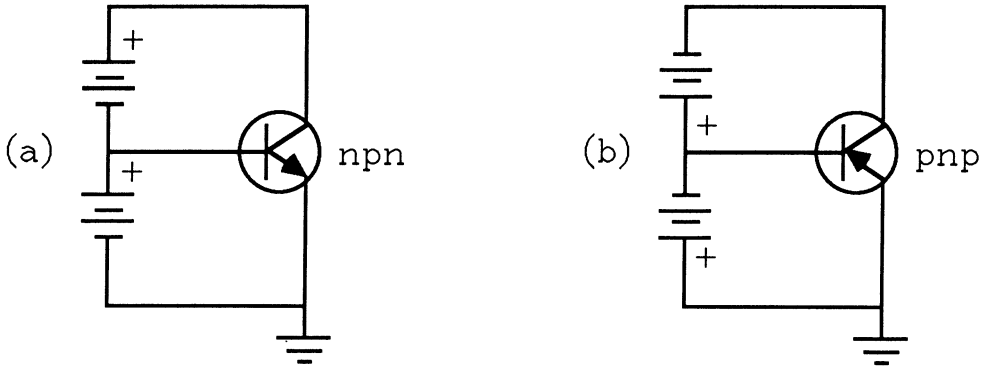
DC CHARACTERISTICS OF BJTs AND FETs

Before we can understand how to design circuits usings BJTs and FETs we must review their basic properties. These basic properties are functions of the operational mechanisms of these devices, i.e. the solid state physics which is covered in other courses. The bipolar transistor, or BJT, comes in two types: npn and pnp referring to the physical construction of the device. The npn transistor is a thin slice of p-type material sandwiched between two slabs of n-type material as shown below.

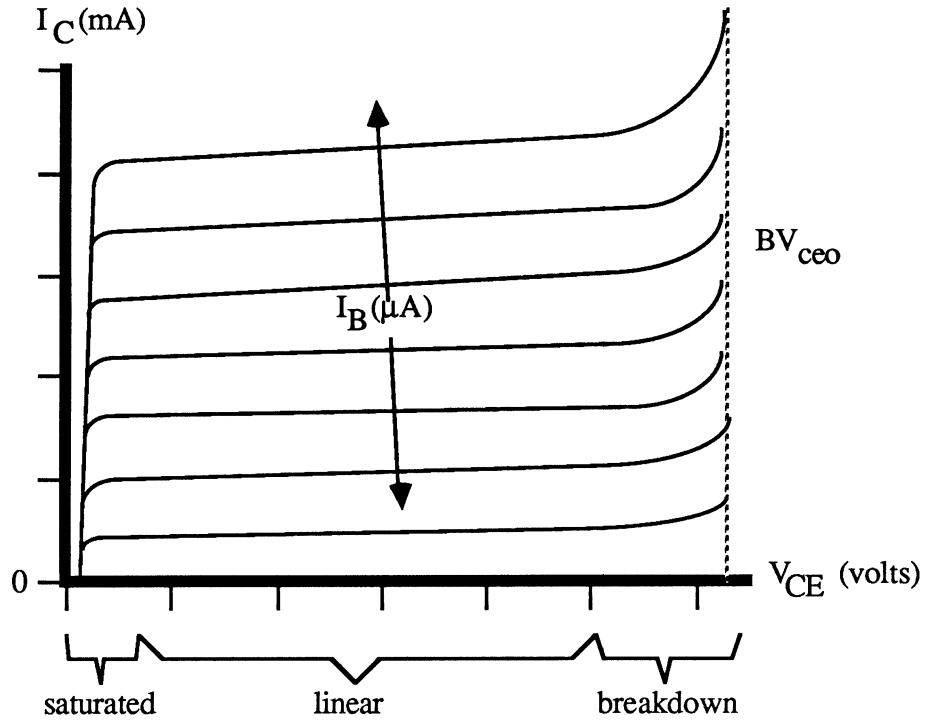


The middle layer is called the base; the substrate (or base upon which the entire structure is fabricated) is called the collector; and the top layer is called the emitter. The net result of this construction is that two diode junctions are formed: one between the collector and base and the other between the base and emitter. In practice, both transistor junctions (the diodes referred to above) are forward biased. Proper bias for npn and pnp transistors are shown below.



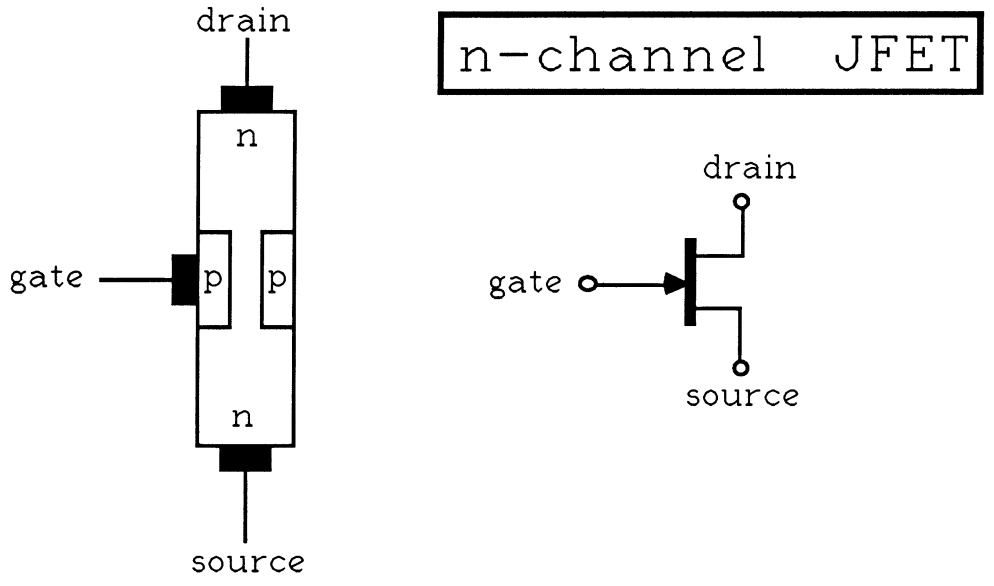
The net result of this bias is that current continuously flows through the junctions of the transistor; however, it is the relative magnitudes of these currents and the relationships between these currents that make the transistor an amplifier. For an npn transistor we can regard current as entering the transistor at both the base and collector and exiting at the emitter. This makes the emitter current the sum of the collector and base currents. The base current is quite small, however, and controls the collector current. The ratio of collector current to base current is the dc beta of the transistor and is denoted by β_{DC}. This ability to amplify current is what makes the bipolar transistor so useful, and even though the primary mode of operation of the BJT is current based, it can usefully function as a voltage and power amplifier when placed in a proper circuit.

The operation of the BJT can be summarized in the relationship between the base current I_B, the collector current I_C and the collector-emitter voltage V_{CE}. The exact relationship can be derived only after a fair digression into physical electronics. Suffice it to say that all bipolar junction transistors have characteristics similar to those shown in the graph below.



For amplifier operation the BJT is used in the "linear" region where the slope of the I_C–V_{CE} curve is almost constant. This linear region makes possible an amplifier with very little distortion as will be discussed later. One wants to avoid operation, for amplifiers, in the saturated region characterized by small V_{CE} (typically 0.2 volts or less). Similarly, one wants to avoid operation in the region to the far right of the graph. This is the region in which large electric field strengths from the large V_{CE} can destroy the transistor junction.

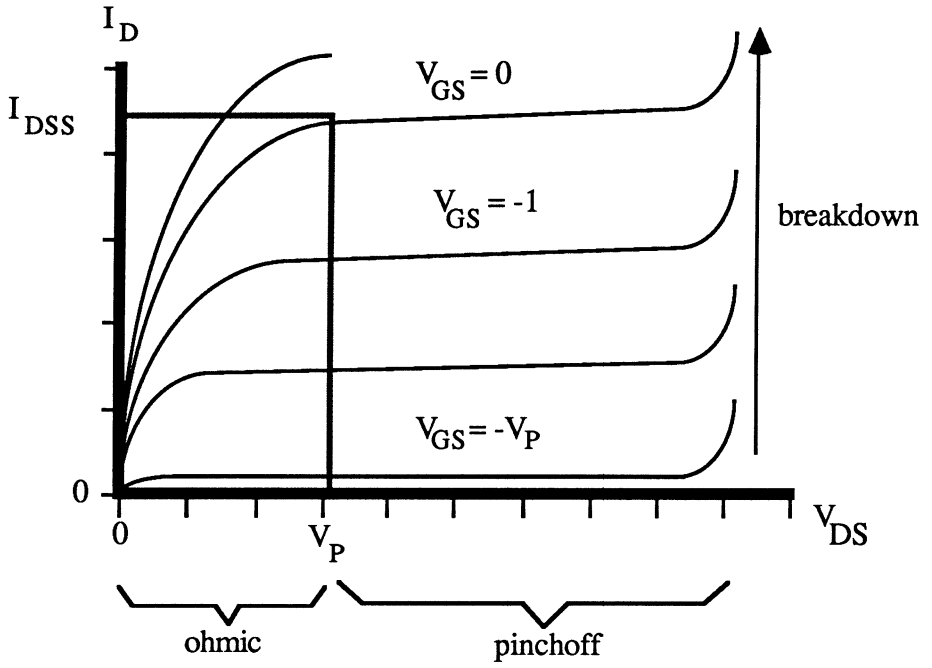
Field effect transistors, or FETs, are voltage-biased rather than current biased like BJTs. The basic structure of the FET is a thin connection between two terminals of similar semiconducting material. For example, the p-type material is used to connect two pieces of n-type material through a narrow n-type gate region as shown below. The two pieces of n-type material are known as the drain and source with current flow from the drain to the source for the FET shown below. The p-type/n-type connecting region is known as the channel region and the p-type material is called the gate.



The drain current is at its maximum value I_{DSS} when the gate-source voltage is zero. The precise definition of I_{DSS} is that it is the short circuit drain current, i.e. the drain current that flows when the gate is shorted to the source. For operation of the FET as a control device the gate-source voltage must be negative. This creates a reverse biased diode and produces a depletion region in the neighborhood of the gate. This depletion region reduces the amount of free carriers and consequently reduces the current flow between the source and drain. As the gate-source potential becomes more negative it eventually reaches a point called the pinchoff voltage V_P where the gate depletion regions close together and the source-drain current becomes essentially zero. The relationship between the drain current and V_{GS} is a square-law relationship:

$$I_D = I_{DSS}(1 - \frac{|V_{GS}|}{V_P})^2$$

The pinchoff voltage (actually $-V_P$) is also the drain-source voltage which marks the boundary between the ohmic and pinch-off regions of operation of the FET. Essentially, the FET behaves like a variable (but non-linear) resistance in the ohmic region and then remains essentially constant for $V_{DS} > V_P$. For amplifiers it is this linear or pinch-off region that is of interest. In the pinch-off region the drain current is almost linearly proportional to the V_{GS} and independent of V_{DS} (see graph below).



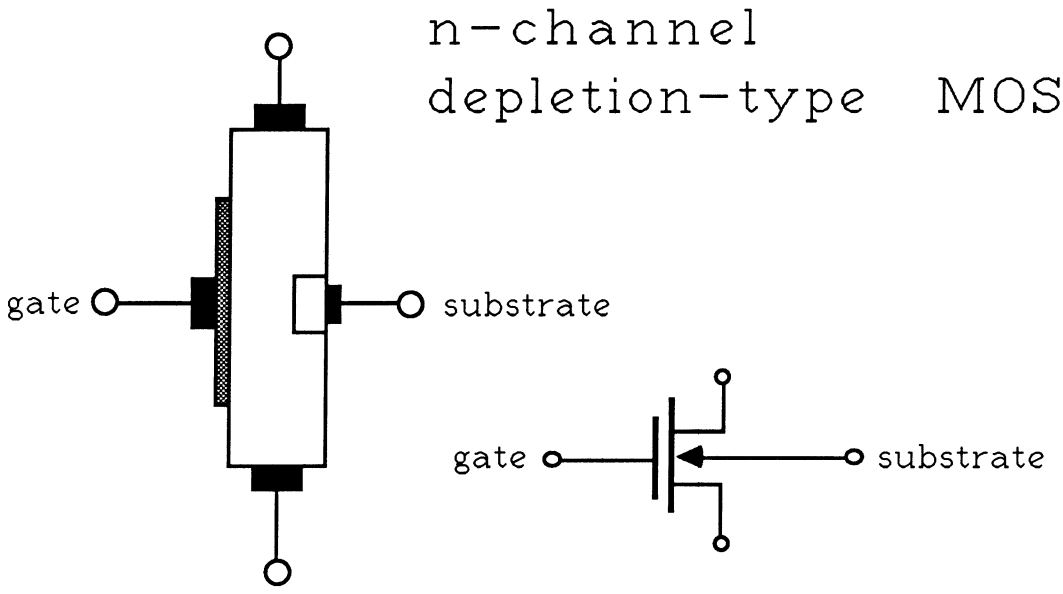
The ratio of change in I_D to the corresponding change in V_{GS} is known as the device transconductance g_m and is of fundamental concern when using the FET as an amplifier. The transconductance when the gate-source voltage is zero is denoted by g_{mo} and is often specified by the transistor manufacturer. The transconductance g_{mo}, the drain saturation current I_{DSS} and the pinch-off voltage V_P are all related by the relationship

$$g_{mo} = \frac{2I_{DSS}}{|V_P|}$$

where $|V_P|$ is the absolute value of the pinch-off voltage.

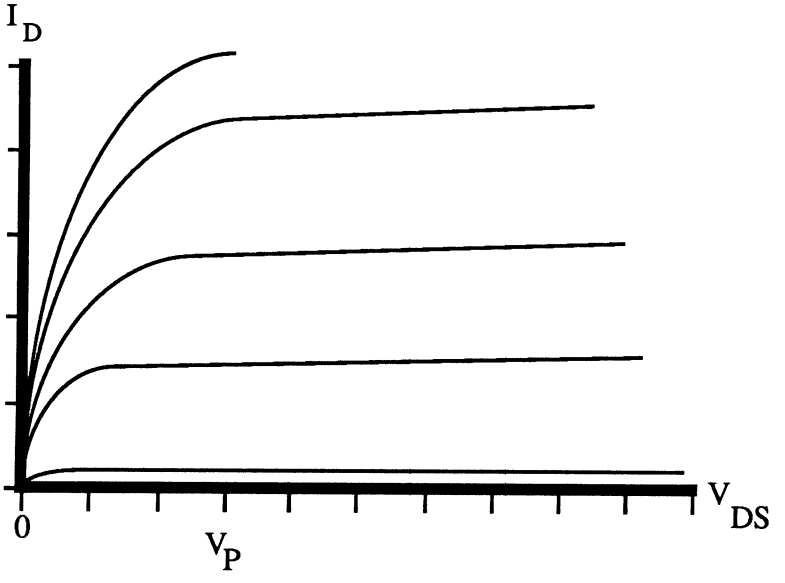
The above discussion was for a n-channel junction FET, or JFET for short. The same device with the semiconductor materials reversed is known as a p-channel JFET.

There is a special version of the JFET known as the MOSFET which is of particular interest in this course. The MOSFET or Insulated Gate FET, is a FET in which a silicon dioxide layer electrically insulates the gate electrode from the rest of the transistor. The internal structure of a MOSFET is shown below.



Since the FET operates by the electrode field created between the gate and the drain and source regions the insulated gate FET also functions in the same manner as an ordinary FET. However, the insulated gate now shifts the gate-source voltages and effectively reduces any already small gate currents to effectively zero.

MOSFETs are characterized as enhancement or enhance/depletion mode devices depending upon the properties of the channel. In enhancement mode MOSFETs the drain current increases as V_{GS} increases;however, the channel only exists when V_{GS} is greater than a certain threshold voltage V_T. In enhancement/depletion mode MOSFETs the drain current increases as V_{GS} increases and the FET will continue to operate for $V_{GS} > 0$. Note that enhancement mode MOSFETs are the only type of FET which can operate with a forward biased gate. It must be pointed out that the polarity of V_{GS} is determined by the type of the bulk semiconducting material. Characteristic curves for n-type (not n-channel) enhancement and enhancement/depletion MOSFETs are shown below.

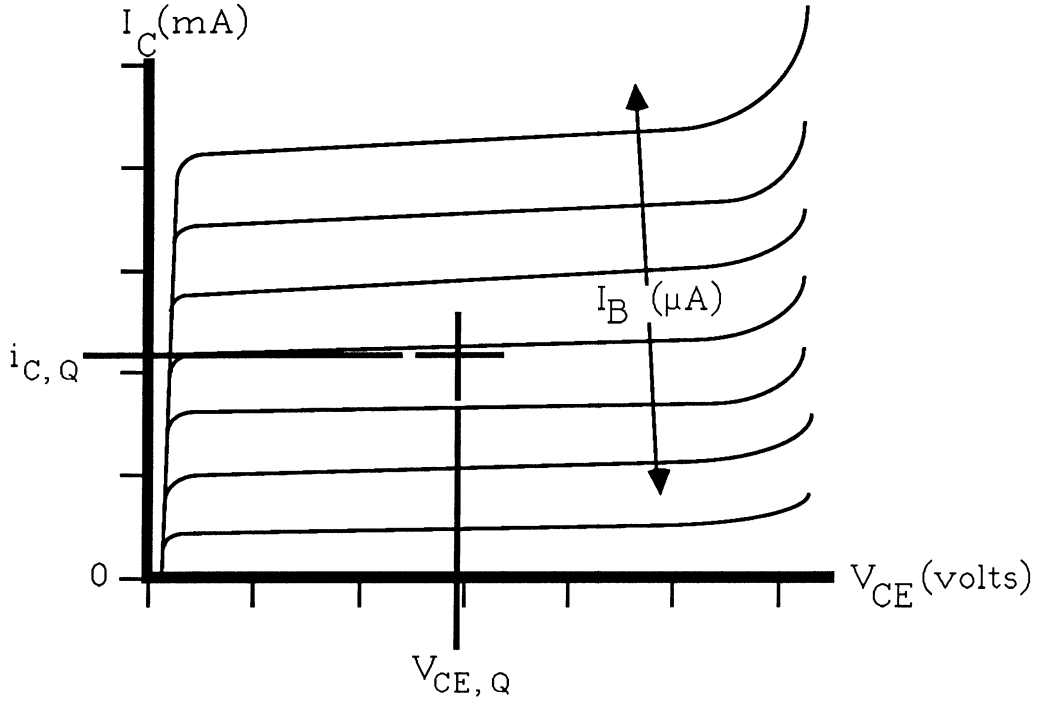


V_{GS}	
enhancement	enhancement /depletion
+5	+2
+4	+1
+3	0
+2	-1
+1	-2
0	

The structure of the MOSFET is such that multiple gates can be fabricated for a common drain-source geometry. This allows the MOSFET to be used for logic circuits and active devices such as mixers where it is important to keep the device inputs electrically isolated from each other.

AMPLIFIER PRINCIPLES

The basic dc characteristics of BJTs and FETs have been developed in previous sections. In this section we will see how those characteristics can be used to permit amplification of current or voltage mode signals.



Consider the basic dc characteristics curve of a npn BJT shown above. The collector current is a function of both I_B and V_{CE}. To understand the operation of the npn BJT as an amplifier write

$$i_C = f(v_{CE}, i_B)$$

and expand i_C in a Taylor series about the initial collector-emitter voltage and base current as shown below

$$i_C \simeq i_{C,Q} + \Delta v_{CE} \frac{\partial f(v_{CE}, i_B)}{\partial v_{CE}} + \Delta i_B \frac{\partial f(v_{CE}, i_B)}{\partial i_B}$$

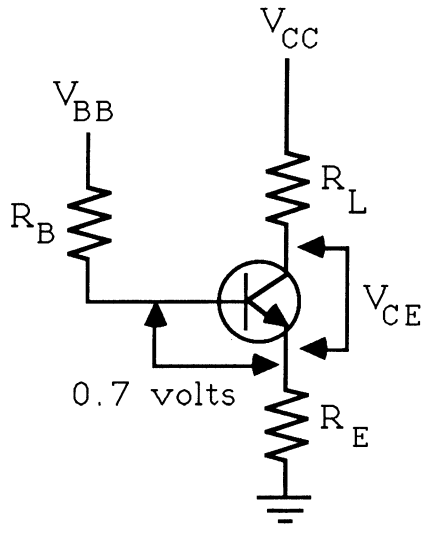
The above expression does not seem to resemble an amplifier, but note that if our initial collector-emitter voltage and base current are situated in the "linear" region of the characteristic

curve the partial derivative of collector current with respect to collector-emitter voltage must be approximately zero. This allows us to re-write the above expression as

$$\Delta i_C = i_C - i_{C,Q} \simeq \Delta i_B \frac{\partial f(v_{CE},\ i_B)}{\partial i_B} = \Delta i_B \beta$$

which indicates that any change in base current causes a change in collector current. If the change in collector current is larger than the change in base current we have an amplifier. This is an important concept and is the reason why we always operate amplifiers in the so-called "linear" part of their operating curves – to remove the function dependence and make the amplification a simple constant.

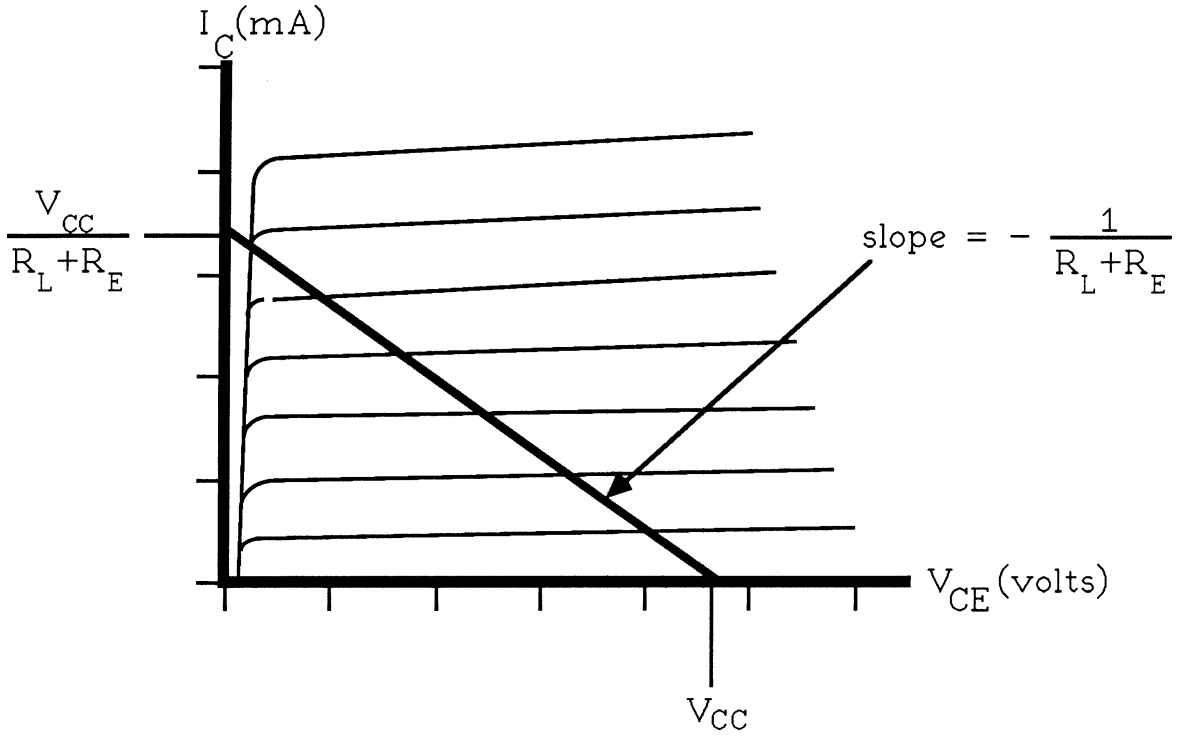
Now that we understand the mathematics of a BJT amplifier, what circuit topology do we need to implement the amplifier? First, we need a circuit to establish an initial base current and collector-emitter voltage. A circuit which will accomplish this is shown below. Note that the collector-emitter voltage is established by the voltage drops across the emitter and collector resistors. The base current is determined by the base resistance, the voltage drop across the base-emitter junction (about 0.7 volts for a silicon BJT), and the voltage drop across the emitter resistance. Using Kirchhoff's Voltage Law we can write equations for the base and collector circuits. As noted before the emitter current is the sum of the collector and base currents; but, as the collector current is usually much larger than the base current, we will use the approximation that the emitter current is approximately the collector current, $I_C \simeq I_E$.



The equation for the collector current can be re-written as

$$I_C = \frac{V_{CC}-V_{CE}}{R_L+R_E} = \frac{V_{CC}}{R_L+R_E} - \frac{V_{CE}}{R_L+R_E}$$

and, when plotted on a transistor characteristic curve as shown below, has a simple interpretation. The first term is the y-intercept of the equation and represents the collector current for zero collector-emitter voltage. This zero collector-emitter voltage corresponds to the transistor condition known as "saturation" and will produce the maximum collector current. From our characteristic curves we see that saturation occurs when the collector-emitter voltage drops below approximately 0.2 volts. The second term is simply the slope of the relationship between the collector-emitter voltage and the collector current. Because any output voltage must be developed across the resistors used in this expression it is called the "load line."



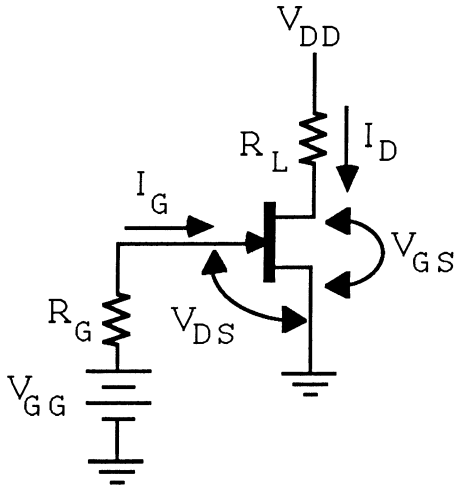
The load is represented by the equation we wrote above to model the transistor load (collector) circuit. The second equation relates the emitter current (assumed to be approximately the collector current), the base current and the base-emitter voltage. This latter voltage represents the voltage drop across the forward biased base-emitter junction which looks like an ordinary silicon diode with a constant voltage drop of approximately 0.7 volts. To solve this equation

$$V_{BB} = I_B R_B + V_{BE} + I_C R_E$$

we note that the collector current is known from the load line; the solution of this second equation then represents the intersection of the load line with a characteristic curve for a constant base current. The only additional consideration is that this solution must lie in the transistor's "linear" region if it is to be used as a good amplifier. The simultaneous solution of these two equations is known as the Q-point (or quiescent point) and represents the dc (or steady) state of the transistor. Returning to the Taylor series expansion of the collector current we see that once the Q-point has been selected according to the above equations any small variation in base current will cause

a larger variation in collector current. This is the basis of amplification in a BJT.

A similar situation holds true for a FET except that the circuit is somewhat simpler to analyze. Consider the common-source FET amplifier shown below.



We can write the equation of a load line for the drain-source circuit:

$$I_D = \frac{V_{DD} - V_{DS}}{R_L} = \frac{V_{DD}}{R_L} - \frac{V_{DS}}{R_L}$$

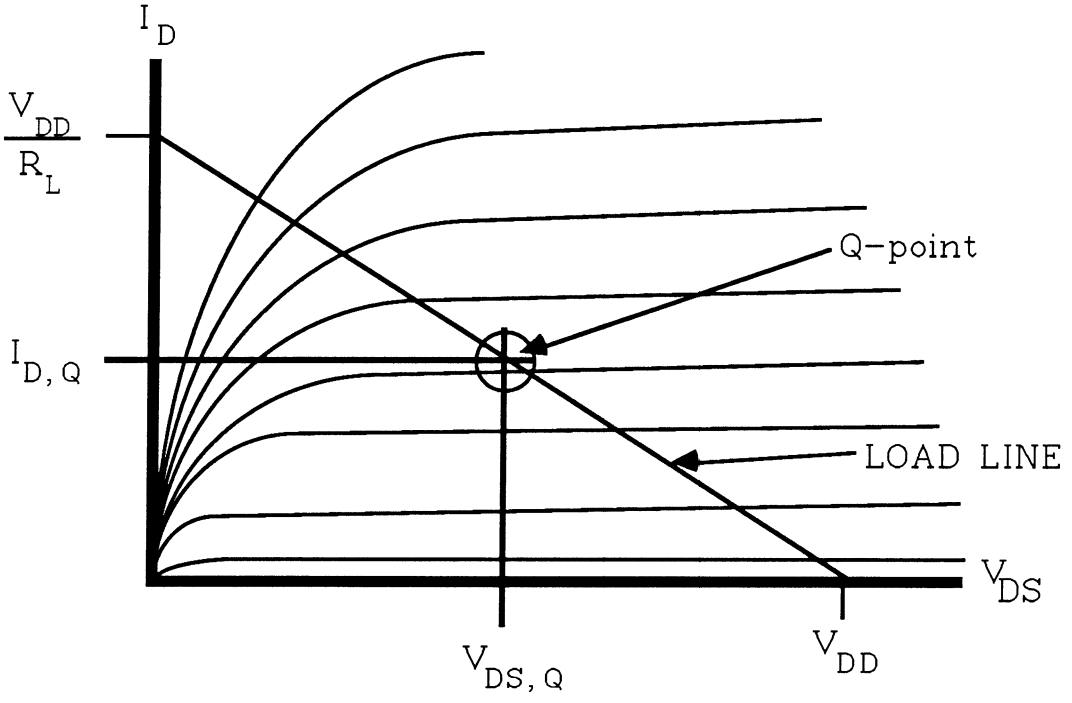
The situation seems more complicated for the gate-source junction than for the BJT. KVL yields an equation which includes the gate current, source current and the gate-source voltage.

$$V_{GG} + I_G R_G + V_{GS} = 0$$

This equation is in three unknowns and we have only two equations. The solution is much simpler than it appears because the effective gate current is zero. There is at most a small leakage current through the gate which can be ignored for most practical purposes. Consequently, KVL for the gate circuit yields

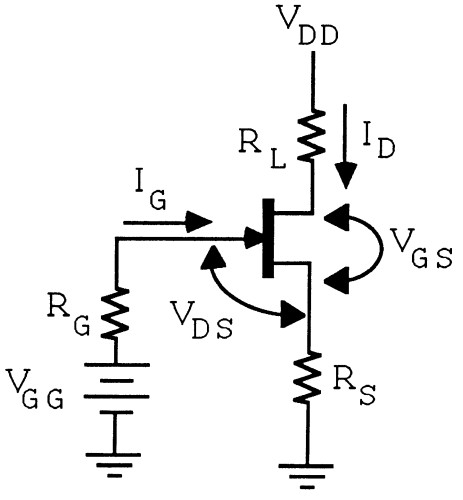
$$V_{GG} \simeq -V_{GS}$$

This situation is nearly identical to that for the BJT. We can plot the load line on the transistor characteristic curve as shown below.



This gives us an equation which will accept a number of gate-source voltages as solutions. If we pick a gate-source voltage which places us in the center of the FETs linear region, we can use the resulting circuit as an amplifier.

Consider the common-source amplifier shown below.



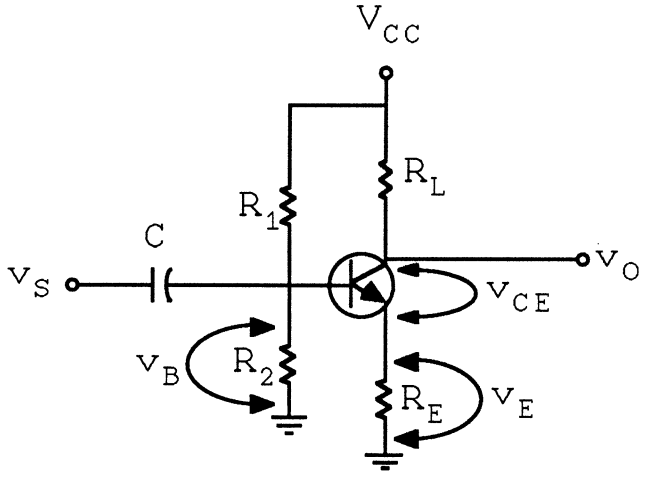
The device has both drain and source "load" resistors which establish the Q-point for the drain-source circuit. To bias the circuit we must choose an appropriate gate-source voltage on the characteristic curve. However, how do we pick the gate resistor shown in the circuit above to create a gate-source voltage other than zero? The answer is simple, the gate current I_G which we previously ignored and will continue to neglect is so small that the voltage drop across the gate resistor can be neglected. The gate bias voltage V_{GG} is set to zero and R_G connected directly to ground putting the gate potential V_G at zero volts. The source, on the other hand, is at some positive potential V_S above ground. The gate to source potential is then V_G-V_S which is the required negative potential. There is a very small "leakage" current through the gate; however, this leakage gate current is so small that R_G must be very large for most FETs – on the order of ½-2 Megohms or more – and a good "rule of thumb" is to use a ½ to 1 MΩ resistor to bias a JFET. A more sophisticated analysis would reveal that R_G can be selected to optimize the bias stability of the amplifier just as the emitter resistor can be selected to stabilize the bias point of a BJT.

DESIGN NOTES FOR COMMON EMITTER BJT AMPLIFIER

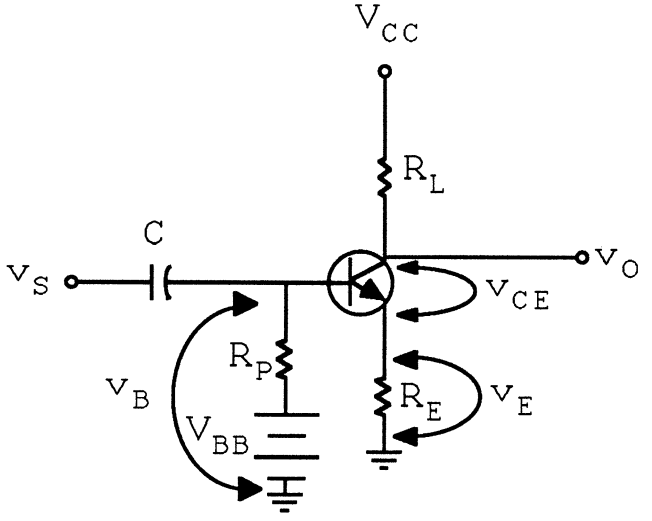
These notes were prepared in collaboration with an experienced circuit designer and represent an attempt to present the philosophy and procedures which are normally used by the design engineer. In order to understand the procedure the first part of this section gives a brief review of the analysis of the common-emitter amplifier.

ANALYSIS

The circuit to be analyzed is the self-biased common-emitter amplifier shown below.



By Thevenizing the bias circuit the above circuit can be re-drawn as



where

$$R_P = \frac{R_1 R_2}{R_1 + R_2}$$

and

$$V_{BB} = V_{CC} \frac{R_2}{R_1+R_2}$$

A common emitter amplifier (or any other type of amplifier) usually has a non-linear relationship between the input and output signal (in spite of the attempts of the circuit designer to make this relationship linear). This is called the transfer characteristic of the amplifier and is shown in Figure 2 for a common emitter BJT amplifier[1]. In biasing such an amplifier the designer's primary objective is to set $V_{CE,Q}$ such that $V_{CE,Q}$ is in the center of the linear region of the transfer characteristic as shown below[2].

The quiescent output voltage $V_{O,Q}$ is given by

$$V_{O,Q} = V_{CC} - I_C R_C \qquad (1)$$

where I_C is related to the base current I_B by

$$I_C = \beta_{DC} I_B \qquad (2)$$

and we are using β_{DC} to denote the dc beta of the transistor. Thus, if we are to establish a particular $V_{O,Q}$ we must set the base current to the appropriate value. Using KVL around the base-emitter loop, we can get an expression for $I_{B,Q}$

[1]A more detailed discussion of an amplifier's transfer characteristic can be found in Senturia and Wedlock, Electronic Circuits and Applications, p.256–259.

[2]The subscript Q will be used throughout this section to denote the quiescent (or bias) value of a circuit variable.

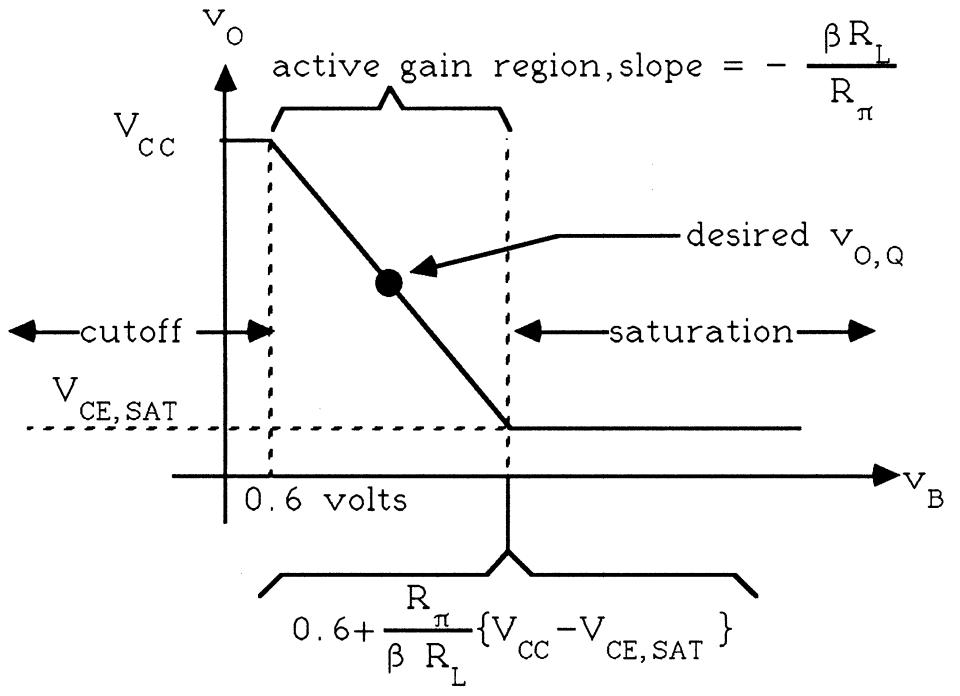


Figure 2 – COMMON EMITTER AMPLIFIER TRANSFER CHARACTERISTIC[3] [R_π is the base input impedance of the transistor]

$$I_{B,Q} = \frac{V_B - 0.6}{(\beta+1)R_E} \qquad (3)$$

So, if $\beta >> 1$, equation (1) becomes, using (3),

$$V_{O,Q} = V_{CC} - (V_B - 0.6)\frac{R_C}{R_E} \qquad (4)$$

which is independent of β. Thus, $V_{O,Q}$ is determined by the base voltage V_B assuming that R_E and R_C are known and the circuit is properly voltage biased. We can also note that the collector current I_C is independent of R_C, at least in the linear region of operation.

Since V_B depends upon I_B (See Figure 1), we can also write (using KVL) that

$$I_{B,Q} = \frac{V_{BB} - 0.6}{R_P + (\beta+1)R_E} \qquad (5)$$

[3]Modeled after Senturia and Wedlock, Electronic Circuits and Applications, Figure 10.3

and

$$V_{O,Q} = V_{CC} - (V_{BB} - 0.6) \frac{\beta R_C}{R_P + (\beta+1) R_E} \qquad (6)$$

For quiescent, i.e. bias, point stability we require that $V_{O,Q}$ be approximately independent of β. This is true only if $\beta R_E >> R_P$ in Equation (6). If this is true, Equations (5) and (6) become

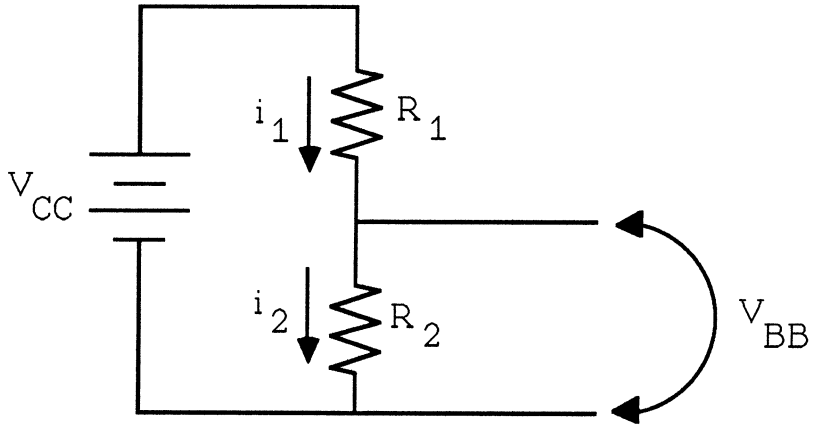
$$I_{B,Q} = \frac{(V_{BB} - 0.6)}{(\beta+1) R_E} \qquad (5a)$$

and

$$V_{O,Q} = V_{CC} - (V_{BB} - 0.6) \frac{R_C}{R_E} \qquad (6a)$$

If we compare these equations with equations (3) and (4) we see that they are of identical form, and that if $\beta R_E >> R_P$, then $V_B = V_{BB}$. The result would be the same as requiring $\beta R_E >> R_P$.

To determine what we must do to make $V_B = V_{BB}$ let's go back to the original circuit and consider the voltage divider which is connected to that base lead. Physically, V_B is the voltage at the base of the transistor and V_{BB} is the Thevenized equivalent voltage of the unloaded bias network. Only when the loading is "light" can $V_{BB} = V_B$.

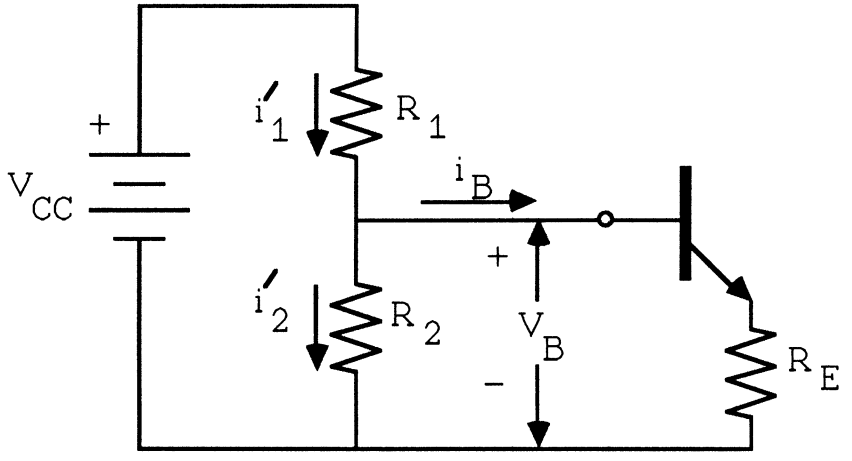


With no load connected to the output terminals of the bias network, $i_1 = i_2 = i_D$ (the D stands for divider) and the output voltage is given by

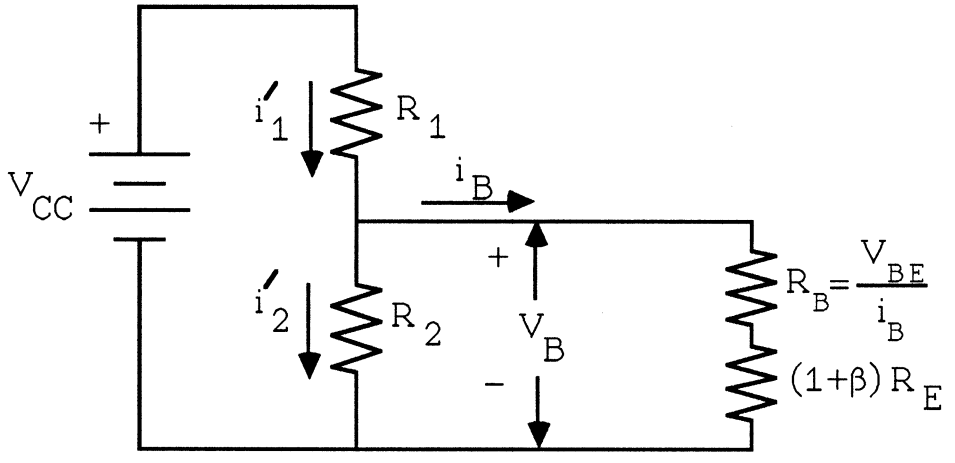
$$V_{BB} = V_{CC} \frac{R_{CC}}{R_1+R_2} \tag{7}$$

$$i_1 = i_2 = \frac{V_{CC}}{R_1+R_2} \tag{8}$$

If we now connect the transistor, we have



which becomes



and i_1 and i_2 (now labeled i_1' and i_2') are no longer equal so $V_B < V_{BB}$. If, however, we make I_B small relative to i_1' and i_2', very little additional current flows when the divider is connected to the transistor, so $V_B \approx V_{BB}$. The importance of this result is that requiring i_B to be small relative to i_1' and i_2' yields the same result as requiring $\beta R_E >> R_P$.

By requiring that $i_B << I_D$ (and subsequently that $i_1 = i_1'$, $i_2 = i_2'$ and $i_D = i_1 = i_2$ = current in the unloaded base bias voltage divider) we have simplified our design calculations. Using KVL across the transistor input

$$V_B = V_{BE}+V_E = V_{CC}\frac{R_2}{R_1+R_2} \qquad (9)$$

Also note that

$$i_B = \frac{i_C}{\beta} \qquad (10)$$

To be certain that $I_D >> I_B$, let $I_D = 10I_B$. This is a reasonable engineering approximation giving

$$i_D = 10i_B = \frac{V_{CC}}{R_1+R_2} \qquad (11)$$

If we know V_{CC} we can easily calculate R_1 and R_2 from Equations (9) and (11) directly without bothering with R_P and V_{BB}.

Up to now we have only considered the dc biasing of the circuit. The ac model of our unbypassed (emitter resistor) amplifier is shown in Figure 3 where we have used h_{fe} as being equivalent to β_{AC}, the ac beta of the transistor.

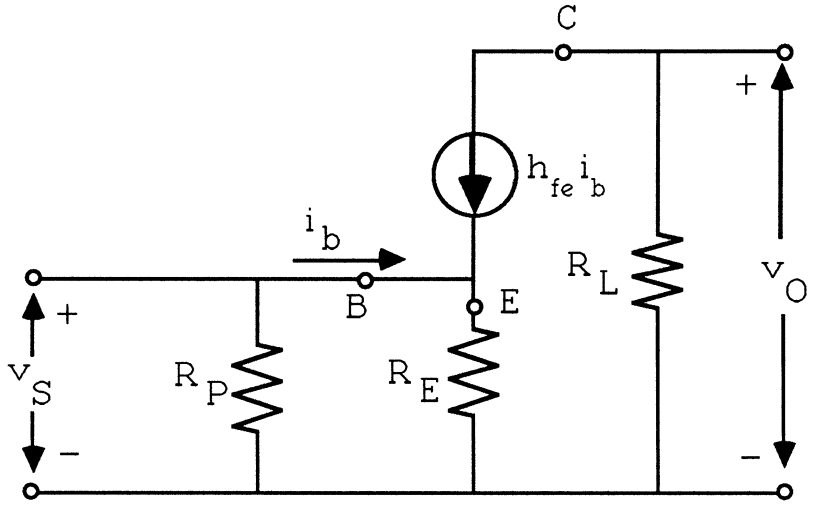


Figure 3 - Common emitter amplifier using tee model

Figure 3 uses a very simplified tee[4] model of a common emitter transistor. A node-loop analysis of Figure 3 gives us the ac small signal voltage gain A_V as

[4]A more comprehensive discussion of the tee model can be found in:

$$A_V = -\frac{R_L}{R_E} \qquad (12)$$

Equation (12) completes the basic relationships we need to design a transistor amplifier.

DESIGN

Design (synthesis) is different from the analysis techniques presented in most textbooks. The designer must consider the interactions between component values and circuit performance as values are selected. Furthermore, the amplifier specifications are constraints which must be satisfied. Unspecified parameters such as input impedance may be varied to design an amplifier which meets the given design criteria. Each design is unique.

Consider the trade-offs available in the circuit of Figure 1. Resistors R_1 and R_2 control the base voltage, thereby affecting the operating point $V_{O,C}$. They do not affect voltage gain, swing or supply voltage, but their values are dependent upon V_{CC}. Input impedance, however, is usually a strong function of R_2 because in practice $R_2 << R_1$ (usually).

Gain, swing and operating point vary with R_C and R_E. Collector current is dependent upon R_E but not on R_C. For the circuit of Figures 1 and 3 the output impedance is approximately R_C. The input impedance is affected by R_E in the cases where R_E is small or R_2 is large.

Frequency response is set by C, R_1, R_2, R_E and β. Supply voltage requirements are related to R_C, R_E, operating point and voltage swing.

A design procedure might start by selecting a value for the emitter voltage. This is a suitable starting point because it determines R_E (when the quiescent collector current $i_{C,Q} = i_{E,Q}$ is specified) which affects nearly every parameter of the amplifier. A value of 1–2 volts for V_E (occasionally you will find V_E up to three volts) is suitable. This value is selected for thermal stability and to be larger than the peak negative input voltage (signal) swing to prevent reverse biasing of the base-emitter junction. An alternative rule-of-thumb which does the same thing (usually) is to pick V_E to be about 10% of V_{CC}. After V_E is selected, $i_{C,Q} = i_{E,Q}$ fixes R_E. The nearest standard value resistance is selected for R_E and the resulting value of V_E

$$V_E = R_E i_E$$

is verified as being in the desired range.

Since the gain of the amplifier is approximately R_C/R_E, R_C is now determined if the gain was specified. Application of KVL and the specified $V_{CE,Q}$ now gives a value for V_{CC}

$$V_{CC} = v_{CE,Q} + i_{C,Q} R_C \qquad (13)$$

If the swing specification of the amplifier is satisfied by these values, the base resistors can be selected.

Precise calculations of the base current and voltages are unnecessary if the usual 10–20% tolerance resistors are used. The required base voltage V_B is given by

$$V_B = V_E + V_{BE} \tag{14}$$

The base current is given by

$$i_B = \frac{i_{C,Q}}{\beta} = \frac{i_{C,Q}}{h_{FE}} \tag{15}$$

where h_{FE} is the DC beta of the transistor. The voltage divider can now be designed to have an open circuit voltage V_B [given by Equation (14)] and a current $i_D = 10i_B$. If this procedure is followed, the loaded divider voltage will be within specification. Note that the circuit is voltage biased, i.e. V_B determines V_E, V_E determines i_E, i_E determines the operating point $V_{O,Q}$. In certain situations, particularly those where i_B is large, the rule-of-thumb cannot be followed and the designer must Thevenize the bias network to arrive at correct loaded values for the bias divider network.

As a check the base voltage V_B should be calculated from the V_{CC} and selected R_1, R_2 values. From this V_E and the other operating point can be verified. If all values are acceptable the input coupling capacitor C can be calculated from

$$f_{3db} = \frac{1}{2\pi R_{IN} C} \tag{16}$$

where R_{IN} is the small signal input impedance of the amplifier.

In the laboratory the following procedures can be used to make necessary adjustments:

1. Change the gain by varying R_C.

2. Change the bias (and the Q-point) by varying R_1.

These changes have the least effect on the other circuit parameters.