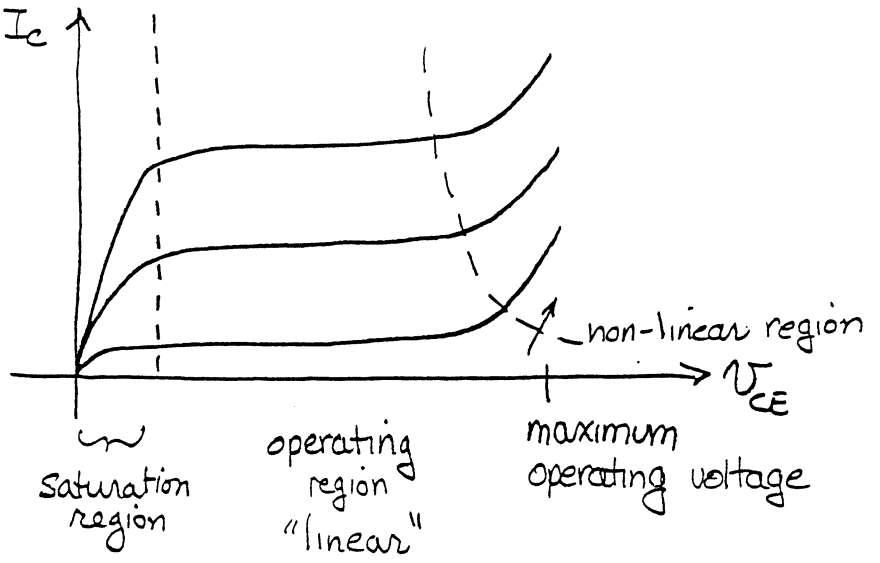
basic transistor characteristics



rules for biasing

1. stay in linear region away from boundaries
2. maintain the Q-point at a constant value for the temperature range of interest
3. minimize the effects of leakage current
4. minimize transistor-to-transistor variations

BOWICK, <u>RF CIRCUIT DESIGN</u>

"in most r.f. amplifier designs, unfortunately, very little thought is ever given to the design of bias networks for the individual transistors involved. For room temperature only no problem for reliable and specified operation (gain, NF, etc.); over large temperature extremes the dc bias network <u>MUST</u> be carefully considered."

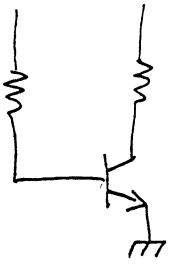
transistor parameters that are temperature dependent

V_{BE} decreases at 2.5mV/°C

β increases at ½%/°C

I_{co} increases at 4%/°C

How do we prevent temperature problems – emitter stabilization



Note: ① As V_{BE} decreases

$I_B = \frac{V_{cc} - V_{BE}}{R_B}$ increases $\Rightarrow I_c$ increases further heating the transistor

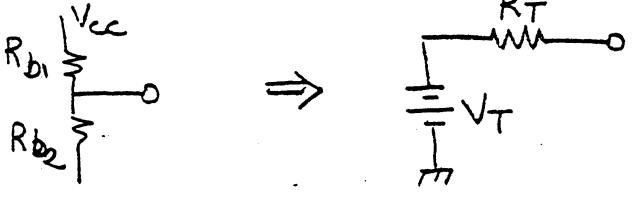
② As β increases, I_c increases

③ As I_{co} increases, I_c increases

I_{co} is the current that flows thru the collector with the emitter open and is called The CB leakage current. Small, typically $0.001 - 0.1\ \mu A$ for low power silicon transistors. Usually modeled as a small current generator.

How do we bias for constant I_E?

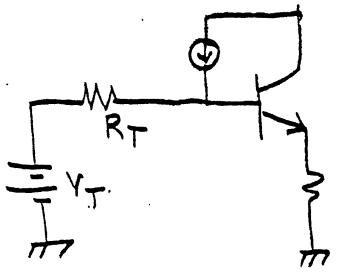
1. Thevenize the bias circuit



$R_T = R_{b1} \| R_{b2}$

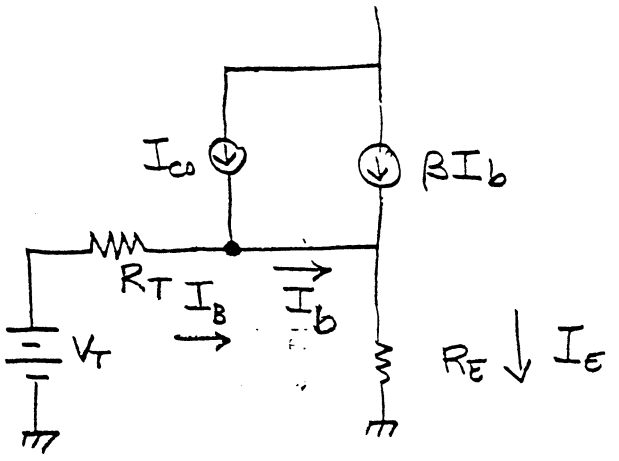
$V_T = \frac{R_{b2}}{R_{b1} + R_{b2}} V_{cc}$

2. Add I_{co} generator.



do "tee" model of circuit

the "tee" model is a large circuit model



$$I_E = (I_B + I_{co}) + \beta (I_B + I_{co})$$

two unknowns I_B, I_E

get second equation from bias loop

$$V_T - I_B R_T - V_{BE} - I_E R_E = 0 \qquad \text{KVL}$$

solve simultaneously $\quad I_B = \dfrac{V_T - V_{BE} - (\beta+1) R_E I_{co}}{(\beta+1) R_E + R_T}$

$$I_E = (\beta+1) I_b$$

$$= \frac{(\beta+1)(V_T - V_{BE}) - (\beta+1)^2 R_E I_{co}}{(\beta+1) R_E + R_T}$$

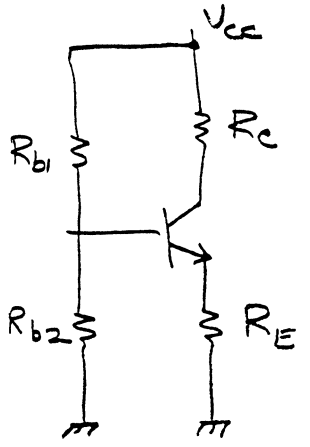
how to make independent of temperature

MAKE SECOND TERM SMALL

i.e. $\quad (\beta+1) R_E \gg R_T$

this is the stability criteria $\quad \left(\text{actually from } \dfrac{\partial I_E}{\partial I_{co}}\right)$

Example:



① from data sheets $\beta = 50$

$V_{CE} = 5$ VOLTS

$I_c = 10mA$

$P_d = V_{CE} I_c = 50\ mW$

② PICK $I_c R_E = 2$ VOLTS (A GOOD NUMBER!)
so input does not reverse bias V_{BE}

$$R_E = \frac{2 \text{ VOLTS}}{I_c} = \frac{2 \text{ VOLTS}}{10mA} = 200\,\Omega$$

③ satisify stability criteria

$(\beta+1) R_E \gg R_T$

$(\beta+1) R_E = (50+1)(.2K) = 10.2K$

PICK $R_T = 1K$

④ from input loop

$$V_T - R_T\left(\frac{I_c}{\beta}\right) - V_{BE} - I_c R_E\left(1+\frac{1}{\beta}\right) = 0$$

write in terms of I_c since we know it

$$V_T = (1K)\left(\frac{10mA}{50}\right) - 0.7 - (10mA)(.2K)\left(1+\frac{1}{50}\right)$$

$$= 0.2 + 0.7 + 2.04 = 2.94 \text{ volts}$$

End first lecture

(5) solve for R_{b1}, R_{b2}

$$V_T = \frac{R_{b1}}{R_{b1} + R_{b2}} V_{cc} \qquad R_T = \frac{R_{b1} R_{b2}}{R_{b1} + R_{b2}}$$

$\Rightarrow$ pick V_{cc} = 10 VOLTS AS AN EXAMPLE

$$\frac{2.94}{10} = \frac{R_{b1}}{R_{b1} + R_{b2}} \qquad 1 = \frac{R_{b1} R_{b2}}{R_{b1} + R_{b2}}$$

Same factors

$$\therefore R_{b2} = \frac{R_{b1} + R_{b2}}{R_{b1}} = \frac{10}{2.94} = 3.4K$$

$$10 R_{b1} = 2.94 (R_{b1} + R_{b2})$$

$$R_{b1} = 0.294 R_{b1} + .294(3.4K)$$

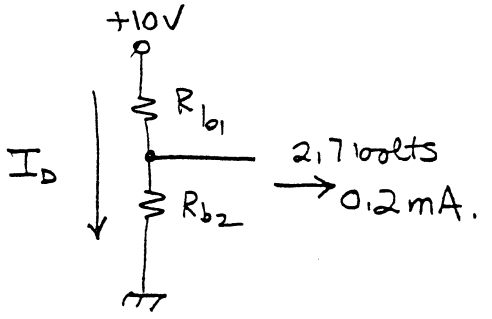
$$R_{b1} = 0.294 R_{b1} + 999.6$$

$$R_{b1} = \frac{999.6}{0.706} = 1416 \Omega$$

Another method which is simpler, find i_B and make bias divider current ten times i_B.

$$\text{since } i_B = \frac{10mA}{50} = 0.2mA = 200\mu A$$

$$V_B = 0.7 + 2.0 = 2.7 \text{ volts}$$



pick $I_D = 2mA$ then $R_{b_1} + R_{b_2} = \frac{10}{2mA} = 5K$ Ohm's Law

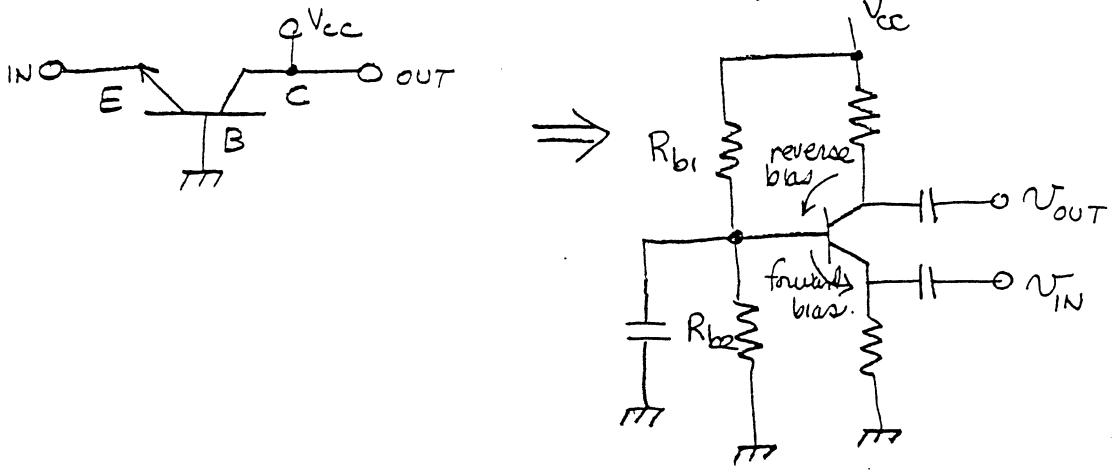
voltage divider $\frac{R_{b2}}{R_{b_1}+R_{b2}}(10 \text{ volts}) = 2.7 \text{ volts}$

$$\Rightarrow R_{b2} = \left(\frac{2.7}{10}\right) 5K = 1.35K$$

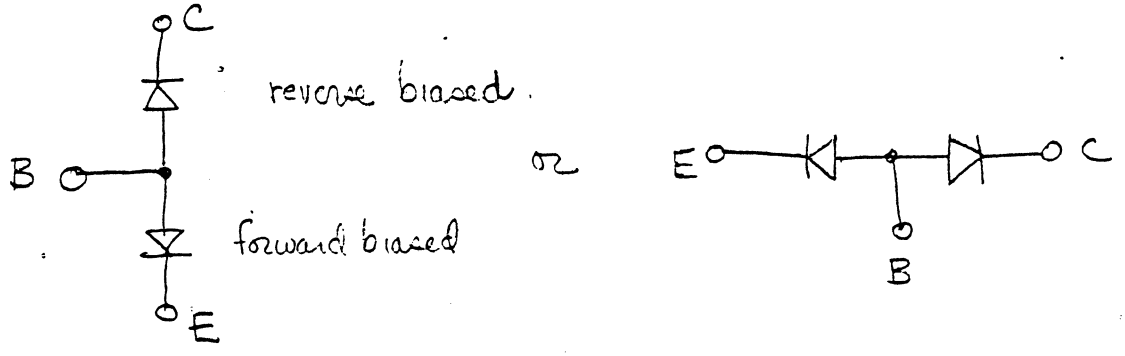
Comparison:	$10\, i_B$	stability criteria
R_{b_1}	3.65K	3.41K
R_{b_2}	1.35K	1.42K

basic small signal models

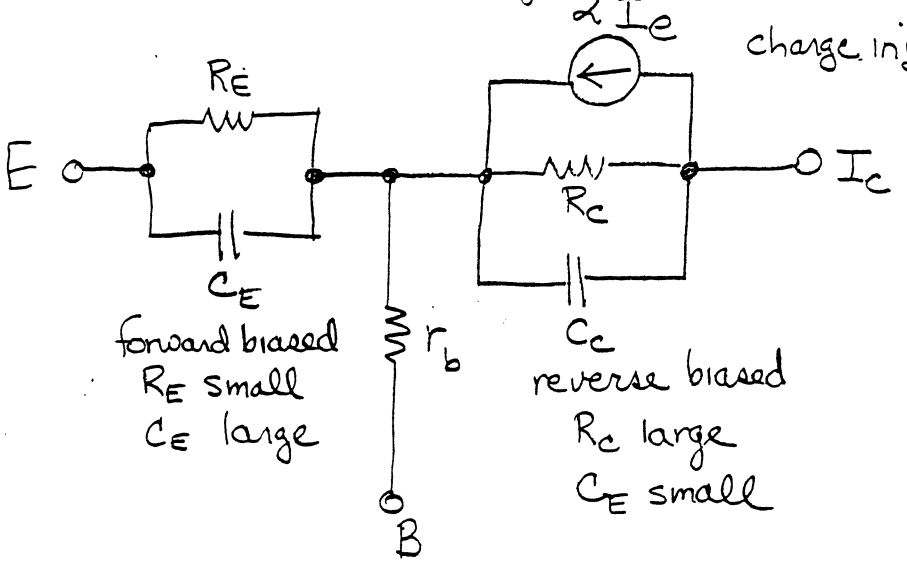
common base amplifier (as an example)



tee equivalent circuit — diode equivalent circuit



actual tee model substitutes equivalent circuits for each transistor



This is a high frequency model suitable for SPICE

r_b = bulk resistance of base thru active region

mathematically, a transistor ~~is~~ can be modeled as back-to-back p-n junction diodes Ebers – Moll equations

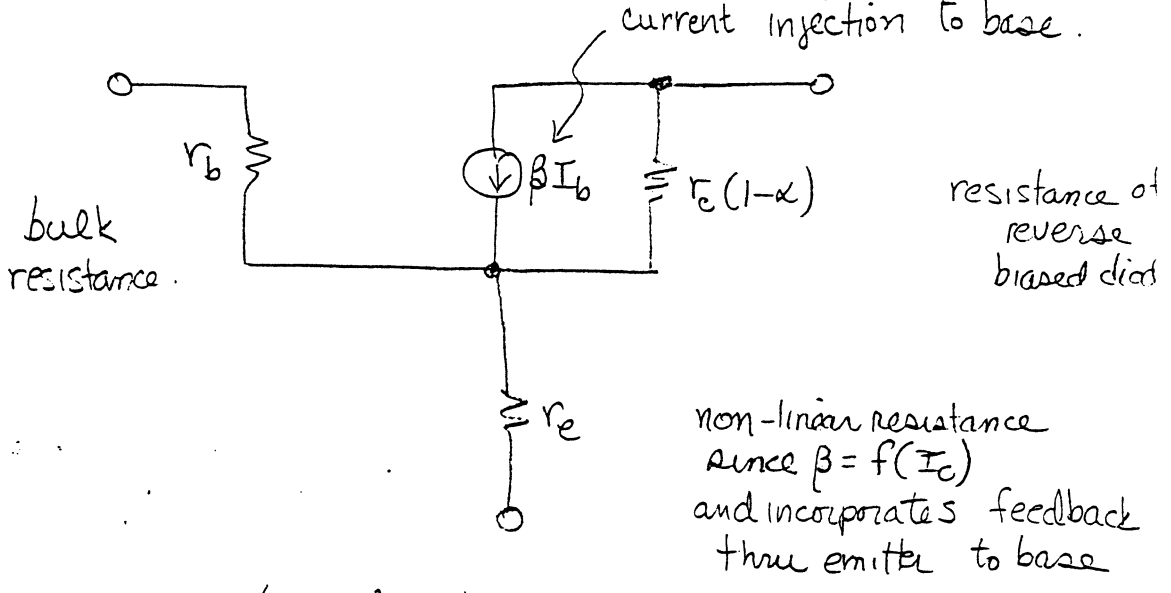
$$I_E = -I_{ES}\left(e^{\frac{V_{BE}}{V_t}} - 1\right) + \alpha_R I_{CS}\left(e^{\frac{V_{BC}}{V_t}} - 1\right)$$

$$I_C = \alpha_F I_{ES}\left(e^{\frac{V_{BE}}{V_t}} - 1\right) - I_{CS}\left(e^{\frac{V_{BC}}{V_t}} - 1\right)$$

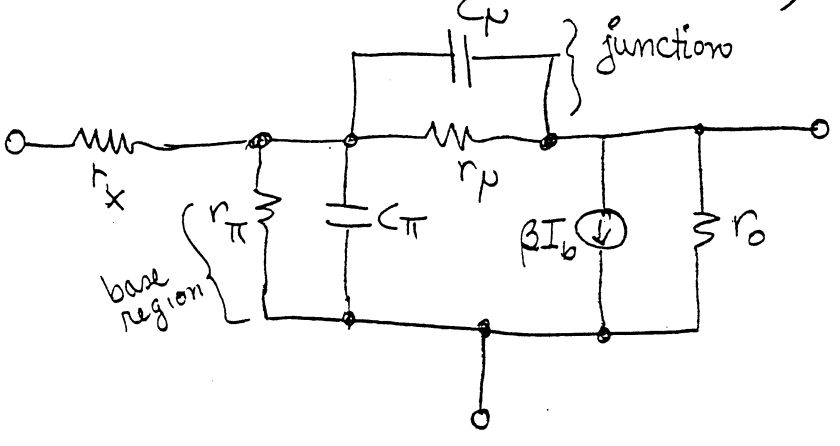
$$V_t = \frac{kT}{q}$$

I_{CS}, I_{ES} are collector and emitter saturation currents

re draw as



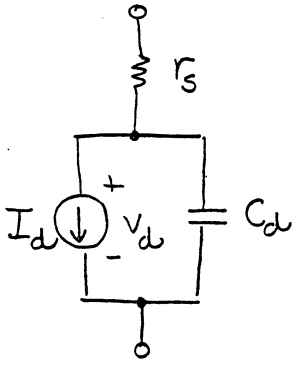
hybrid-π model (similar but not same)



tee-equivalent circuit

the tee-equivalent circuit predicts device behavior in <u>all</u> circuit regions of operation. This model is based upon a large signal CAD model for a diode:

pn-junction diode



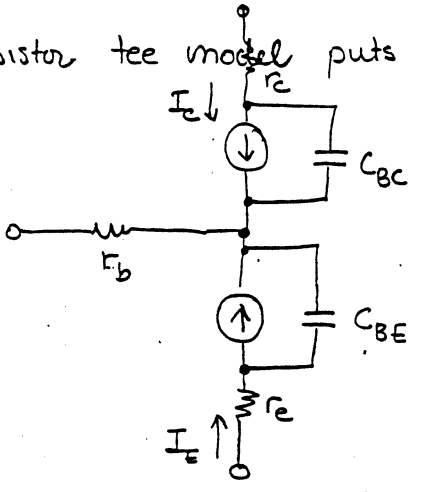
r_s = series resistance

$C_d = \dfrac{dQ_d}{dV_d}$ is a small signal capacitance (charge in depletion/diffusion layer)

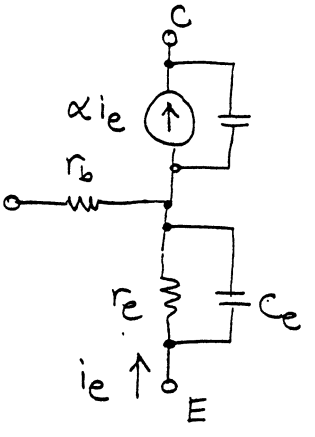
$I_d = I_s\left(e^{\frac{\lambda q}{kT}V_d} - 1\right)$

$\frac{1}{2} < \lambda < 1$ and is basically a fudge factor to match measured characteristics

The full transistor tee model puts <u>diodes back-to-back</u>.



$\Longrightarrow$ simplified



$$\alpha(j\omega) \approx \frac{\alpha_0}{1 + j\frac{\omega}{\omega_\alpha}}$$

ω_α: α-cutoff frequency

tee-equivalent circuit

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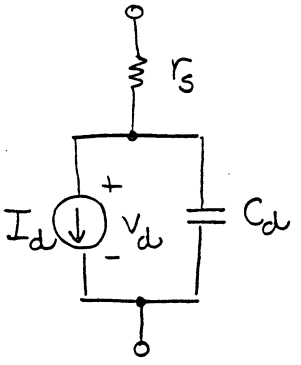

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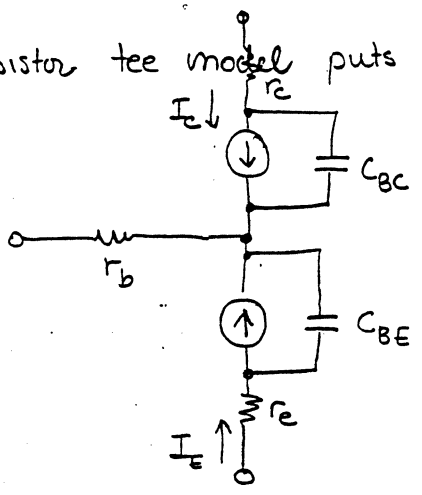
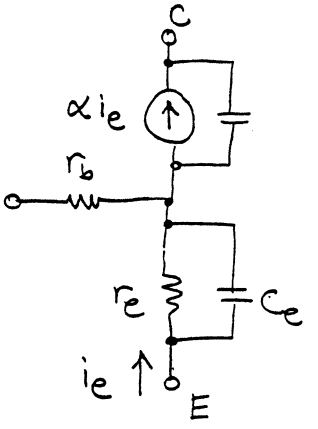


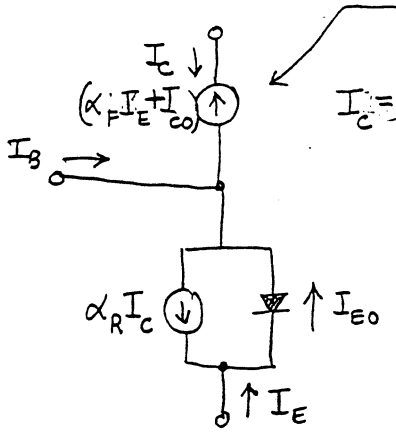
simplified ⟹



$$\alpha(j\omega) \approx \frac{\alpha_0}{1 + j\frac{\omega}{\omega_\alpha}}$$

ω_α: α-cutoff frequency.

normal region : $v_{BE} > 0$ $v_{Bc} < 0$



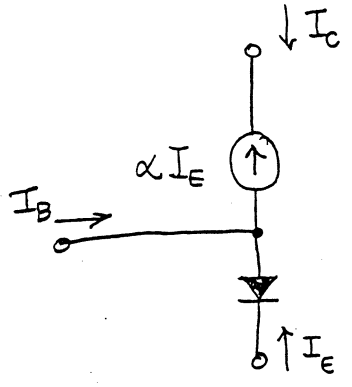
diode disappeared because it was reverse biased

$$I_C = -\left[\alpha_F I_E - I_{CO}\left(e^{\frac{V_{Bc}}{V_t}} - 1\right)\right]$$

$$\approx -(\alpha_F I_E + I_{CO})$$

I_{CO} is formally defined as the reverse collector current when $I_E = 0$ and V_{Bc} is reverse biased

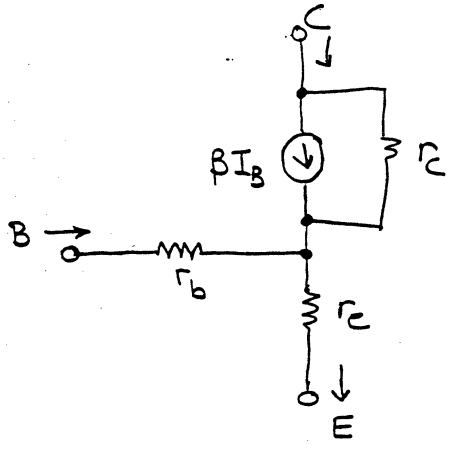
which can be further approximated by



$.9 < \alpha < 0.998$

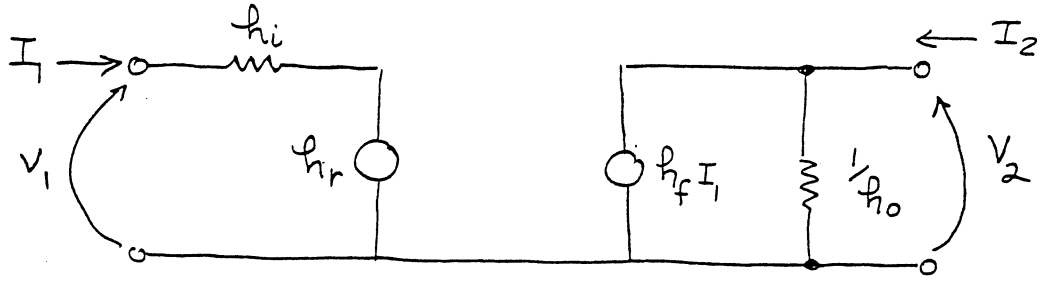
$\alpha_R \ll 1$

This model can be embelished by adding series resistances.



drawn for an NPN transistor

Another commonly used model is the h-parameter model which has no physical basis whatsoever but is easy to measure.



This <u>looks</u> very similar to the hybrid-π but is easier to manipulate and measure.

h_i = input impedance , output short circuited = $\frac{V_1}{I_1}$

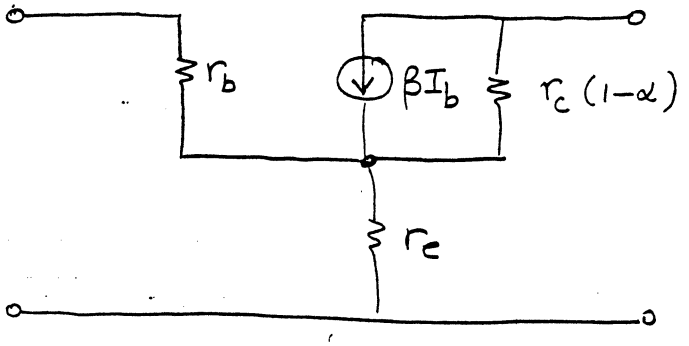
h_o = output admittance , input open = $\frac{I_2}{V_2}$

h_r = reverse voltage ratio, input open = $\frac{V_1}{V_2}$

h_f = forward current ratio, output shorted = $\frac{I_2}{I_1}$

Since h-parameters are easily measured they are often found on transistor data sheets.

- compare with basic tee model which comes from physics



$r_b \neq r_\pi$ and is the resistance of the base contact thru bulk substrate to active region

βI_b current injection to base

$r_c(1-\alpha)$ resistance of reverse biased diode

r_e non-linear resistance (since $\beta = f(I_c)$) and represents feedback thru emitter to base

Examine manufacturer's data sheets

$I_c = 1mA$, $V_{CE} = 10$ volts, $f = 1kHz$

$h_{fe} = 50-200$ $\qquad h_{FE} = 45$ (minimum)

$h_{re} =$ to 10×10^{-4}

$h_{ie} = 1-6\ k\Omega$

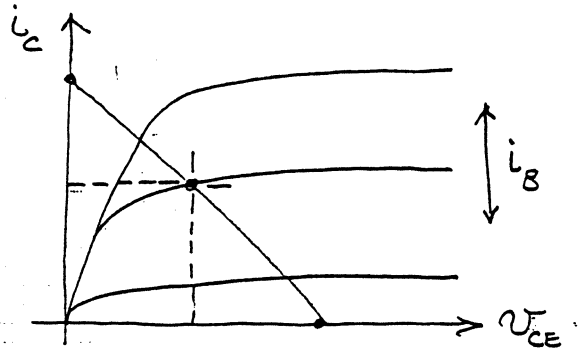
$h_{oe} = 4-40\ \mu\mho$

Can I translate these to hybrid-π? Yes.

① from physics $g_m = \frac{q}{kT}|I_c| = \frac{I_c}{25mV} = 0.04\mho$

② Note: h_{FE} = min 45 for $I_c = 1mA$, $V_{CE} = 1$ volt

$h_{fe} = 50-200$ for $I_c = 1mA$, $V_{CE} = 10$ volts



$h_{FE} = \frac{i_c}{i_B}$ this is a simple ratio or a dc quantity

$h_{fe} = \frac{\Delta i_c}{\Delta i_B}$ this is a derivative or an ac quantity

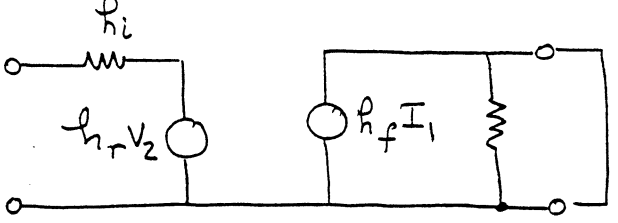
③ $r_\pi = \frac{\beta}{g_m} = \frac{h_{fe}}{g_m} \cong \frac{125}{.04} = 3125\Omega$ where the average of h_{fe} was used

④ from data sheets $h_{ie} \approx 3500$ where again an average was used.

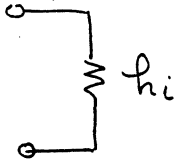
but $h_{ie} = r_b + r_\pi$ if output is shorted. At the 1kHz test frequency the capacitance can be neglected.

$r_b = h_{ie} - r_\pi = 3500 - 3125 = 375\Omega$

for h-parameter model

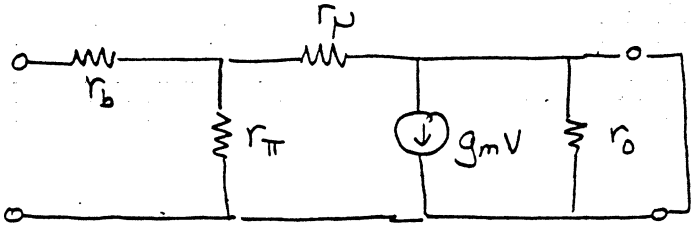


① Short output
② $h_r V_2 \to 0$ since $V_2 = 0$

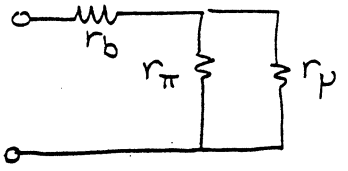


is then short circuit (output) input impedance.

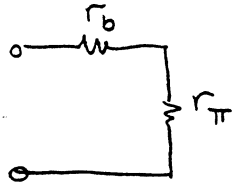
for hybrid-π model



① Short circuit output

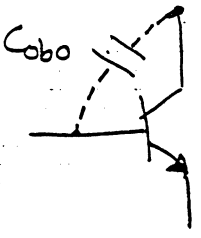


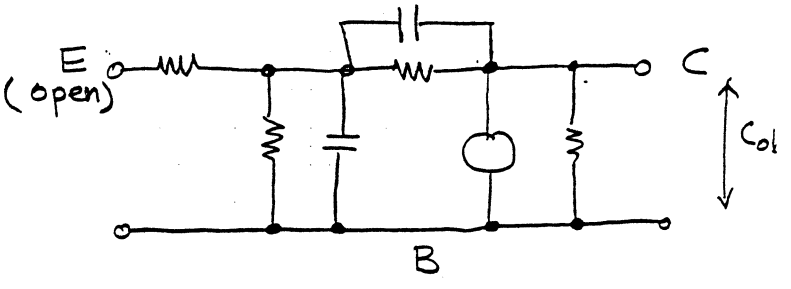
② neglect capacitances
③ $r_\mu \gg r_\pi$



At low frequencies r_b is usually negligible and it becomes a constant (on the order of 50-100 Ω) at low frequencies.

⑤ $C_{obo} \triangleq$ collector base capacitance with emitter open (in common base)



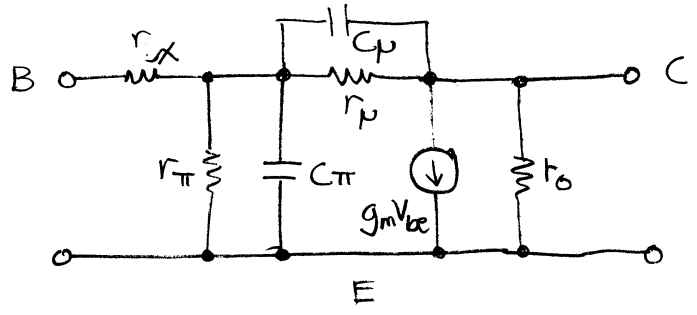


For ac two capacitors in series $C_s = \frac{C_\mu C_\pi}{C_\mu + C_\pi}$ are seen between the collector and base. But, as C_π usually $\gg C_\mu$. $C_s \approx C_\mu$.

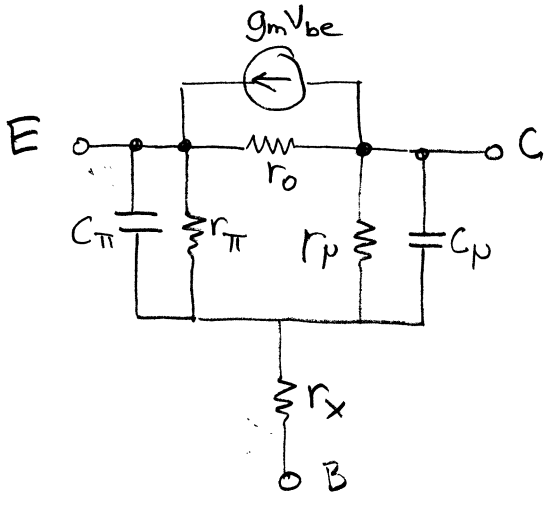
Correction to p. 123

(5) $C_{obo} \triangleq$ Common-base parallel output capacitance with input open-circuited

draw conventional hybrid-π CE equivalent circuit



now re-draw in CB form



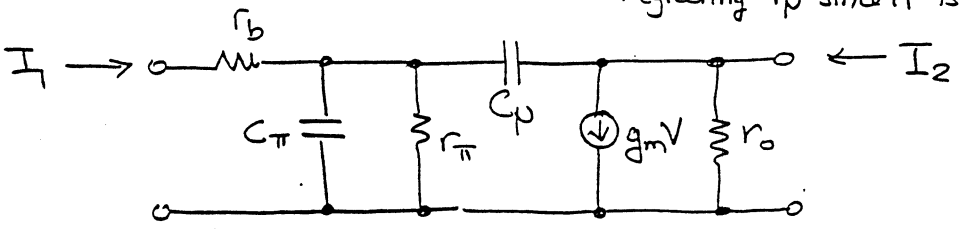
Typically r_x can be neglected

If r_o is large then $Z_o \approx r_\mu \| \frac{1}{j\omega C_\mu}$ and $C_o \approx C_\mu$

If r_o is small then $Z_o \approx r_\mu \| r_\pi \| \frac{1}{j\omega C_\mu} \| \frac{1}{j\omega C_\pi}$ and $C_o \approx \frac{C_\mu + C_\pi}{C_\mu * C_\pi}$

⑥ C_π is much harder to calculate.

neglecting r_μ since it is so large

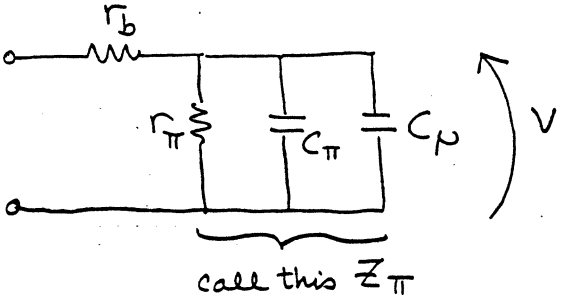


$$h_{fe} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \quad \text{by definition}$$

By inspection $I_2 = +I_c$ (the collector current)

$I_1 \approx +I_B$ (the base current)

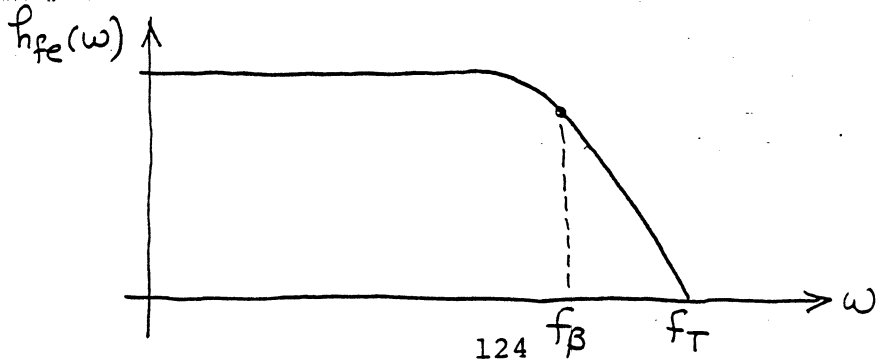
look at input with output shorted to calculate h_{fe}. The resultant circuit is:



$$Z_\pi = r_\pi \parallel \frac{1}{j\omega C_\mu} \parallel \frac{1}{j\omega C_\pi} = \frac{r_\pi}{1 + j\omega (C_\pi + C_\mu) r_\pi}$$

What is I_2? Since the values of feedback <u>impedance</u> are large $I_2 \approx g_m V = g_m Z_\pi I_1$

$$\therefore \quad h_{fe}(\omega) = \frac{g_m r_\pi}{1 + j\omega (C_\pi + C_\mu) r_\pi}$$



Plotting $h_{fe}(\omega)$ we observe a 3-db point at f_β, the β-cutoff frequency, and a high frequency asymptote f_T. These are related in a manner similar to the gainbandwidth product.

$$f_T = \beta_o f_\beta$$

In fact, one definition of r.f. frequencies is that $f_\beta < f < f_T$ so that one is always operating in the region where this relationship holds true. To prove the above expression

at a 3-db point $\omega(C_\pi + C_\mu) r_\pi = 1$ or

$$\omega_\beta (C_\pi + C_\mu) r_\pi = 1$$

$$2\pi f_\beta (C_\pi + C_\mu) r_\pi = 1$$

$$f_\beta = \frac{1}{2\pi (C_\pi + C_\mu) r_\pi}$$

at f_T $\quad |1| = \dfrac{g_m r_\pi}{1 + j 2\pi f_T (C_\pi + C_\mu) r_\pi} = \dfrac{\beta}{1 + j f_T / f_\beta}$

$$1 + j \frac{f_T}{f_\beta} = \beta$$

$$j \frac{f_T}{f_\beta} = \beta - 1$$

$$f_T \approx \beta f_\beta \quad \text{since } \beta \text{ is usually} >> 1$$

This also means that

$$f_T \cong \frac{g_m r_\pi}{2\pi (C_\pi + C_\mu) r_\pi} = \frac{g_m}{2\pi (C_\pi + C_\mu)}$$

Evaluating this expression for our given data

$I_c = 10mA,\ V_{CE} = 20V,\ f = 100\,MHz \qquad f_T = 250\,MHz$

(We must be careful since I_c and V_{CE} are not the same as before but we will neglect this for the minute)

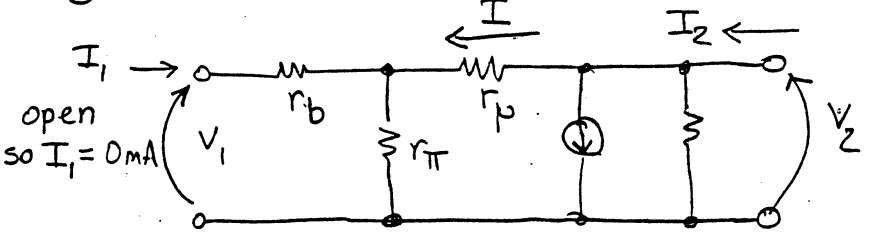
$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

$$250\times10^6 = \frac{4\times10^{-2}}{2\pi(C_\pi + 6pf)}$$

$$C_\pi + 6pf = \frac{4\times10^{-2}}{2\pi(250\times10^6)} = 2.55\times10^{-3}\times10^{-8} = 25.5pf$$

$$C_\pi = 25.5 - 6 = 19.5pf$$

(7) Since r_μ is in the feedback path from collector to base we may expect it to involve some relationship with h_r.



By definition $h_{re} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$

But $I = \frac{V_2 - V_1}{r_\mu}$ where it is assumed that $V_2 > V_1$.

V_1 can be found from the voltage drop across r_π since $I_1 = 0$

$$V_1 = I r_\pi = (V_2 - V_1)\frac{r_\pi}{r_\mu}$$ since no current thru r_b

$$h_{re} = \frac{V_1}{V_2} = \frac{(V_2 - V_1)}{V_2}\frac{r_\pi}{r_\mu} = \left(1 - \frac{V_1}{V_2}\right)\frac{r_\pi}{r_\mu}$$ but $\frac{V_1}{V_2} = h_{re}$

$$= (1 - h_{re})\frac{r_\pi}{r_\mu}.$$

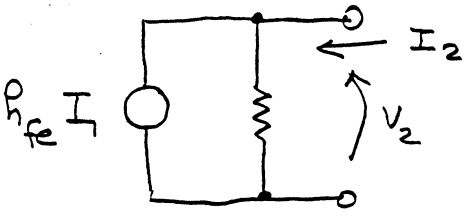
Solving for r_μ : $r_\mu = \frac{1-h_{re}}{h_{re}} r_\pi \approx \frac{r_\pi}{h_{re}}$ since usually $h_{re} \ll 1$.

For the 2N3250 $r_\mu \approx \frac{3.125K}{10\times10^{-4}} = 3.125\,M\Omega$

(8) find $h_o = \frac{1}{r_o}$

h_o is defined as $\left.\frac{i_2}{v_2}\right|_{i_1=0}$, i.e. the output admittance

when $i_1 = 0$ so the current source drops out. and the output circuit looks like:



$r_o = \frac{1}{h_o} = \frac{1}{22\times10^{-6}} = 45k\Omega$

---

neglect feedback for h_o calculation

All parameters must be specified for the same test conditions, i.e. I_c, V_{CE}. The variation of the basic small signal parameters is listed in the table below.

parameter	formula	I_c	V_{CE}	Temp.
g_m	$\frac{q}{kT}\lvert I_c\rvert$	linear	independent	$\frac{1}{T}$
g_π	$\frac{g_m}{\beta}$	linear	decreases	$\frac{1}{T^{1+}}$
C_π	$\frac{g_m}{2\pi f_T} - C_\mu$	$\approx$ linear	decreases	$T^{-0.3}$ to $T^{+0.7}$
C_μ		independent	decreases as $\lvert V_{CE}\rvert^{-\frac{1}{3}}$ or $\lvert V_{CE}\rvert^{-\frac{1}{2}}$ depending on junction type; use $\lvert V_{CE}\rvert^{-\frac{1}{2}}$ for abrupt junction	independe
β		$\approx$ independent	increases	increases
g_x	—— hard to explain ——			

Example of parameter variation: C_π was calculated to be 19.5 pf for 2N3250

f_T @ $I_c = 10mA$, $V_{CE} = 20Vdc$

need g_m at $I_c = 10mA$, C_μ at $I_c = 10mA$, $V_{CE} = 20V$.

$$g_m = \frac{|I_c|}{25mV} = \frac{10}{25} = 0.4\,\mho$$

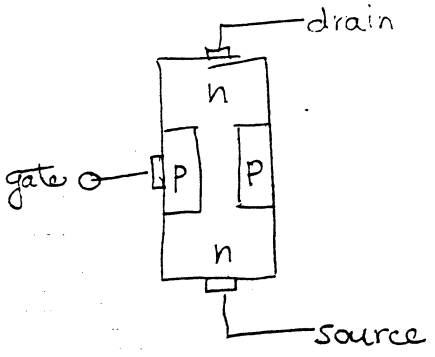
$$C_\mu \propto \frac{1}{\sqrt{V_{CE}}} \Rightarrow \frac{C_\mu}{C_{\mu'}} = \frac{\sqrt{V_{CE}'}}{\sqrt{V_{CE}}} \quad \text{or} \quad C_\mu = C_{\mu'}\sqrt{\frac{V_{CE}'}{V_{CE}}} = 6pf\sqrt{\frac{10}{20}} = 4.24pf$$

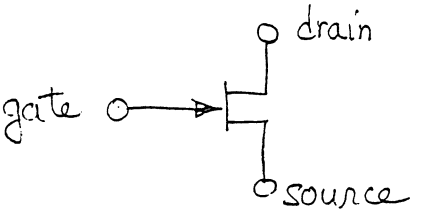
now compute $C_\pi = \frac{g_m}{2\pi f_T} - C_\mu$

$$= \frac{0.4}{2\pi(250\times10^6)} - 4.2pf = 255 - 4.2 = 250.8\,pf$$

this can be compared to our earlier value of 25pf.

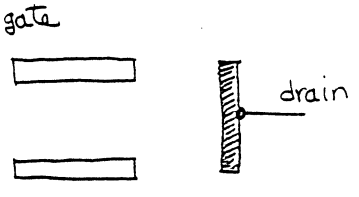
Field effect transistors — voltage amplifiers



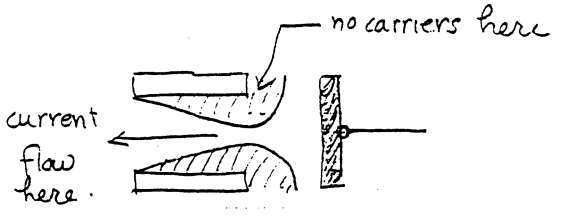


The drain current is at a maximum when $V_{GS}=0$
we call this maximum current I_{DSS}
specifically I_{DSS} is the drain current when the gate is short circuited to the source.

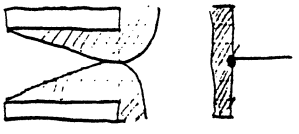
Without going into a lot of detail a FET operates like a voltage controlled resistor. Suppose $V_{GS}=0$. For small values of V_{DS} we have a typical resistor's linear i-v relationship. As V_{DS} increases the gate-drain junction becomes more reverse biased and a larger depletion region, i.e. an area with few mobile charges appears. As V_{DS} increases the depletion region increases increasing the resistance of the junction and lowering the slope (conductance) of the i-v curve.



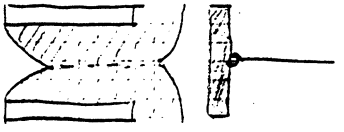
V_{DS} very small.



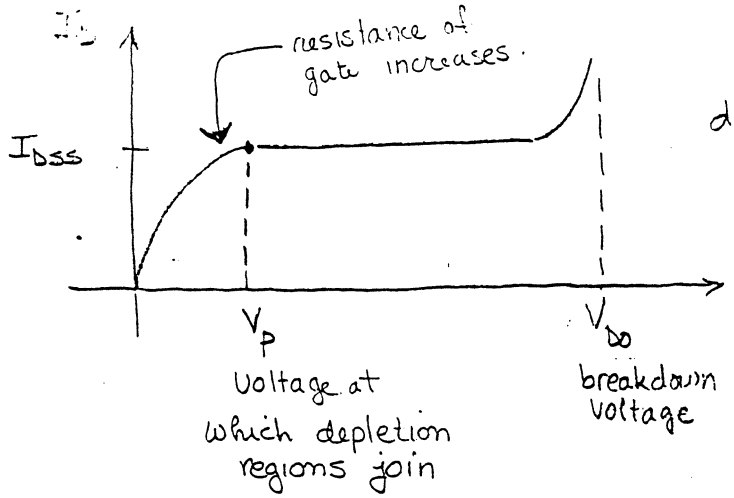
V_{DS} increasing



$V_{DS}=V_P$

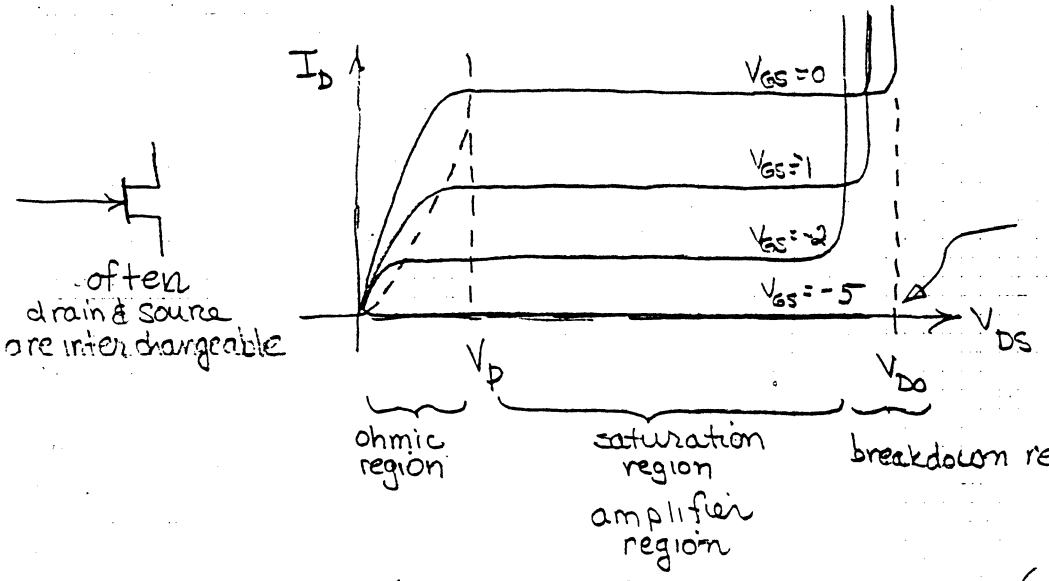


$V_{DS}>V_P$



drawen for $V_{GS} = 0$

As we vary V_{DS} we can generate a family of device curves



If $V_{GS} > 0$ junction is not reverse biased so transistor will not w

for a constant V_{DS} as V_{GS} becomes more negative it eventually cutsoff the FET.

at cutoff (or pinchoff) for a constant V_{DS} (V_p decreases as V_{GS} decreases

$$V_{DS}(\text{pinchoff}) \approx V_{po} + V_{GS} = V_P$$

V_{po}: pinchoff for zero V_{GS}

V_P: pinchoff voltage

The operation of the junction FET can be mathematically summarized as

1. ohmic region

$$I_D = I_{DSS}\left[2\left(1+\frac{V_{GS}}{V_{po}}\right)\frac{V_{DS}}{V_{po}} - \left(\frac{V_{DS}}{V_{po}}\right)^2\right]$$

for V_{DS} small $\quad I_D \approx \frac{2I_{DSS}}{V_{po}}\left(1+\frac{V_{GS}}{V_{po}}\right)V_{DS}$

looks like a resistor with

$$\frac{1}{r_{DS}} \approx \frac{2I_{DSS}}{V_{po}}\left(1+\frac{V_{GS}}{V_{po}}\right)$$

2. saturation region

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_{po}}\right)^2$$

note: $V_{GS} < 0$

$V_{po} > 0$

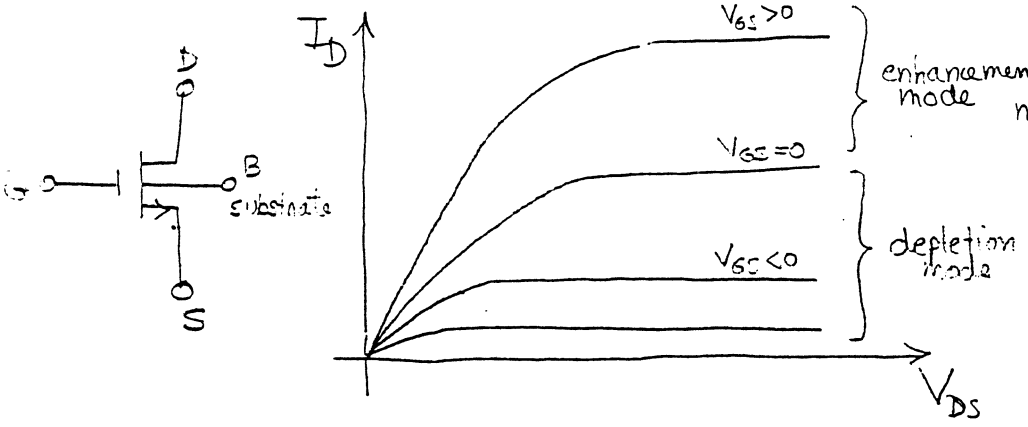
3. cutoff region $\quad I_D = 0$

A transistor manufacturer will often specify the transconductance g_{mo} defined by

$$g_{mo} = \frac{2\, I_{DSS}}{|V_{po}|}$$

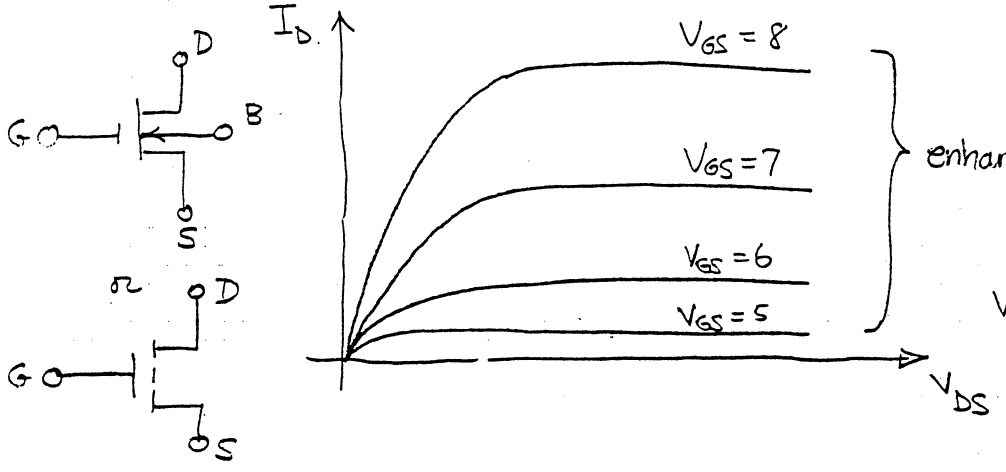
MOSFET

The MOSFET is a special version of the JFET in which a silicon dioxide layer electrically insulates the gate electrode from the rest of the transistor. Basically the MOSFET behaves identically to a JFET. As V_{GS} becomes more negative the minority carriers become depleted and the MOSFET behaves exactly like a JFET. However, because the gate is insulated from the rest of the transistor no p-n junction is formed at the gate and even if V_{GS} becomes positive no gate current can flow. If V_{GS} becomes positive negative charges are induced in the channel creating an "effective" larger majority carrier concentration. This increases the conductivity of the channel and increases I_D. When $V_{GS} > 0$ the MOSFET is operating in the enhancement mode.



n-channel depletion MOSFET

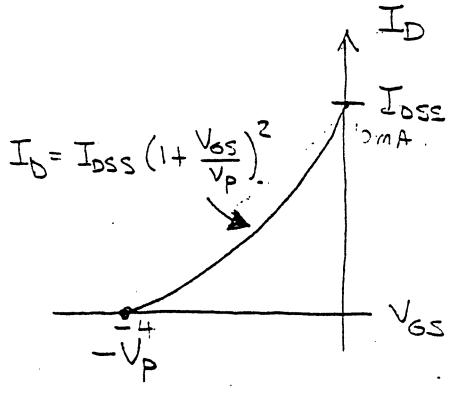
certain MOSFET's can only operate in the enhancement mode. This is because a channel is formed by the applied field (adding majority carriers) and does not exist when $V_{GS} \leq 0$.



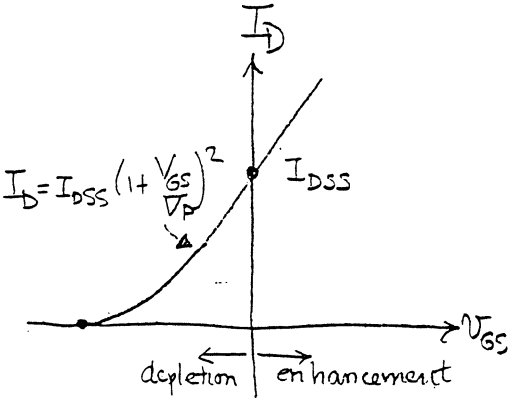
enhancement mode.

V_{GS} at which the channel form is called V_T, the thresho voltage.

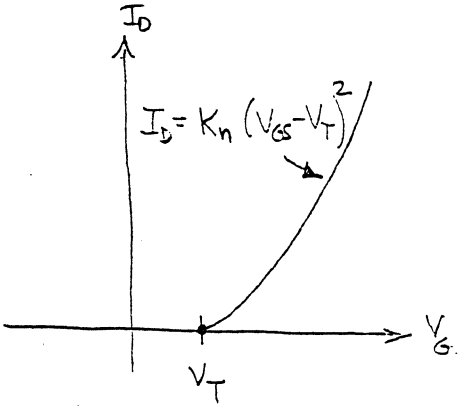
A very common way of displaying FET characteristics is the transfer characteristic curve which plots I_D as a function of V_{GS}, i.e. the output versus the input for a FET.



JFET



enhancement/ depletion MOSFET



enhancement MOSFET

V_T is the threshold voltage

all are n-channel.

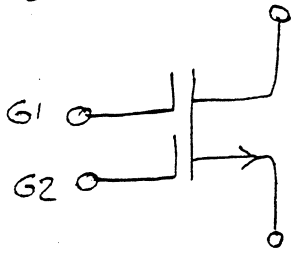
Why use FET's? Their transfer characteristics

A square-law relationship is good for mixers, amplifiers and gain-controlled stages.

$$g_m \triangleq \frac{\Delta I_D}{\Delta V_{GS}}$$ so this is the parameter that will be important.

g_{mo} is also the slope of the transfer characteristic.

Specialized MOSFET - dual gate

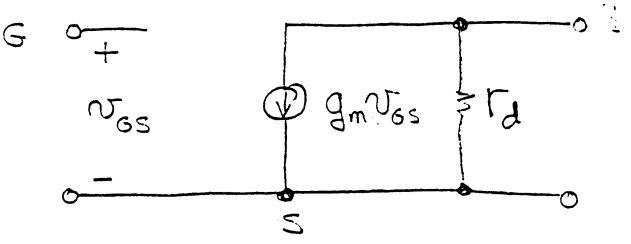


common substrate

very useful for mixers:

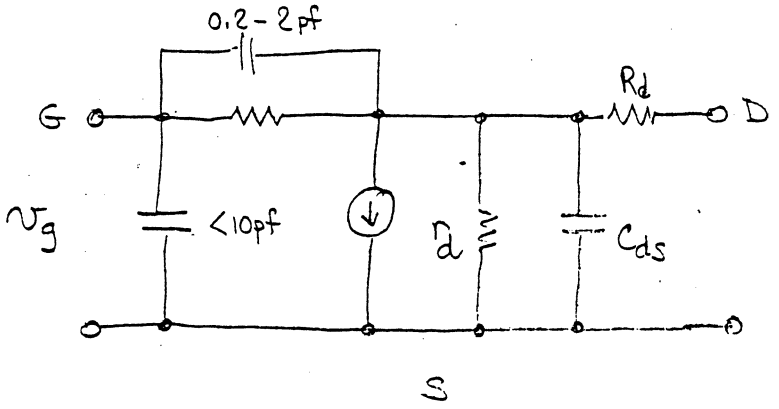
FET small signal model

circuits II (midband) model:

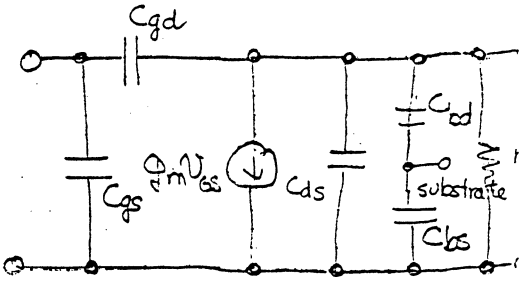


high frequency models:

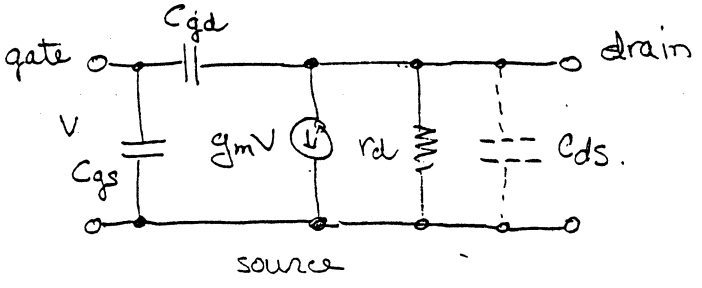
JFET



MOSFET



simplified high frequency π model



- C_{gd} feedback capacitance 0.05 – 5 pf
- C_{gs} input capacitance 0.1 – 10 pf
- r_d effective channel resistance 500 – 5000 Ω
- C_{ds} is usually small enough to be neglected.

In general, a FET is NOT better than a BJT at high frequencies

① The input impedance drops rapidly with frequency and quickly becomes reactive for a FET. (Even though the FET still has a somewhat higher impedance this can be made up for by a matching circuit for a BJT)

② A BJT usually has a better power gain.

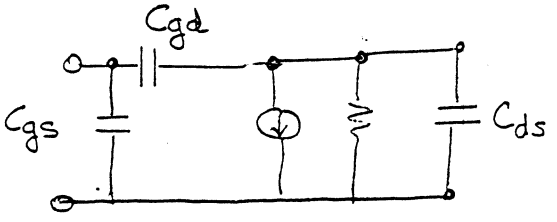
③ The BJT has a larger gain bandwidth product.

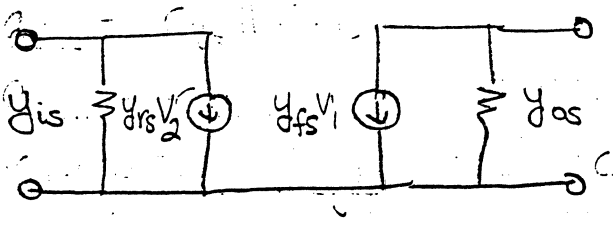
FET data sheets

transconductance $g_{mo} = \frac{2 I_{DSS}}{|V_p|}$

C_{iss}	common source	short-circuit input capacitance
C_{rss}		reverse transfer capacitance
C_{ds}		output capacitance

use π-model



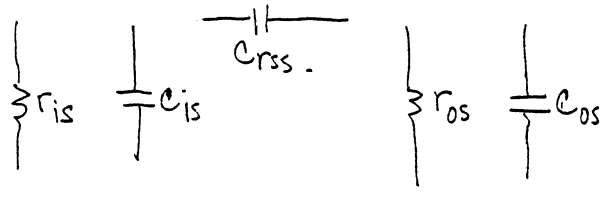


$C_{gd} \approx C_{rss}$ corresponds to C_p.

$C_{gs} \approx C_{iss} - C_{rss}$ input ‖ feedback

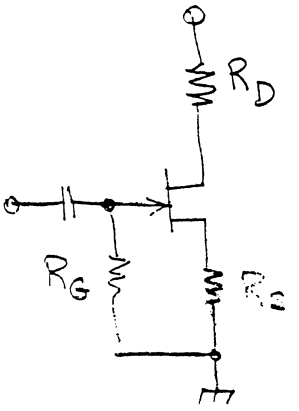
$C_{ds} \approx C_{oss} - C_{rss}$ output ‖ feedback.

i.e.



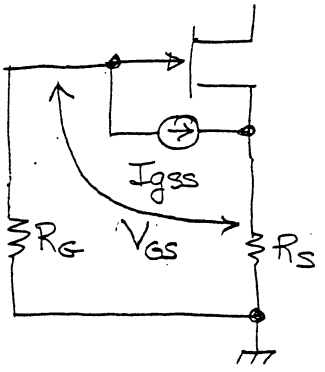
Biasing FET's (p. 98)

simple self-bias circuit



Why does this work?

Leakage current I_{gss} thru gate.



use KVL on gate bias circuit.

$$0 = I_{gss} R_G + V_{GS} + (I_{gss} + I_D) R_S$$

usually $I_{gss} \ll I_D$

$$V_{GS} = -\left(I_{gss} R_G + R_S I_D\right)$$

differentiate with respect to I_{gss}

$$\frac{\partial V_{GS}}{\partial I_{GSS}} = -R_G - R_S \frac{\partial I_D}{\partial I_{GSS}}$$

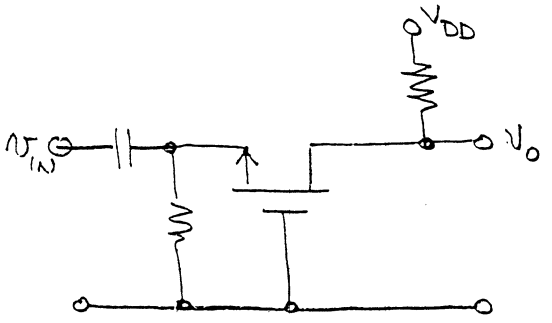
equivalent to stability criteria except for FET's.

$$\text{pick } R_G \leq -R_S \left.\frac{\partial I_D}{\partial I_{gss}}\right|_{max} + \left.\frac{\partial V_{GS}}{\partial I_{DSS}}\right|_{min}$$

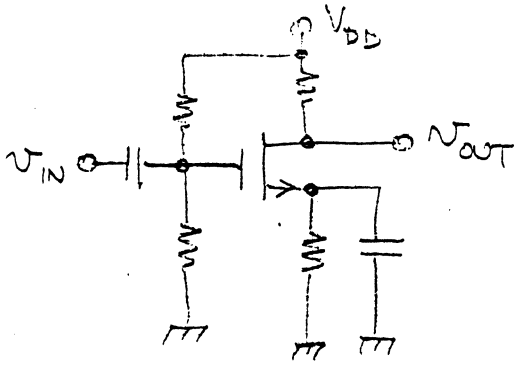
usually $R_G \sim 1 - 1.5 M\Omega$

FET amplifier topologies

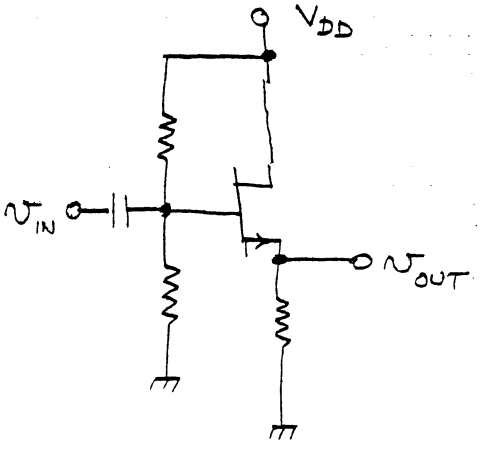
common gate



common source



common drain (source follower)

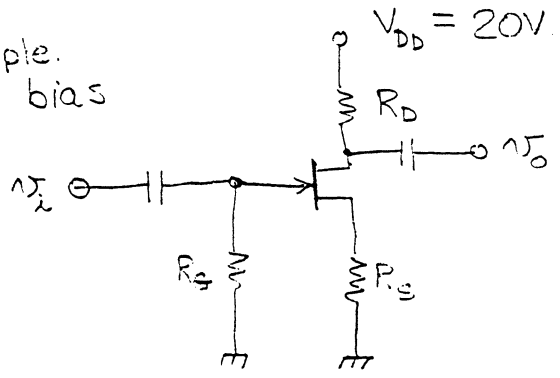


properties of a FET amplifier

	common gate	common source	common drain
R_{IN}	500Ω	∞	∞
R_{OUT}	∞	20kΩ	500Ω
A_v	4	-4	0.80

($g_m = 2 \times 10^{-3}$ Ω^{-1}, r_d = 20k, r_L = 2k)

Example.
JFET bias



For the JFET shown
$I_{DSS} = 8\,mA$
$V_P = -6V$

Bias at $I_D = 2.0\,mA$, $V_{DS} = 10V$

① Find V_{GS} from transfer characteristic

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

$$2 = 8\left(1 + \frac{V_{GS}}{+6}\right)^2$$

$$\frac{1}{4} = \left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\pm\frac{1}{2} = 1 + \frac{V_{GS}}{6}$$

$$\frac{1}{6}V_{GS} = -1 + \frac{1}{2}, -1 - \frac{1}{2} = -\frac{1}{2}, -\frac{3}{2}$$

$$V_{GS} = -3, -9$$

↖ beyond Pinchoff

$$\Rightarrow V_{GS} = -3 \text{ volts}$$

② Pick $R_G \approx 0.5\,M\Omega$

③ Use KVL at input

$$V_{GS} = -I_G R_G - I_D R_S \approx -I_D R_S$$

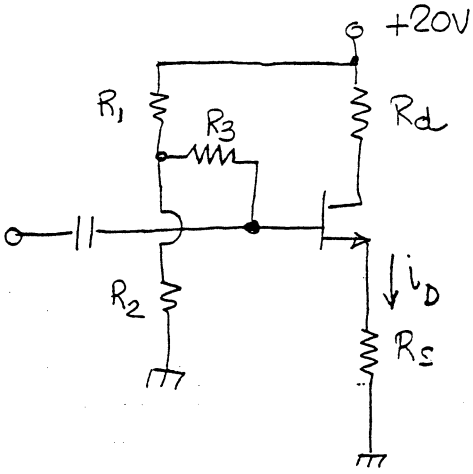
$$R_S \approx -\frac{V_{GS}}{I_D} = \frac{+3}{2\,mA} = 1.5K$$

④ use KVL at output

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

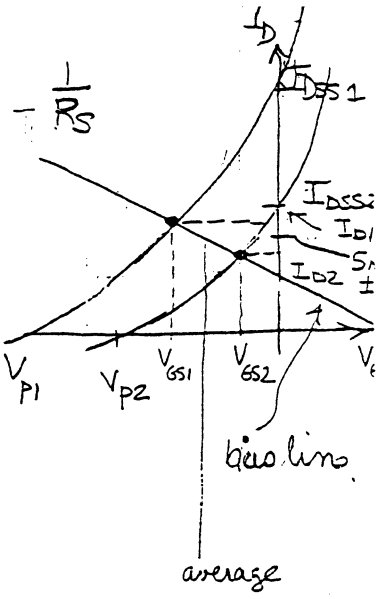
$$R_D = \frac{V_{DD} - V_{DS} - I_S R_S}{I_D} = \frac{20 - 10 - 1.5(2mA)}{2mA} = 3.5K$$

Example: depletion type MOSFET



$4 < V_p < 6$ volts

$8 < I_{DSS} < 10mA$



bias at $I_D = 5mA$, $V_{DS} = 8V$ with ±10% variation in I_D

① use transfer characteristic to get V_{GS}

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

$$\pm\left(1 + \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_P\left(\mp\sqrt{\frac{I_D}{I_{SSS}}} - 1\right)$$

V_{GS} will be a maximum when V_p is a maximum., I_D is a maximum

$$V_{GS} = 6\left(\mp\sqrt{\frac{5.5}{10}} - 1\right) = 6(\mp .74 - 1) = \begin{cases} -1.56 \\ -10.44 \leftarrow \text{belo} \\ \text{pinc} \end{cases}$$

use 10% variation in I_D.

V_{GS} will be a minimum when V_p is a minimum, I_D is a minimum

$$V_{GS} = 4\left(\mp\sqrt{\frac{4.5}{8}} - 1\right) = 4(\mp .75 - 1) = \begin{cases} -1.0 \\ -7.0 \leftarrow \text{belo} \\ \text{pinc} \end{cases}$$

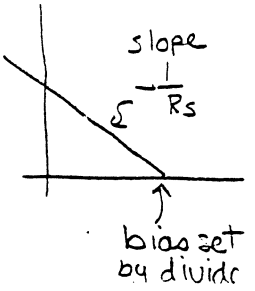
?? ~~+1.97 < V_{GS} < 7.68~~ volts due to parameter variation

② small signal analysis

$$V_{GS} = V_G - R_S I_D$$

$$\therefore I_D = \frac{V_G}{R_S} - \frac{1}{R_S} V_{GS}$$

↖ slope.



$$\therefore \quad R_S = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{-1.55+1.0}{5.5mA-4.5mA} = \frac{-0.55}{1mA} = 550\Omega$$

③ find V_G

$$V_G = V_{GS} + I_D R_S$$

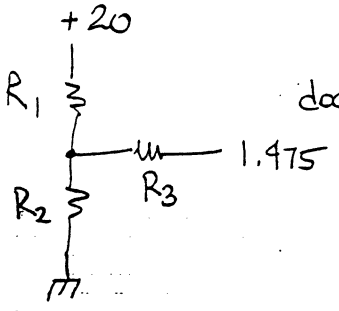
use average $V_{GS} = \frac{-1.55-1.0}{2} = -1.275$

$$V_G = -1.275 + (5\times10^{-3})(550) = +1.475$$

nominal value

④ pick simple voltage divider

pick $R_3 = 500K$ for leakage current



doesn't really matter

pick $R_1 = 100K$

$$\frac{R_2}{R_1+R_2}\,20 = 1.475$$

$$20R_2 = 1.475R_1 + 1.475R_2$$

$$R_2 = \frac{1.475R_1}{18.525} = .0796\,(100K)$$

$$= 7.9K$$

⑤ use KVL at output

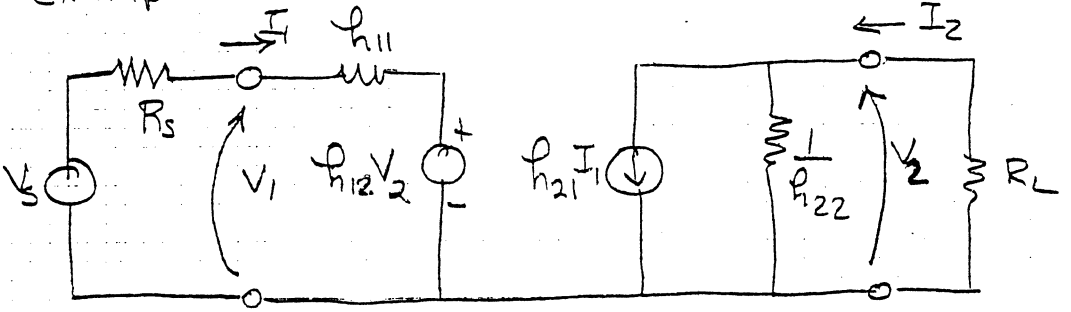
$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$20 = (5)R_D + 8V + (5)(550)$$

$$R_D = \frac{20-8}{5mA} - 550\Omega = 1850\Omega.$$

Because amplifier topologies are identical for the h-parameter model we can determine a single formula for all external parameters such as input impedance, voltage gain, etc.

Example:



the "general" h-parameters $h_{11}, h_{12}, h_{21}, h_{22}$ are used here.

Let us find R_i, the input impedance of the above h-parameter model. By definition

$$R_i = \frac{V_1}{I_1} = \frac{\overbrace{I_1 h_{11} + h_{12} V_2}^{\text{input loop.}}}{I_1}$$

Write V_2 in terms of I_1 to eliminate all variables from expression for R_i. To find V_2 use output node.

$$-I_2 = \frac{V_2}{R_L}$$

note sign convention due to direction of I_2

$$I_2 = h_{21} I_1 + V_2 h_{22}$$

output node.

Combining these expressions

$$-\frac{V_2}{R_L} = h_{21} I_1 + V_2 h_{22}$$

and solving for V_2

$$V_2 \left(-\frac{1}{R_L} - h_{22}\right) = h_{21} I_1$$

Substituting into our original expression for R_i

$$R_i = \frac{I_1 h_{11} + h_{12}\left(\frac{h_{21}}{-\frac{1}{R_L} - h_{22}}\right) I_1}{I_1}$$

$$R_i = h_{11} - \frac{h_{12} h_{21}}{\frac{1}{R_L} + h_{22}}$$

Note that if $R_L \to 0$ the second term goes away and $R_i \to h_{11}$ as we would expect. Putting the above expression into a more standard form

$$R_i = \frac{h_{11}\frac{1}{R_L} + \overbrace{h_{11}h_{22} - h_{12}h_{21}}^{\Delta h}}{\frac{1}{R_L} + h_{22}}$$

$$R_i = \frac{h_{11} + \Delta h R_L}{1 + h_{22} R_L}$$

We can also find the small signal voltage gain the same way. By definition

$$A_V = \frac{V_2}{V_1} = \frac{V_2}{I_1 h_{11} + h_{12} V_2}$$

Here we want to write I_1 in terms of V_2 which we already know from our previous calculation

$$A_V = \frac{V_2}{V_2\left(\frac{-\frac{1}{R_L} - h_{22}}{h_{21}}\right) h_{11} + h_{12} V_2}$$

$$A_v = \frac{h_{21}}{\left(-\frac{1}{R_L} - h_{22}\right) h_{11} + h_{12} h_{21}}$$

$$A_v = \frac{h_{21}}{-\frac{h_{11}}{R_L} - \underbrace{h_{22} h_{11} + h_{12} h_{21}}_{-\Delta h}} = \frac{h_{21}}{-\frac{h_{11}}{R_L} - \Delta h}$$

$$A_v = -\frac{h_{21} R_L}{h_{11} + \Delta h R_L}$$

To check this result Note that as $R_L \to \infty$ $A_v \to -\frac{h_{21}}{\Delta h}$

as $R_L \to 0$ $A_v \to 0$

Both answers are to be expected. If $R_L = \infty$ the gain is determined by the transistor internal parameters; If $R_L = 0$ there can be no output voltage and, consequently, no voltage gain.

Tabulated values of R_i, R_o, A_v, A_i and A_p for the three different amplifier topologies are given on the following page.

h-PARAMETER AMPLIFIER:

AMPLIFIER MATRIX REPRESENTATIONS

AMPLIFIER CHARACTERISTICS AND PARAMETER CONVERSIONS

MATRIX	COMMON BASE	COMMON EMITTER	COMMON COLLECTOR
h_{11}	h_{ib}	$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$	$h_{ic} = \frac{h_{ib}}{1+h_{fb}}$
h_{12}	h_{rb}	$h_{re} = \frac{(\Delta_h)_b - h_{rb}}{1+h_{fb}}$	$h_{rc} = 1$
h_{21}	h_{fb}	$h_{fe} = -\frac{h_{fb}}{1+h_{fb}}$	$h_{fc} = -\frac{1}{1+h_{fb}}$
h_{22}	h_{ob}	$h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{oc} = \frac{h_{ob}}{1+h_{fb}}$

AMPLIFIER EXTERNAL CHARACTERISTICS[1]:

$$R_{INPUT} = \frac{h_{11}+R_L\Delta_h}{1+h_{22}R_L} \qquad R_{OUTPUT} = \frac{R_S+h_{11}}{\Delta_h+h_{22}R_S}$$

$$A_{CURRENT} = \frac{h_{21}}{1+h_{22}R_L} \qquad A_{VOLTAGE} = \frac{h_{21}R_L}{h_{11}+\Delta_h R_L}$$

$$A_{POWER} = \frac{h_{21}^2 R_L}{(h_{11}+\Delta_h R_L)(1+h_{22}R_L)}$$

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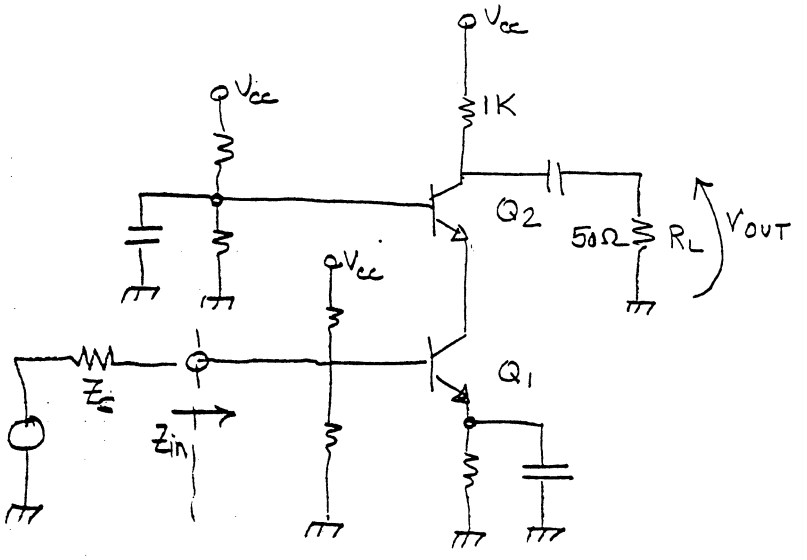
[1]NOTE: These formulae are valid for ALL two-port matrix parameters. For example, you can substitute y_{11} for h_{11}, etc. as long as you do it throughout the formula.

EXTERNAL AMPLIFIER CHARACTERISTICS

	Common emitter	Common base	Common collector
R_{INPUT}	medium 200–2000Ω	low 30–800Ω	high 10^3–10^5Ω
R_{OUTPUT}	medium 10^3–10^5Ω	high 10^5–10^6Ω	low 10^2–10^4Ω
$A_{VOLTAGE}$	high variable	high variable	low 1
$A_{CURRENT}$	high 20–200	low 1	high 20–200
A_{POWER}	high 1000–10,000	low 20–50	medium 20–200

Cascode amplifier



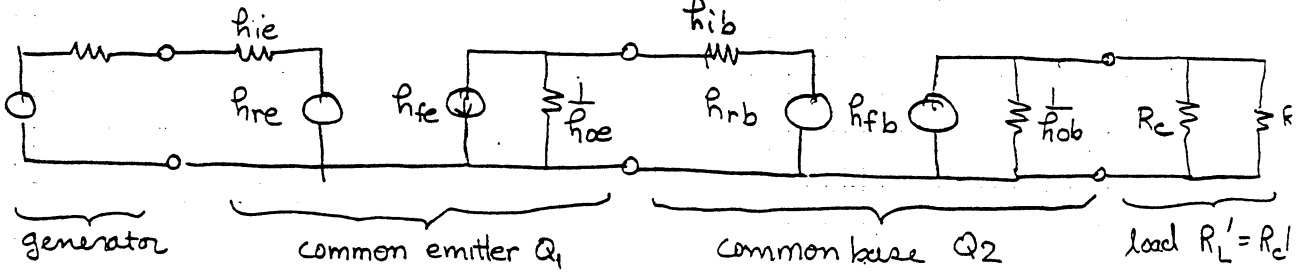
$R_L' = 50\Omega \,||\, 1K$
$= 47.6\,\Omega.$

biasing of this amplifier is discussed in B-N p. 334 – 336

We can simply determine Z_{in}, Z_{out}, A_p, etc. using matrix parameters

Q_1 is a common emitter amplifier
Q_2 is a common base amplifier

Basically, Q1 and Q2 are in series so overall small signal circuit look like this



From data sheet

$h_{ie} = 1.25K$
$h_{re} = 4\times10^{-4}$
$h_{fe} = 375$
$h_{oe} = 200\times10^{-6}$

calculating $\Delta h_e = h_{ie}h_{oe} - h_{fe}h_{re} = (1250)(200\times10^{-6}) - (375)(4\times10^{-4}) \approx 0.1$

to get CB parameters we must use conversion formula

$$h_{fb} = -\frac{h_{fe}}{1+h_{fe}} = -\frac{375}{1+375} = -.997$$

$$h_{oe} = h_{ob}(h_{fe}+1) \text{ or } h_{ob} = \frac{h_{oe}}{h_{fe}+1} = \frac{200\times10^{-6}}{375+1} = 0.53\times10^{-6}$$

$$h_{ib} = \frac{h_{ie}}{h_{fe}+1} = \frac{1250}{375+1} \cong 3.32\,\Omega$$

$$h_{rb} = h_{ib}h_{ob}(h_{fe}+1) - h_{re}$$
$$= (3.32)(.53\times10^{-6})(375+1) - 4\times10^{-4}$$
$$= 6.65\times10^{-4} - 4\times10^{-4} \approx 2.65\times10^{-4}$$

$$\Delta h_b = h_{ib}h_{ob} - h_{fb}h_{rb} = (3.32)(.53\times10^{-6}) - (2.65\times10^{-4})(.997)$$
$$= 1.766\times10^{-6} - 2.64\times10^{-4} \approx -2.64\times10^{-4}$$

we can now quickly calculate the effective R_{IN} and voltage gain of Q_2.

$$R_{IN} = \frac{h_{11} + R_L\Delta h}{1 + h_{22}R_L} = \frac{h_{ib} + R_L'\Delta h_b}{1 + h_{ob}R_L'}$$

$$= \frac{3.32 + (47.6)(2.64\times10^{-4})}{1 + (.532\times10^{-6})(47.6)} \approx 3.32$$

$$A_V = \frac{h_{21}R_L}{h_{11} + R_L\Delta h} = \frac{h_{fb}R_L'}{h_{ib} + R_L'\Delta h_b} = \frac{(.997)(47.6)}{3.32 + \underbrace{(47.6)(-2.64\times10^{-4})}_{-.0125}}$$

$$\cong 14.34$$

R_{IN} is actually R_L for Q_1 so we can now calculate Z_{in} for the amplifier

$$Z_{in} = \frac{h_{ie} + R_{IN}\Delta h_e}{1 + h_{oe}R_{IN}} = \frac{1.25K + (3.32)(0.1)}{1 + (200\times10^{-6})(3.32)} \approx 1.25K$$

$$A_{V,Q_1} = \frac{h_{fe}R_{IN}}{h_{ie} + \Delta h_e R_{IN}} = \frac{(375)(3.32)}{1250 + (0.1)(3.32)} \approx 0.996 \quad \text{close to 1.}$$

overall $A_V = A_{V,Q_1}A_{V,Q_2} = (0.996)(14.34) = 13.2$

since no voltage divider between Q_1 and Q_2