3.5. Sketch i against v to scale for the circuits shown in Figure P3.5. The diodes are typical small-signal silicon devices at 300 K. The reverse-breakdown voltages of the Zener diodes are shown. Assume 0.6 V for all diodes (including Zeners) in the forward-bias region.

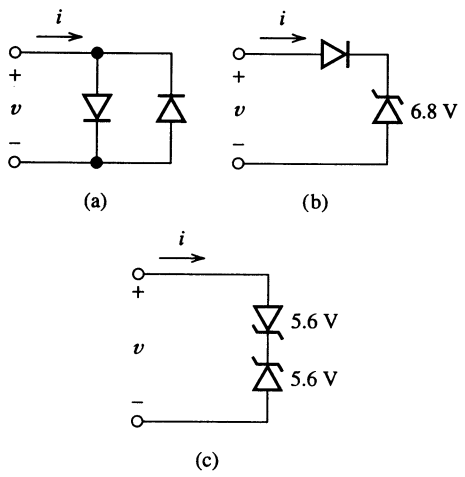
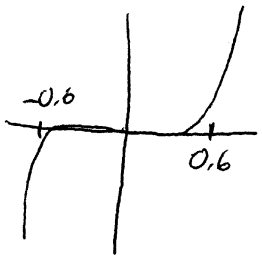


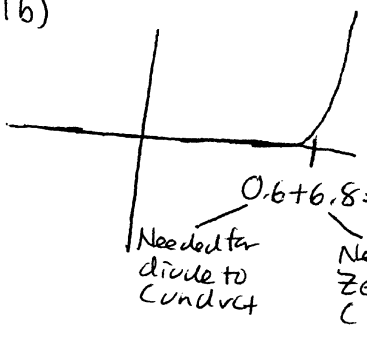
Figure P3.5

3.5 Note, These are not ideal, but typical diodes. Thus, They have ~0.6 V drop when conducting, and slight curve

(a)

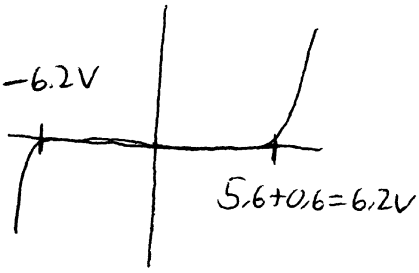


(b)



Note: The Zener will conduct at -0.6V and lower, but the other diode won't until it breaks

(c)



In both directions, we need 0.6 volts to turn on the forward diode, and 5.6 more to push the reverse diode into breakdown

3.35. Consider the circuit shown in Figure P3.35. Allow 0.6 V for the forward drops of the diodes. Sketch the transfer characteristic to scale. (Combining the bridge rectifier with a Zener diode is a neat way to obtain nearly identical characteristics for both polarities of the input voltage.)

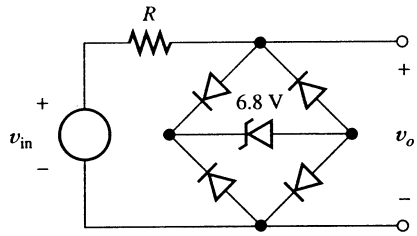
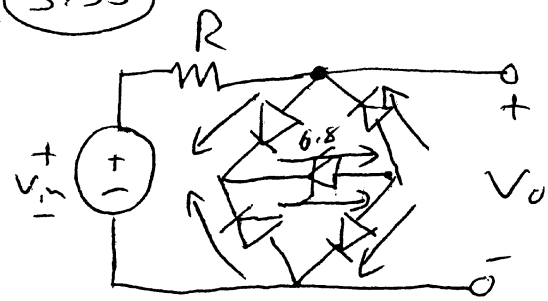


Figure P3.35

3.35

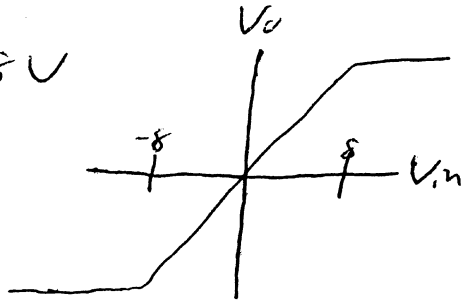


If the bridge is off, $V_o = V_{in}$. Once the bridge turns on, V_o will be held at that voltage. Higher voltages will cause more current over R & the output will be held at the initial "on" voltage.

In either direction, to turn the bridge on, we must fwd bias 2 diodes, and reverse-bias the zener into breakdown.

Thus, On voltage = $0.6 + 6.8 + 0.6 = \pm 8\,V$

Current paths are labeled above.



3.32. Voltage-doubler circuit. Consider the circuit of Figure P3.32. The capacitors are very large, so that they discharge only a very small amount per cycle. (Thus, no ac voltage appears across the capacitors, and the ac input plus the dc voltage of C_1 must appear at point A.) Sketch the voltage at point A against time. Find the voltage across the load. Why is this circuit called a voltage doubler? Determine the peak inverse voltage across each diode in terms of V_m.

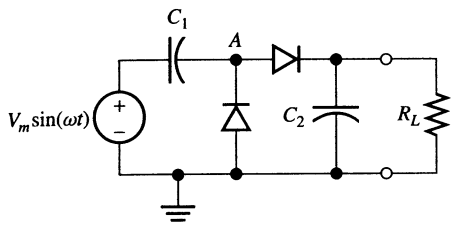
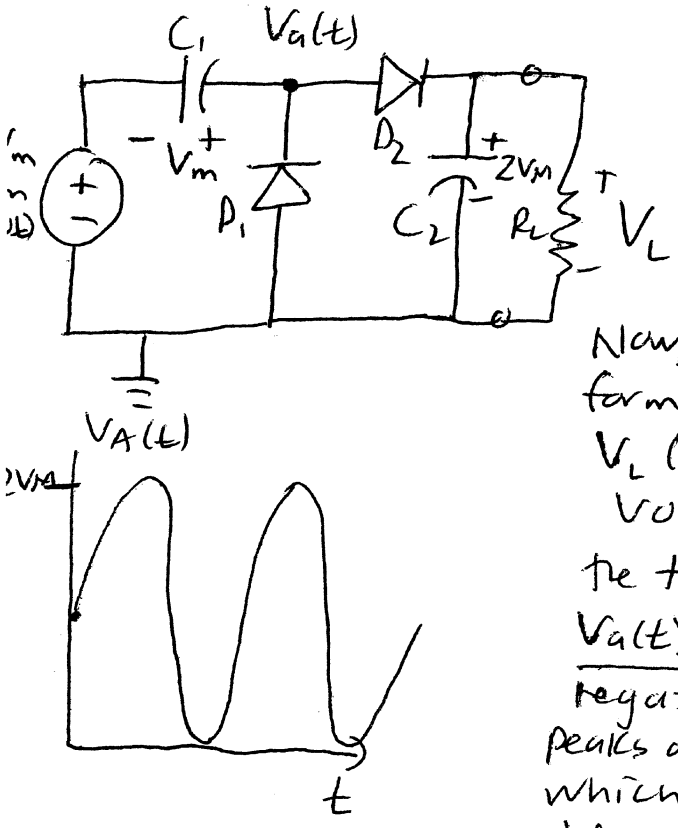


Figure P3.32

3.32



First, notice that D_1 & C_1 form a "clamp" circuit; i.e. when $V_m \sin(\omega t) < 0$, D_1 conducts charging C_1. Thus, negative peaks are clamped to 0V. Now, notice that D_2 & C_2 & R_L form a half-wave rectifier; thus, V_L (V_{C_2}) will charge to the peak voltage seen at $V_a(t)$. Combining the two, $V_a(t)$ will be:

$V_a(t) = V_m + V_m \sin(\omega t)$ to clamp negative peaks at 0V. Positive peaks of $V_a(t)$ will thus be at $2V_M$, which is what V_L will be.

$V_O = V_L = V_{C_2} = 2V_M$

Peak inverse $D_2 = 2V_m$ Peak inverse $D_1 = 2V_M$

3.22. Figure P3.22 shows an ac voltmeter. Assume that the diode is ideal. Suppose that the meter reads full scale when the average current is 5 mA. Assume that the resistance of the meter is negligible. For what value of R will full scale correspond to an ac voltage of 10 V rms? (*Hint:* The average value of a half-wave rectified sine wave is the peak value divided by π.)

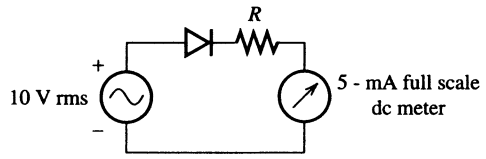


Figure P3.22

3.22 The current thrayh the meter is a half-wave rectified sinusoid. Since voltage is $10 V_{RMS}$, $V_{p-p} = 10\sqrt{2}$. Thus, current will be $\frac{10\sqrt{2}}{R}$. As given in the problem, the $Avg = \frac{V_{pp}}{\pi}$.

Avg current $= \frac{10\sqrt{2}}{\pi R} = 5mA$ $\boxed{R = 900\Omega}$

3.24. Consider the battery-charging circuit of Figure P3.24 with $V_m = 20$ V, $R = 10\,\Omega$, and $V_B = 14$ V. Find the peak current, assuming an ideal diode. Also, find the percentage of each cycle for which the diode is in the on state. Sketch $v_s(t)$ and $i(t)$ to scale against time.

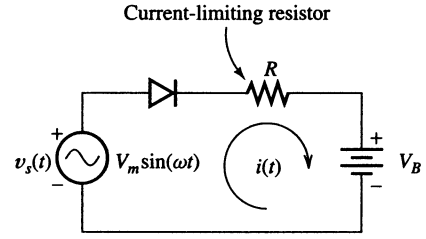
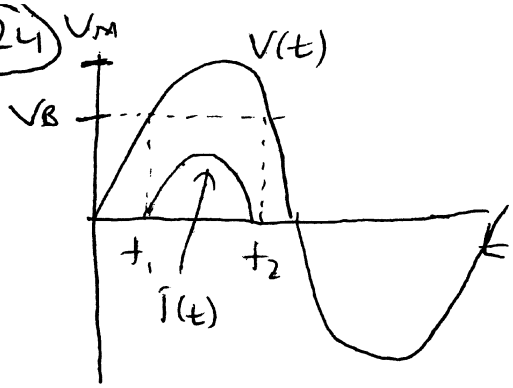


Figure P3.24 Half-wave battery charger.

3.24



$i(t)$ is non-zero only when $V(t) > V_B$
$i(t)$ will peak when $V_s(t)$ peaks at V_m. Thus, $i_{max} = \frac{V_M - V_B}{R}$ $\boxed{i_{max} = 0.6\,A}$

As a function of time, $i(t) = \frac{V_m \sin(\omega t) - V_B}{R}$ Setting $i(t) = 0$,

$\sin(\omega t) = \frac{V_B}{V_M}$. We have two solutions: $t_1 = \frac{.775}{\omega}$ $t_2 = \frac{2.37}{\omega}$.

These are marked on the graph. Sine wave period is $T = 2\pi/\omega$.

diode on $= \frac{2.37/\omega - .775/\omega}{2\pi/\omega} = \boxed{25.3\%}$

3.20. Sketch the transfer functions (v_o versus v_{in}) for the circuits displayed in Figure P3.20. Also, plot v_o to scale against time for $v_{in}(t) = 10\sin(200\pi t)$. Assume ideal diodes.

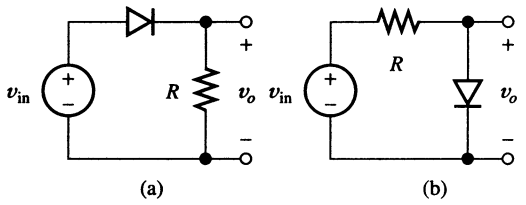
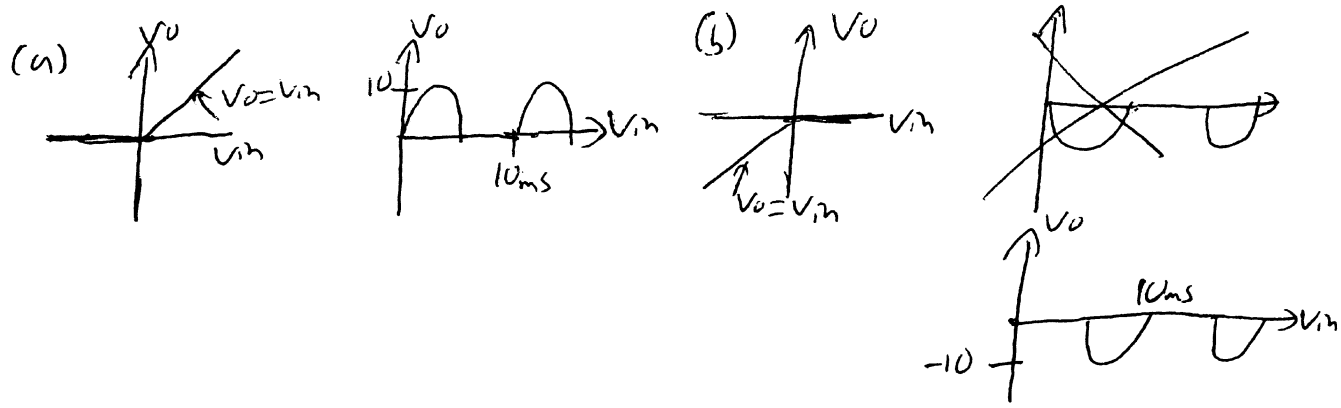
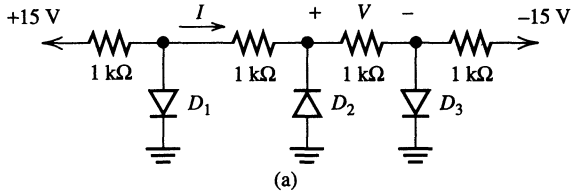


Figure P3.20

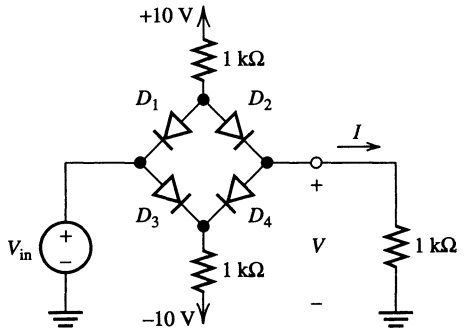
(3.20) ideal diode → short when on. In both circuits, diodes conduct for $V_{in} > 0$. In (A) this causes V_{in} to pass to R. In (B) it shorts V_o. For $V_{in} < 0$, in (a) voltage cannot get to V_o. In (b), all V_{in} will be across V_o since it is an open circuit



3.17. Assuming that the diodes are ideal, find the values of I and V for the circuits of Figure P3.17. For part (b), consider $V_{in} = 0$, 2, 6, and 10 V. Then plot V against V_{in} for $-10 \le V_{in} \le 10$.



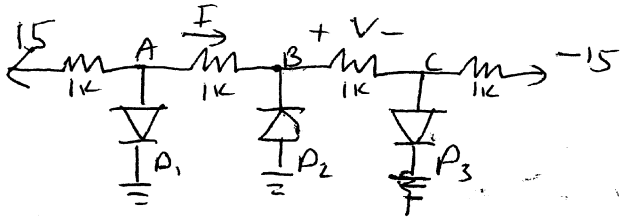
(a)



(b)

Figure P3.17

(3.17) Start analysis by assuming all diodes off, then turn on and re adjust

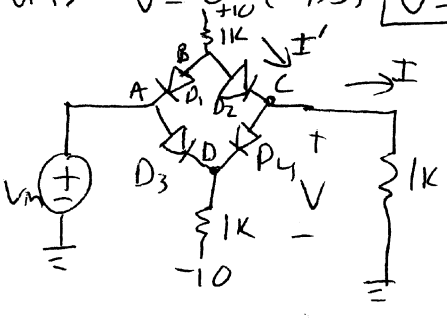


D_1 sees +15 forward bias, it turns on. $V_A = 0$

D_3 sees −15 reverse bias, stays off.

D_2 sees +15 (0−(−15)) fwd bias turns on. $V_B = 0$.

$V_A = V_B = 0 \therefore \boxed{I = 0}$ $V_C = -7.5$ V (voltage divider) D_3 is still off. $V = 0 - (-7.5)$ $\boxed{V = 7.5 \text{ V}}$



$V_{in} = 0 \rightarrow$ All diodes on. $V_A = V_B = V_C = V_D = 0$. $\boxed{V = 0, I = 0}$ $I' = 10$mA, but all goes through D_4 to −10.

$V_{in} = 2 \rightarrow$ All diodes on. $V_A = V_B = V_C = V_D = 2$. $V = 2$, $I = 2$mA $I' = 8$mA, excess goes thru D_4, circuit still works. $\boxed{V = 2, I = 2\text{mA}}$

$V_{in} = 6 \rightarrow$ All diodes on. $V_A = V_B = V_C = V_D = 6$. $V = 6$, $I = 6$mA. However, $I' = 4$mA. Extra current must come through D_1 or D_{4} but can't travel backwards through diode. Therefore, $I \le I'$

$I = I'$ at 5mA. $V_B = V_C = 5$. However, this turns D_1 & D_4 off. So, for input voltages greater than 5, output remains at $\boxed{V = 5, I = 5\text{mA}}$ and the excess current from the input is shunted to −10.

$V_{in} = 10$ See above $\boxed{V = 5, I = 5\text{mA}}$

3.15. Assuming that the diodes are ideal, find the values of I and V for the circuits of Figure P3.15.

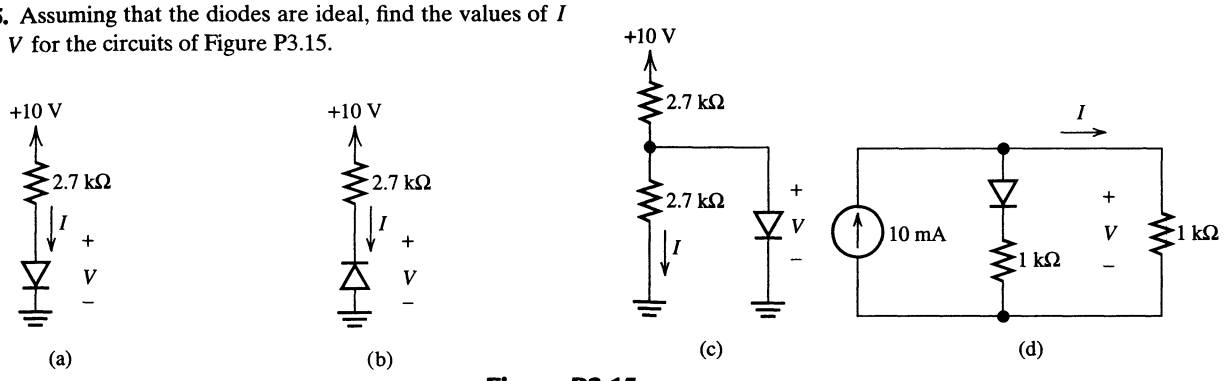
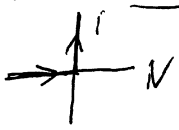


Figure P3.15

(3.15) Note that these are ideal diodes; they have the following transfer:  Thus, when on, Vd=0, not 0.6

A good way to analyze is to assume the diodes are off, then turn them on when forward biased and re-analyze circuit until everything fits.

(a) +10V at the anode, 0 at the cathode → diode will turn on. Thus, $\boxed{V=0}$ and $\boxed{I=\frac{10V}{2.7k\Omega}=3.7mA}$

(b) 0 at the anode, 10V at the cathode → diode remains off. $\boxed{V=10,\ I=0}$ (diode acts like open circuit)

(c) 5V at anode, 0 at cathode → diode turns on. Since $R_{on}=0$ for diode, all current will flow through it. Thus, $\boxed{I=0,\ V=0}$ (diode acts like a wire)

(d) Initially, diode is off. All current flows through R_2, causing V to rise to $(10mA)(1k)=10V$. Diode R_2 turns on, and we have a current divider.

$\boxed{I=5mA,\ V=5V}$

3.9.

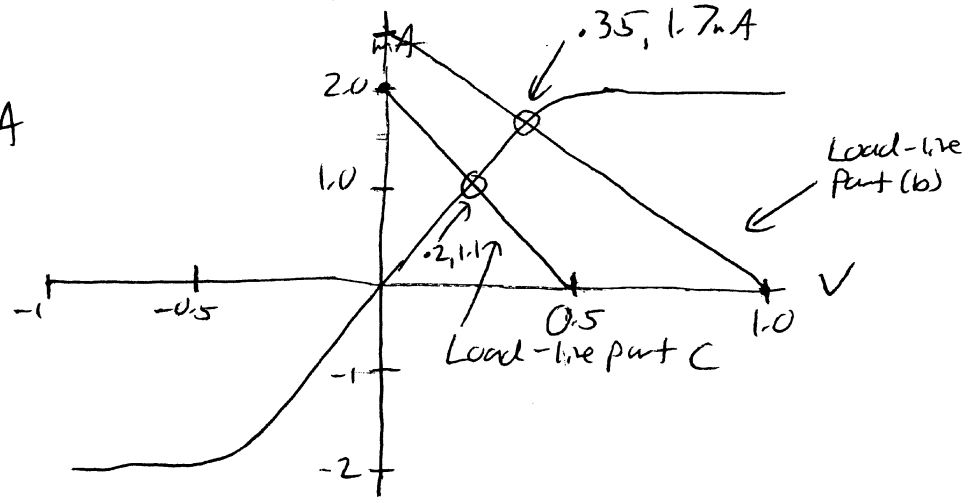
$V_{OC} = 1V$

$I_{SC} = \frac{1V}{400\Omega} = 2.5mA$

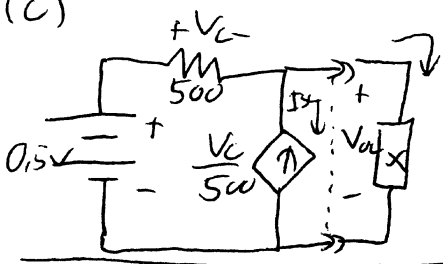
$I_b = i_x = \boxed{1.7mA}$

$V_b = V_x + 200 i_x$

$\boxed{V_b \approx 0.69V}$



(c)



$V_{OC} = 0.5V$

$I_{SC} = \frac{V_C}{500} + \frac{V_C}{500} = \frac{V_C}{250}$

When shorted, $V_C = 0.5V \therefore I_{SC} = 2mA$

$\boxed{I_C = i_x \approx 1.1mA \quad V_C = 0.5 - V_x \approx 0.3V}$

3.9. Use graphical load-line analysis to find the currents and voltages labeled in the circuits shown in Figure P3.9. The device characteristics are illustrated in Figures P3.9d and e.

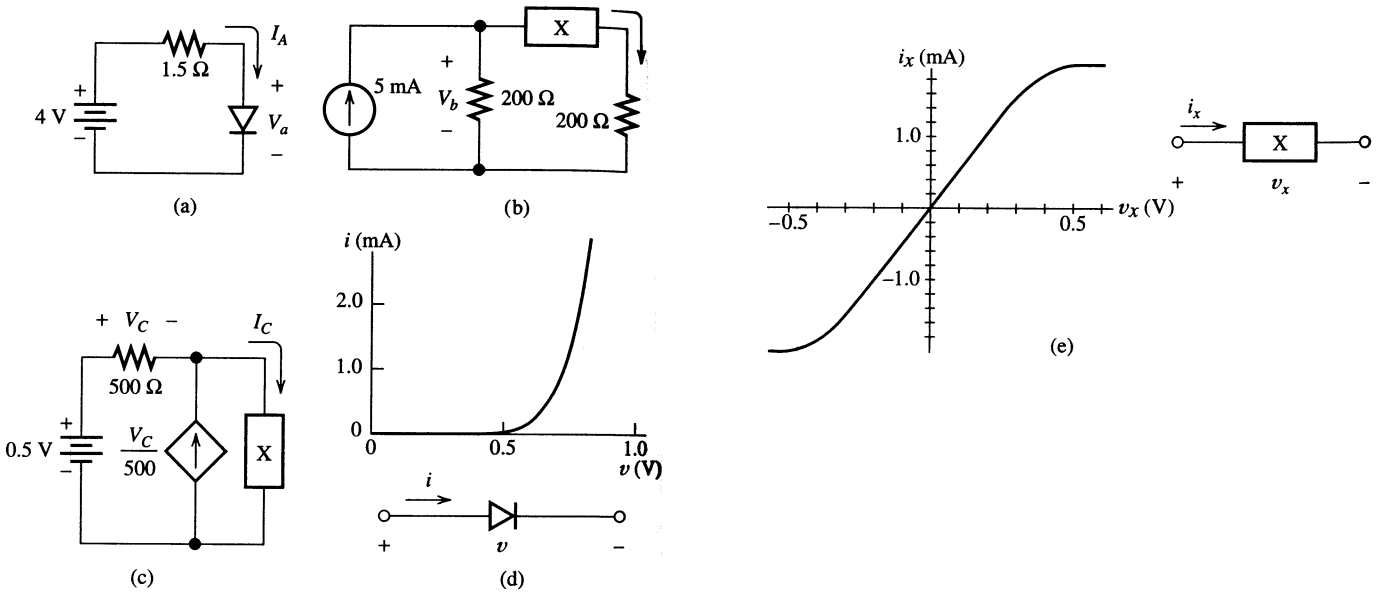
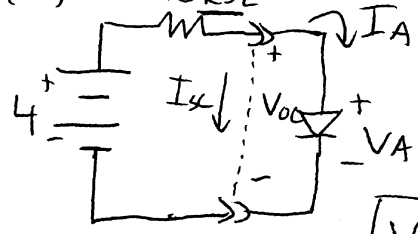


Figure P3.9

(3.9) The key to load-line is to find the open-circuit voltage and short-circuit current, plot them, draw a line, and then find the operating point. BE CAREFUL in drawing your graphs; if the scale is off, your answer will be too.

(a) 1.5kΩ ← book mistake

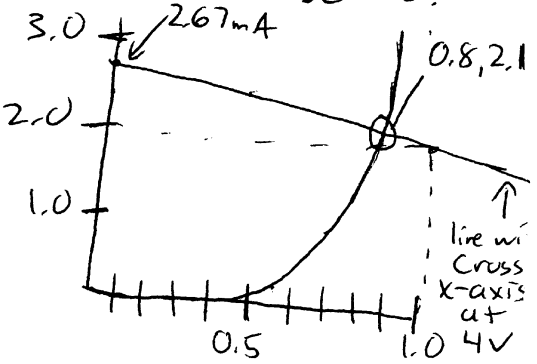


$V_{OC} = 4V$

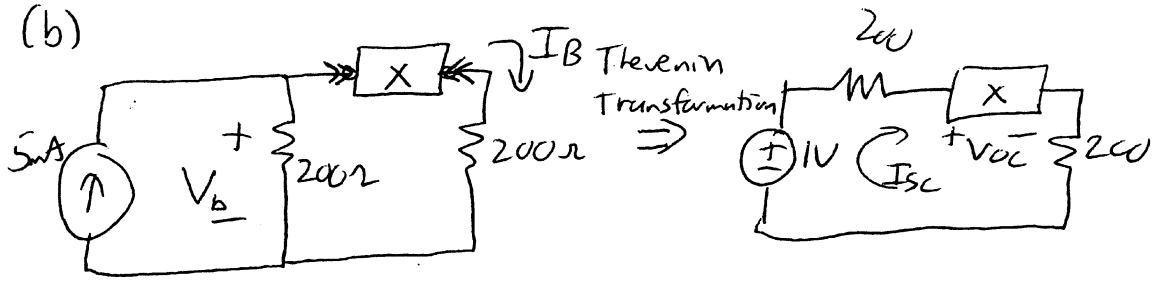
$I_{SC} = \frac{4}{1.5k\Omega} = 2.67mA$

$V_A \approx 0.8V$

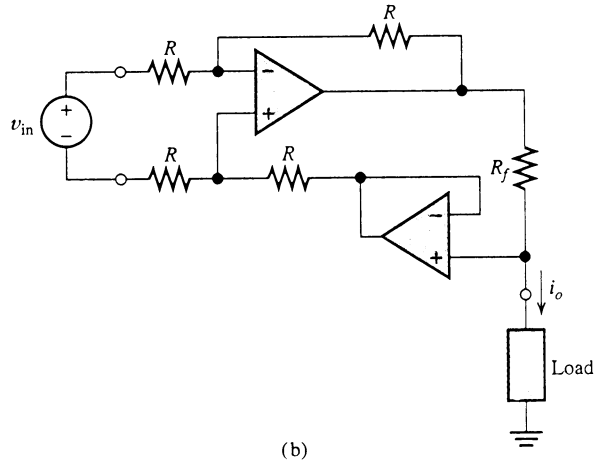
$I_A \approx 2.1mA$



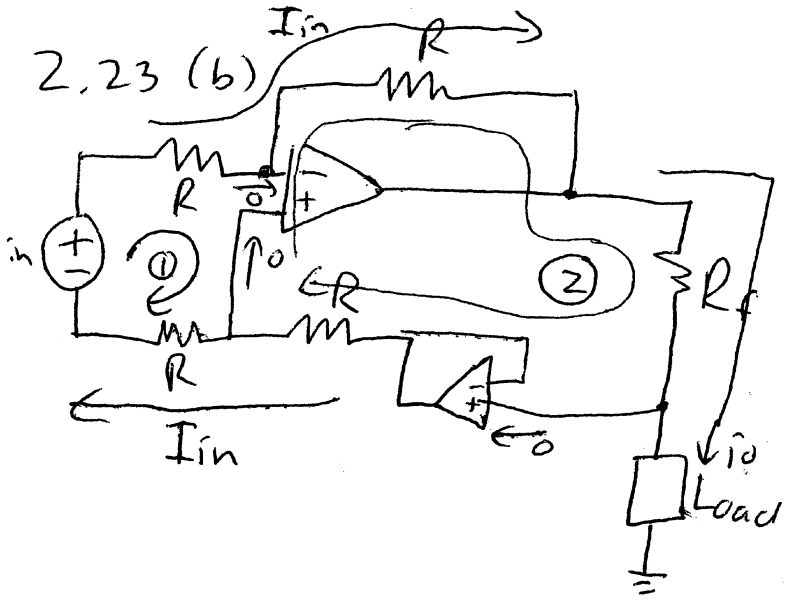
(b)



2.23.



(b)



First, because $i_n = i_p = 0$, $i_{in} + i_{out}$ must flow as shown on the diagram. Once we know this, we can apply KVL around 2 loops to get the relationship.

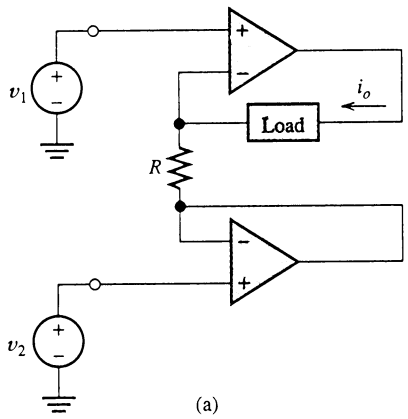
Loop 1: $V_{in} = I_{in}R + 0 + I_{in}R$ $\quad V_{in} = 2I_{in}R$

Loop 2: $RI_{in} + R_f I_o + RI_{in} = 0$ $\quad 2I_{in}R = -R_f I_o$

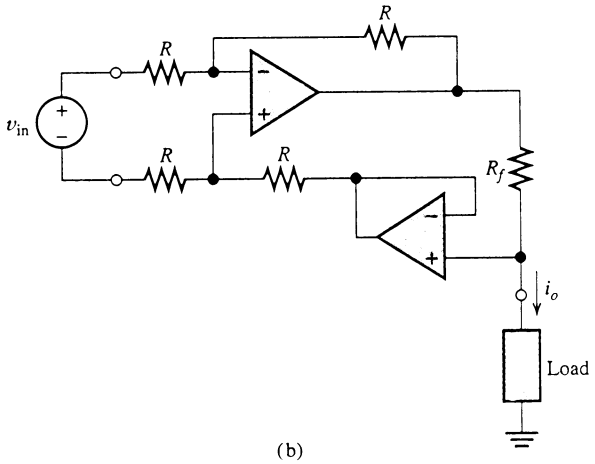
Solving, $\boxed{i_o = -V_{in}/R_f}$ since i_o is independent of load

$\boxed{\text{Output impedance} = \infty}$

2.23. Analyze each of the ideal op-amp circuits shown in Figure P2.23 to find expressions for i_o. What is the value of the output resistance (seen by the load) for each of these circuits? Why?

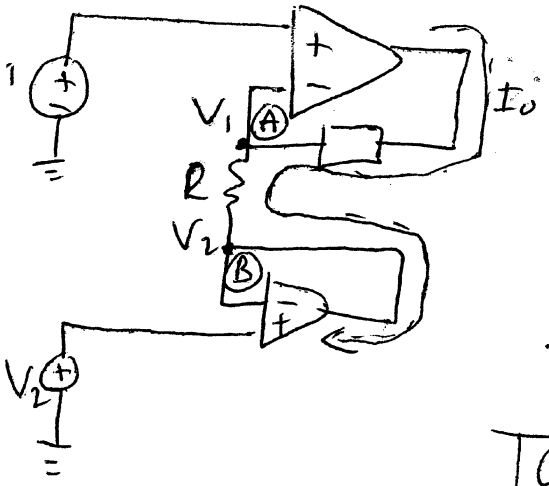


(a)



(b)

2.23 (a)



$V_p = V_n \therefore V_A = V_1 \& V_B = V_2$

Since $i_n = 0$ for both OP-Amps, i_o must travel as shown.

$i_o = \frac{V_A - V_B}{R} \therefore \boxed{i_o = \frac{V_1 - V_2}{R}}$

i_o is independent of load $\therefore$

$\boxed{\text{Output impedence} = \infty}$

2.22. Analyze the ideal op-amp circuit shown in Figure P2.22 to find an expression for v_o in terms of v_A, v_B, and the resistor values.

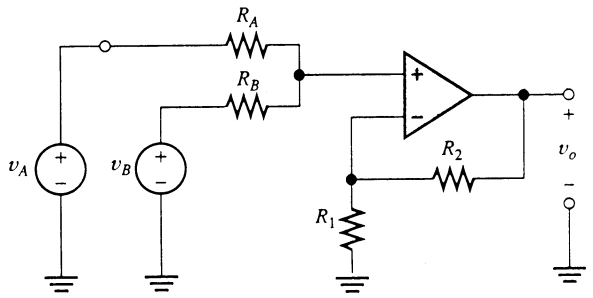
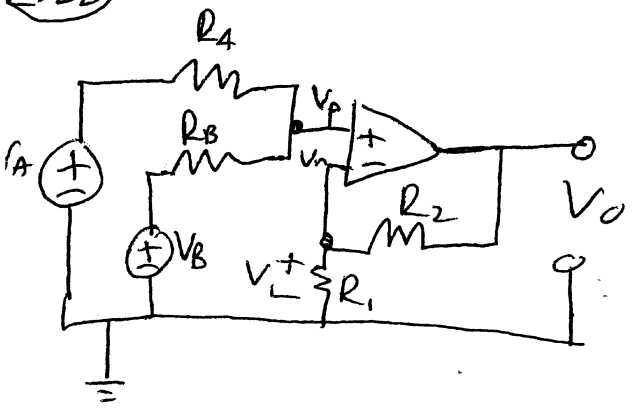


Figure P2.22

2.22



$V_n = V_p = V_1$. Now, ip must be 0 since this is the input of an OP-AMP $\therefore$

$$\frac{V_A - V_1}{R_A} + \frac{V_1 - V_B}{R_B} = 0 \quad \text{solving,}$$

$$V_1 = \frac{V_A R_B + V_B R_A}{R_A + R_B}$$

Now, rest of the circuit is a standard non-inverting amplifier:

$$V_o = \frac{R_1 + R_2}{R_1} V_1 \quad \therefore \quad \boxed{V_o = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{V_A R_B + V_B R_A}{R_A + R_B}\right)}$$

2.14. Determine the closed-loop voltage gain of the circuit shown in Figure P2.14, assuming an ideal op amp. All of the resistors are equal in value.

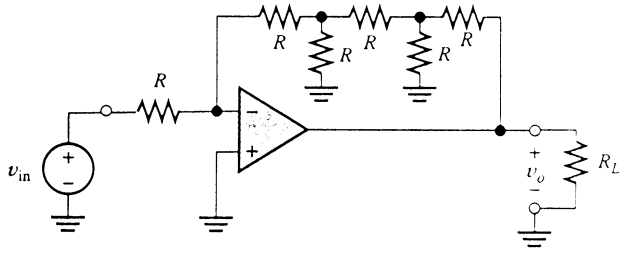
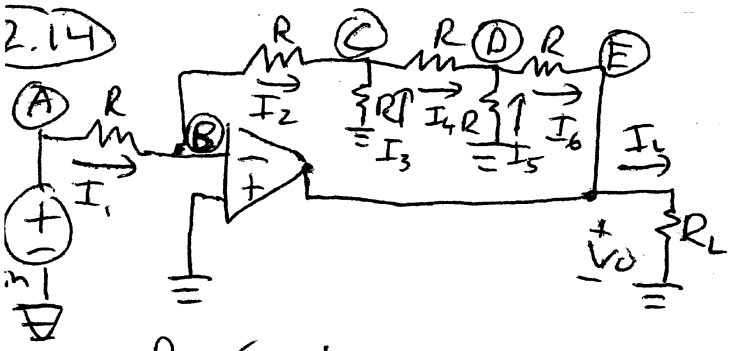


Figure P2.14

2.14



Refer to labeled diagram.

$V_B = 0$ since $V_p = V_n$ for OP-Amp

$I_1 = \frac{A-B}{R} = \frac{V_{in}}{R} = I_1$

$I_1 = I_2$ since $I_n = 0$

$I_2 = \frac{B-C}{R} = \frac{V_{in}}{R} \therefore C = -V_{in}$ $I_3 = \frac{0-C}{R} \therefore I_3 = \frac{V_{in}}{R}$

$I_4 = I_3 + I_2 = \frac{2V_{in}}{R}$ $I_4 = \frac{C-D}{R} = \frac{2V_{in}}{R}$ $D = -3V_{in}$

$D = -3V_{in}$ $I_5 = \frac{0-D}{R} \therefore I_5 = \frac{3V_{in}}{R}$

$I_6 = I_5 + I_4 \therefore I_6 = \frac{5V_{in}}{R}$ $I_6 = \frac{D-E}{R}$ $E = -8V_{in}$

$E = V_o \therefore V_o = -8V_{in}$ $\boxed{V_o/V_{in} = -8}$

4–5 The circuit in Figure P4–5 is an ideal current amplifier with negative feedback via the resistor R_E.

(a) For $i_S = 25\ \mu A$ and $R_E = 250\ \Omega$, find the output current i_2 and the voltage gain v_2/v_1.

(b) Find the input resistance $R_{IN} = v_1/i_1$.

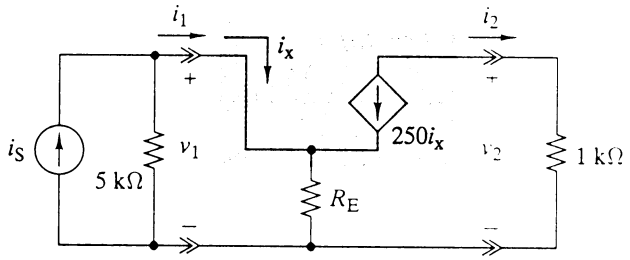
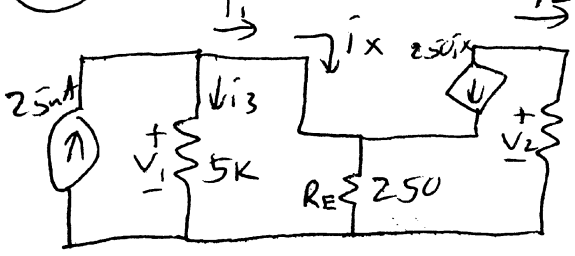


FIGURE P4–5

4.5



(1) $i_1 = i_x$ (2) $i_2 = -250 i_x$

(3) $V_1 = 25 i_x R_E$ (4) $i_1 + i_3 = 25uA$

(5) $V_1 = i_3 \cdot 5K$ (6) $V_2 = i_2 \cdot 1K$

Substituting (5) & (1) into (4) gives $i_x + \frac{V_1}{5K} = 25uA$. Placing (3) into this yields $i_x + 25 i_x \frac{R_E}{5K} = 2uA$ $R_E = 250 \therefore$ $\underline{i_x = 1.845uA}$

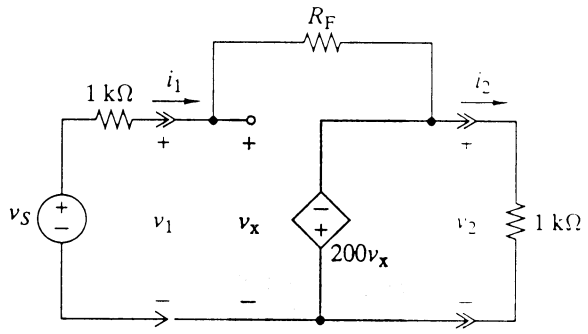
By (2) $\boxed{i_2 = -0.461mA}$ By (6), $\underline{V_2 = -.461}$ By (3), $V_1 = .11577 \therefore$

$\boxed{\frac{V_2}{V_1} = -3.98}$ $\boxed{\frac{V_1}{i_1} = 62.75\ K\Omega}$

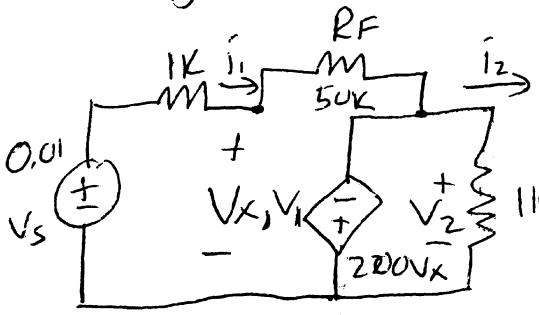
4–4 The circuit in Figure P4–4 is an ideal voltage amplifier with negative feedback provided via the resistor R_F.

(a) For $v_S = 10$ mV and $R_F = 50$ kΩ, find the output voltage v_2 and the current gain i_2/i_1.

(b) Find the input resistance $R_{IN} = v_1/i_1$.



(4.4) The key to solving linear-dependent source circuits is writing down all of the device equations.



(1) $V_2 = -200V_x$ (2) $V_x = V_1$

(3) $V_S = V_x + i_1(1K)$

(4) $i_1 = \frac{V_x - V_2}{R_F}$ (5) $i_2 = \frac{V_2}{1K}$

Substituting (1) into (4) gives $\frac{V_x + 200V_x}{R_F} = i_1$ By (3), $i_1 = \frac{V_S - V_x}{1K}$ ∴

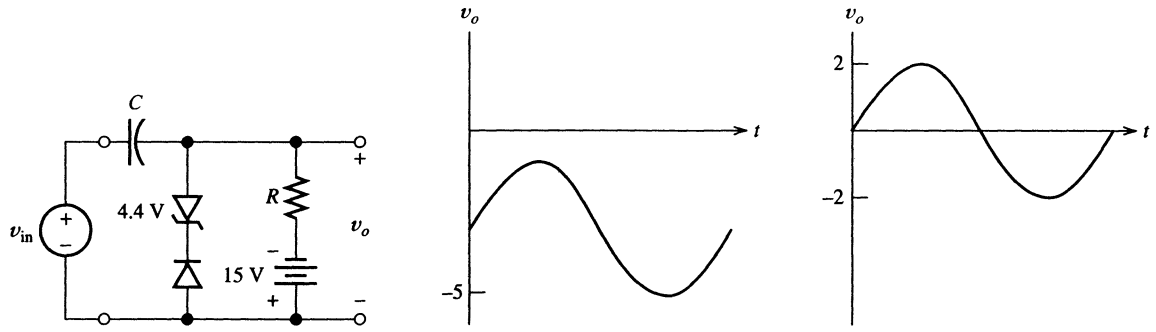
$\frac{V_x + 200V_x}{R_F} = \frac{V_S - V_x}{1K}$. $V_S = 0.01$, so $V_x = 2mV$ By (2), $\boxed{V_2 = -0.4V}$

By (5), $i_2 = -0.4mA$. By (4), $i_1 = 8.04uA$ $\boxed{\frac{i_2}{i_1} = -49.8}$

$\boxed{\frac{V_1}{i_1} = 249\Omega}$

D3.37. Clamp-circuit design. Design a clamp circuit to clamp the negative extreme of a periodic input waveform to −5 V. Use diodes, Zener diodes, and standard 5%-tolerance resistor values. Assume a 0.6-V forward drop for all diodes, and suppose that the Zener diodes have an ideal characteristic in the breakdown region. Power-supply voltages of ±15 V are available. *Look at Figure 3.20a for ideas.*

D3.38. Clamp-circuit design. Repeat Problem D3.37 to clamp the positive extreme to +5 V. *Look at Figure 3.20a for ideas.*

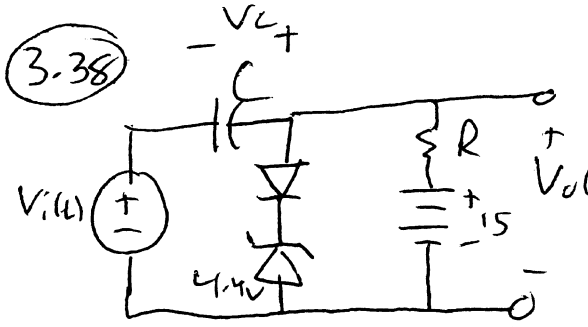


(a) A circuit that clamps the negative peaks to –5 V (an allowance of 0.6 V forward drop is made)

(b) Output for $v_{in} = 2\sin(\omega t)$

(c) Output for $v_{in} = 2\sin(\omega t)$ and R returned directly to ground (diodes do not turn on)

Figure 3.20



Circuit operation: With no input, ($V_i(t)=0$), Diodes will activate, Charging capacitor until $V_c = V_o = 5V$. Then, diodes shut off. If $RC \gg T$, where T is the period of $V_i(t)$, when $V_i(t)$ is turned On, Vc will remain almost constant. If $V_i(t) < 5V$, this will be passed directly to Vo. If $V_i(t) > 5V$, diodes will conduct, increasing Vc + keeping maximum at 5V. The battery is there to initially charge the capacitor to the 5V bias.