chapter

Field-Effect Transistors 9

9-1 INTRODUCTION

A field-effect transistor (FET) may be specified by a device statement. PSpice generates complex models for FETs. These models are quite complex and incorporate an extensive range of device characteristics (e.g., dc and small-signal behavior, temperature dependency, and noise generation). If such complex models are not necessary, users can ignore many model parameters, and PSpice assigns default values to the parameters. The FETs are of three types:

Junction field-effect transistors (JFETs)
Metal-oxide silicon field-effect transistors (MOSFETs)
Gallium arsenide MESFETs

9-2 JUNCTION FIELD-EFFECT TRANSISTORS

The PSpice JFET model is based on the FET model of Schichman and Hodges [1]. The model of an *n*-channel JFET is shown in Fig. 9-1. The small-signal model and the static (or dc) model, which are generated by PSpice, are shown in Figs. 9-2 and 9-3, respectively. The model parameters for a JFET device and the default values assigned by PSpice are given in Table 9-1. The model equations of JFETs that are used by PSpice are described in Schichman and Hodges [1], Vladimirescu and Liu [3], and the *PSpice Manual* [7].

The model statement of an *n*-channel JFET has the general form

```
.MODEL  JNAME  NJF  (P1=A1 P2=A2 P3=A3 ... PN=AN)
```

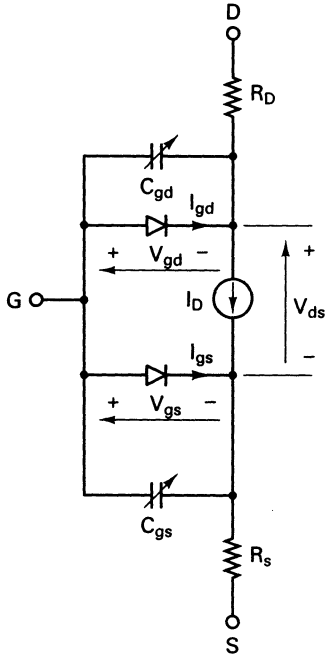


Figure 9-1 PSpice *n*-channel JFET.

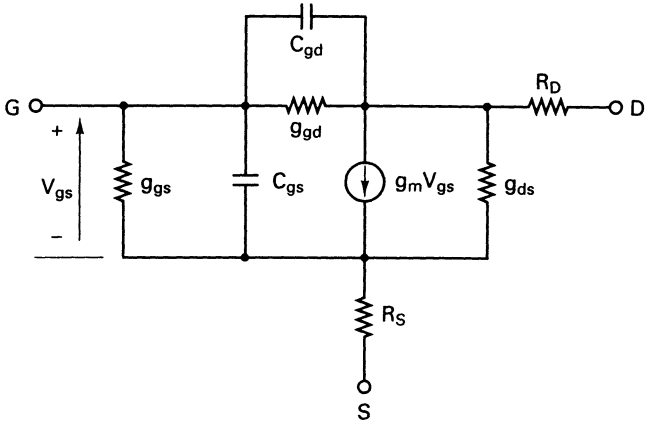


Figure 9-2 Small-signal *n*-channel JFET model.

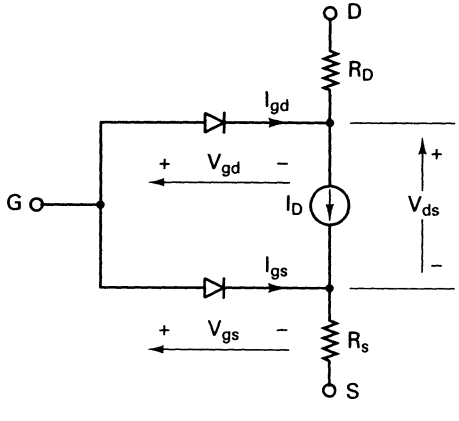


Figure 9-3 Static *n*-channel JFET model.

TABLE 9-1 MODEL PARAMETERS OF JFETS

Name	Area	Model parameters	Units	Default	Typical
VTO		Threshold voltage	Volts	−2	−2
BETA	*	Transconductance coefficient	Amps/Volts^2	1E−4	1E−3
LAMBDA		Channel-length modulation	Volts^{-1}	0	1E−4
RD	*	Drain ohmic resistance	Ohms	0	100
RS	*	Source ohmic resistance	Ohms	0	100
IS	*	Gate *p-n* saturation current	Amps	1E−14	1E−14
PB		Gate *p-n* potential	Volts	1	0.6
CGD	*	Gate-drain zero-bias *p-n* capacitance	Farads	0	5PF
CGS	*	Gate-source zero-bias *p-n* capacitance	Farads	0	1PF
FC		Forward-bias depletion capacitance coefficient		0.5	
VTOTC		VTO temperature coefficient	Volts/°C	0	
BETATCE		BETA exponential temperature coefficient	percent/°C	0	
KF		Flicker noise coefficient		0	
AF		Flicker noise exponent		1	

and for a *p*-channel JFET, the statement has the form

```
.MODEL  JNAME  PJF (P1=A1 P2=A2 P3=A3 ... PN=AN)
```

where JNAME is the model name; it can begin with any character and its word size is normally limited to eight characters. NJF and PJF are the type symbols of *n*-channel and *p*-channel JFETs, respectively. P1, P2, . . . and A1, A2, . . . are the parameters and their values, respectively.

As with diodes and BJTs, an *area factor* is used to determine the number of equivalent parallel JFETs. The model parameters that are affected by the area factor are marked by an asterisk (*) in Table 9-1. The [(area) value] scales BETA, RD, RS, CGD, CGS, and IS; it defaults to 1.

RD and RS represent the contact and bulk resistances per unit area of the drain and source, respectively. The JFET is modeled as an intrinsic device. The area value, which is the relative device area, is specified in the .MODEL statement and changes the actual resistance values. The default value of the area is 1.

The dc characteristics that are represented by the nonlinear current source I_D are defined (1) by parameters VTO and BETA, which determine the variation of the drain current with the gate voltage, (2) by LAMBDA, which determines the output conductance, and (3) by IS, which determines the reserve saturation current of the two gate junctions. VTO is negative for depletion-mode JFETs, both for *n*-channel and *p*-channel types, and it is positive for enhancement-mode JFETs. VTO does not identify whether the JFET is *n*-channel or *p*-channel.

The symbol for a JFET is *J*. The name of a JFET must start with *J* and it takes the general form of

```
J⟨name⟩ ND  NG  JNAME  [(area) value]
```

where ND, NG and NS are the drain, gate, and source nodes, respectively.

Some JFET Statements

```
JIM  5   6  8  JNAME
.MODEL JNAME  NJF
J15  3   9  12  SWITCH  1.5
.MODEL SWITCH NJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 VTO=-5)
JQ   1   5   9   JMOD
.MODEL JMOD PJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 CGD=5PF CGS=1PF
+VTO=5)
```

9-3 JFET PARAMETERS

The library file EVAL.LIB of the student version of PSpice supports models for n-channel JFETs: J2N3819 and J2N4393. As an example, we shall generate approximate values of some parameters [8, 9] from the data sheet of the n-channel JFET of type 2N5459, shown in Fig. 9-4.

I_{DSS} = 4 to 16 mA at V_{GS} = 0 V, and V_{DS} = 15 V. Taking the geometric mean,

$$I_{DSS} = \sqrt{(4 \times 16)} = 8 \text{ mA}$$

The threshold voltage, $V_{Th} = V_{GS(\text{off})} = -2$ to -8 V. Taking the geometric mean,

$$V_{Th} = -\sqrt{(2 \times 8)} = -4 \text{ V}$$

That is, VTO = -4 V (for depletion-mode).

The transconductance coefficient is given by

$$\text{BETA} = \frac{I_{DSS}}{V_{Th}^2} \tag{9-1}$$

$$= \frac{8 \text{ mA}}{(-4)^2} = 0.5 \text{ mA/V}^2$$

The gate reverse current $I_{GSS} = -\text{IS} = -1$ nA at $V_{GS} = -15$ V, and $V_{DS} = 0$.

The common-source reverse transfer capacitance, $C_{rss} = C_{gd}$ = 1.5 to 3 pF at V_{DS} = 15 V, and V_{GS} = 0 V. Taking the geometric mean,

$$C_{rss} = C_{gd} = \sqrt{(1.5 \times 3)} \text{ pF} = 2.12 \text{ pF}$$

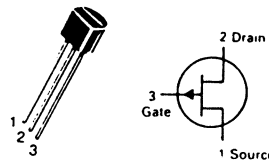
At $V_{DG} = V_{DS} - V_{GS} = 15 - 0 = 15$ V, C_{gdo} can be found from

$$C_{gd} = \frac{C_{gdo}}{(1 + V_{DG}/V_{\text{off}})^{1/3}} \tag{9-2}$$

where $V_{\text{off}} = 0.75$ V. Equation (9-2) gives, $C_{gdo} = 5.85$ pF.

2N5460 thru 2N5465

CASE 29-04, STYLE 7
TO-92 (TO-226AA)



JFET AMPLIFIER

P-CHANNEL — DEPLETION

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	V_{GSR}	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82		mW mW/°C
Junction Temperature Range	T_J	−65 to +135		°C
Storage Channel Temperature Range	T_{stg}	−65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	$V_{(BR)GSS}$	40 60	—	— —	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) (V_{GS} = 30 Vdc, V_{DS} = 0) (V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C) (V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465 2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465	I_{GSS}	— — — —	— — — —	5.0 5.0 1.0 1.0	nAdc μAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$V_{GS(off)}$	0.75 1.0 1.8	— — —	6.0 7.5 9.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc) (V_{DS} = 15 Vdc, I_D = 0.2 mAdc) (V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	V_{GS}	0.5 0.8 1.5	— — —	4.0 4.5 6.0	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	I_{DSS}	1.0 2.0 4.0	— — —	5.0 9.0 16	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465	$\lvert y_{fs} \rvert$	1000 1500 2000	— — —	4000 5000 6000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\lvert y_{os} \rvert$	—	—	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	1.0	2.0	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	—	1.0	2.5	dB
Equivalent Short-Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	—	60	115	$nV/\sqrt{Hz}$

Figure 9-4 Data sheet for the *n*-channel JFET of type 2N5459 (Courtesy of Motorola, Inc.).

The common-source input capacitance, C_{iss} = 4.5 to 7 pF at V_{DS} = 15 V, and V_{GS} = 0 V. Taking the geometric mean,

$$C_{iss} = \sqrt{(4.5 \times 7)}\ \text{pF} = 5.61\ \text{pF}$$

Since C_{iss} is measured at V_{GS} = 0 V, $C_{gs} = C_{gso}$. That is,

$$C_{iss} = C_{gso} + C_{gd}$$

which gives $C_{gso} = C_{iss} - C_{gd} = 5.61 - 2.12 = 3.49$ pF.

The output admittance $|Y_{os}|$ = 10 to 50 μmhos at V_{DS} = 15 V, and V_{GS} = 0. Taking the geometric mean,

$$|Y_{os}| = \sqrt{(10 \times 50)}\ \mu\text{mhos} = 22.36\ \mu\text{mhos}$$

Since $|Y_{os}|$ is given at V_{GS} = 0, the channel-modulation length λ (LAMBDA) can be found approximately from

$$\text{LAMBDA} = \frac{|Y_{os}|}{I_{DSS}} \approx \frac{22.36\ \mu\text{mhos}}{8\ \text{mA}} = 2.395\text{E}{-3}$$

The PSpice model statement for the JFET of type J2N5459 is

```
.MODEL J2N5459 NJF (IS=1N  VTO=-4  BETA=0.5M  CGDO=5.85PF
+                   CGSO=3.49PF    LAMBDA=2.395E-3)
```

9-4 EXAMPLES OF JFET AMPLIFIERS

The approximate values of JFET model parameters can be determined from the data sheet. If a model parameter is not specified, PSpice assumes its default value, as indicated in Table 9-1. The following examples illustrate the PSpice simulation of JFET circuits.

Example 9-1

For the *n*-channel JFET in Fig. 9-5, plot the output characteristics if V_{DD} is varied from 0 to 12 V in steps of 0.2 V and V_{GS} is varied from 0 to −4 V in steps of 1 V. The model parameters are IS=100E−14, RD=10, RS=10, BETA=1E−3, and VTO=−5.

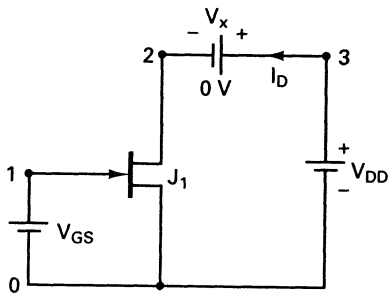


Figure 9-5 A circuit with an *n*-channel JFET.

The common-source input capacitance, C_{iss} = 4.5 to 7 pF at V_{DS} = 15 V, and V_{GS} = 0 V. Taking the geometric mean,

$$C_{iss} = \sqrt{(4.5 \times 7)}\ \text{pF} = 5.61\ \text{pF}$$

Since C_{iss} is measured at V_{GS} = 0 V, $C_{gs} = C_{gso}$. That is,

$$C_{iss} = C_{gso} + C_{gd}$$

which gives $C_{gso} = C_{iss} - C_{gd} = 5.61 - 2.12 = 3.49$ pF.

The output admittance $|Y_{os}|$ = 10 to 50 μmhos at V_{DS} = 15 V, and V_{GS} = 0. Taking the geometric mean,

$$|Y_{os}| = \sqrt{(10 \times 50)}\ \mu\text{mhos} = 22.36\ \mu\text{mhos}$$

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The PSpice model statement for the JFET of type J2N5459 is

```
.MODEL J2N5459 NJF (IS=1N  VTO=-4  BETA=0.5M  CGDO=5.85PF
+                   CGSO=3.49PF    LAMBDA=2.395E-3)
```

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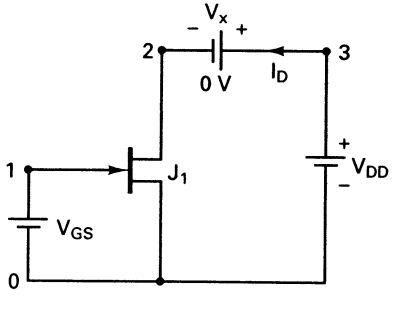


Figure 9-5 A circuit with an n-channel JFET.

Solution The listing of the circuit file follows.

Example 9-1 Output characteristics of an *n*-channel JFET

```
▲ *   Gate to source voltage of 0 V
  VGS  1  0  DC  0V
  *   A dummy voltage source of 0 V
  VX   3  2  DC  0V
  *   Dc supply voltage of 12 V
  VDD 3  0  DC  12V
▲▲ *  J1 with model JMOD
    J1   2  1  0  JMOD
    .MODEL  JMOD  NJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 VTO=-5)
▲▲▲ *   VDD is swept from 0 to 12 V and VGS from 0 to -4 V.
     .DC  VDD  0  12  0.2  VGS  0  -4  1
     .PLOT  DC  I(VX)
     .PROBE
.END
```

The output characteristics, which are plots of I_D versus V_{DD}, are shown in Fig. 9-6.

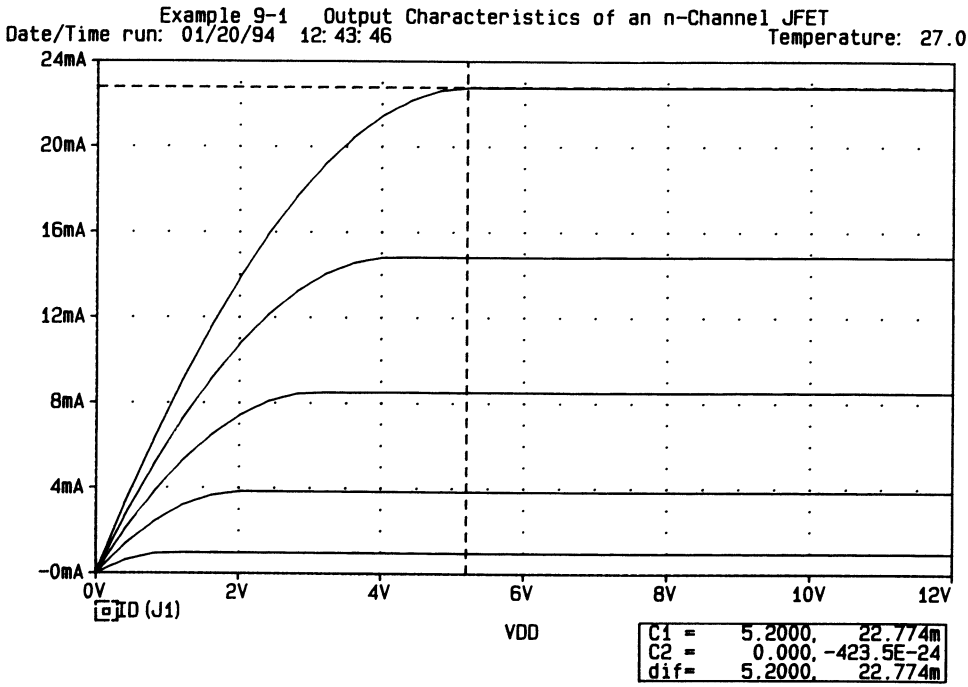


Figure 9-6 Output characteristics of the JFET in Example 9-1.

Example 9-2

For the JFET in Example 9-1, plot the input characteristic if V_{GS} is varied from 0 to -5 V in steps of 0.1 V, and $V_{DD} = 10$ V.

Solution The listing of the circuit file follows.

Example 9-2 Input characteristics of an *n*-channel JFET

```
▲ VGS   1   0   DC   0V
  VX    3   2   DC   0V
  *    Dc supply voltage of 10 V
  VDD   3   0   DC   10V
▲▲ *   J1 with model JMOD
    J1    2   1   0   JMOD
    .MODEL   JMOD   NJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 VTO=-5)
▲▲▲ *    VGS is swept from 0 to -5 V.
     .DC   VGS   0   -5V   0.1V
     .PLOT   DC   I(VX)
     .PROBE
.END
```

The input characteristic, which is a plot of I_D versus V_{GS}, is shown in Fig. 9-7.

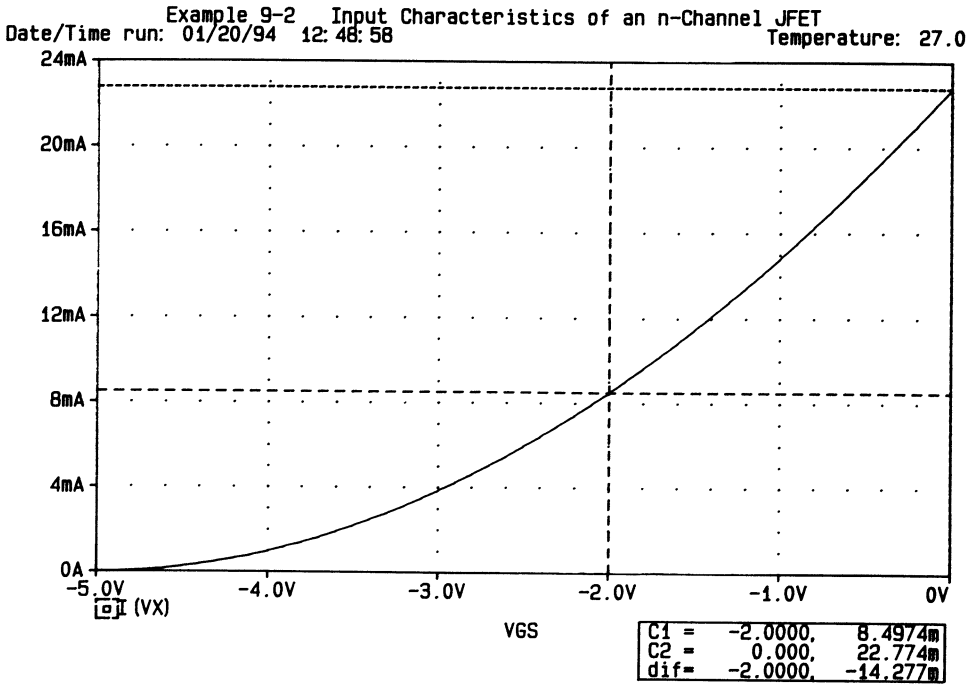


Figure 9-7 Input characteristic for Example 9-2.

Example 9-3

A JFET transistor amplifier circuit is shown in Fig. 9-8. The output is taken from node 6. If the input voltage is $v_{in} = 0.5 \sin(2000\pi t)$, use ac analysis to calculate and print the magnitudes and phase angles of the output voltage, the input current, and the load current. Plot the transient responses of the voltages at nodes 1, 4, and 6 from 0 to 1 ms in steps of 10 μs. The model parameters of the JFET are IS=100E−

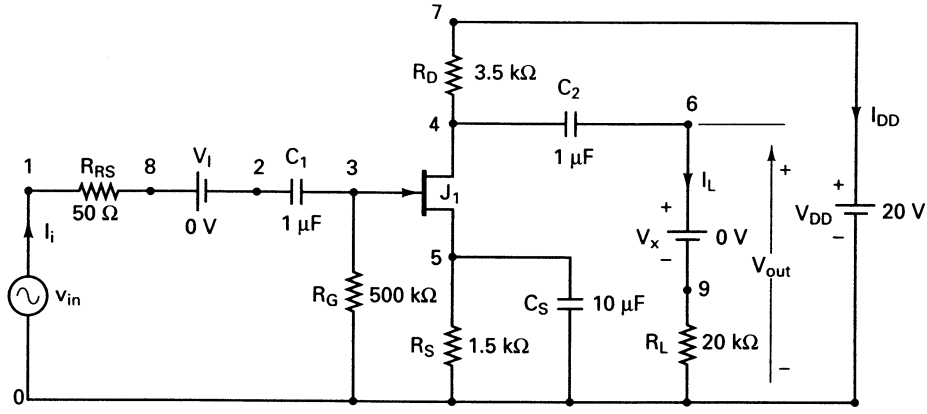


Figure 9-8 An *n*-channel JFET amplifier circuit.

14, RD=10, RS=10, BETA=1E−3, CGD=5PF, CGS=1PF, and VTO=−5. The details of the dc analysis and transient analysis operating points should be printed.

Solution The listing of the circuit file follows.

Example 9-3 An *n*-channel JFET amplifier

```
▲ .OPTIONS  NOPAGE  NOECHO
  *  Input voltage has 0.5 V peak at 1 kHz with zero offset value for
  *  transient response and 0.5 V peak for frequency response.
  VIN  1  0  AC  0.5V  SIN (0  0.5V  1KHZ)
  VDD  7  0  DC  20V
  *  Dummy voltage source of 0 V
  VI  8  2  DC  0V
  VX  6  9  DC  0V
▲▲ RRS  1  8  50
   RG  3  0  0.5MEG
   RD  7  4  3.5K
   RS  5  0  1.5K
   RL  9  0  20K
   C1  2  3  1UF
   C2  4  6  1UF
   CS  5  0  10UF
   *  n-channel JFET with model JMOD
   J1  4  3  5  JMOD
   .MODEL JMOD NJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 CGD=5PF CGS=1PF VTO=-5)
▲▲▲ *  Ac analysis at 1 kHz with a linear increment and only 1 point
   .AC  LIN  1  1KHZ  1KHZ
   *  Transient analysis with details of transient analysis operating point
   .TRAN/OP  10US  1MS
   *  Print the details of the ac analysis operating point.
   .OP
   * Print the results of the ac analysis for the magnitudes of voltages at
   * node 6 and 1 and for the magnitude of current through resistance RRS
   * and the current through VX.
```

```
.PRINT AC  VM(6) VP(6) IM(RRS) IP(RRS)
.PRINT AC  IM(VI) IP(VI) IM(VX) IP(VX)
*  Plot transient response.
.PLOT TRAN V(6)  V(1)
.PROBE
.END
```

The equivalent circuit for determining the dc bias point is shown in Fig. 9-9. The details of the dc bias are given next.

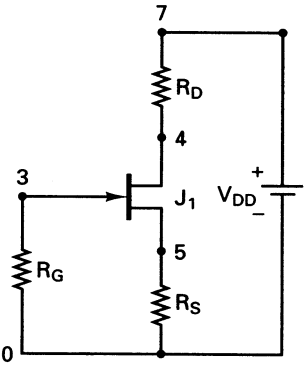


Figure 9-9 Equivalent circuit for dc bias calculation.

```
****     SMALL-SIGNAL BIAS SOLUTION                TEMPERATURE =  27.000 DEG C
NODE     VOLTAGE     NODE     VOLTAGE     NODE     VOLTAGE     NODE     VOLTAGE
(   1)    0.0000     (   2)    0.0000     (   3)  8.694E-06    (   4)   11.9300
(   5)    3.4585     (   6)    0.0000     (   7)    20.0000    (   8)    0.0000
(   9)    0.0000

   VOLTAGE SOURCE CURRENTS
   NAME          CURRENT
   VIN           0.000E+00
   VDD          -2.306E-03
   VI            0.000E+00
   VX            0.000E+00
   TOTAL POWER DISSIPATION  4.61E-02  WATTS
```

Once the dc bias points are determined, the small-signal parameters of the JFET in Fig. 9-8 are calculated. The details of the operating points are given next.

```
****     OPERATING POINT INFORMATION               TEMPERATURE =  27.000 DEG C
****  JFETS
NAME          J1
MODEL         JMOD
ID            2.31E-03
VGS          -3.46E+00
VDS           8.47E+00
GM            3.04E-03
GDS           0.00E+00
CGS           4.72E-13
CGD           1.39E-12
```

The outputs at a frequency of 1 kHz are as follows.

FREQ	VM(6)	VP(6)	IM(RRS)	IP(RRS)
1.000E+03	4.382E+00	−1.769E+02	9.990E−07	2.555E+00
FREQ	IM(VI)	IP(VI)	IM(VX)	IP(VX)
1.000E+03	9.990E−07	2.555E+00	2.191E−04	−1.769E+02

The equivalent circuit for determining the transient analysis bias point is shown in Fig. 9-10. The transient analysis bias point and the operating point are the same as those of the dc analysis because the capacitors do not have any initial voltages. The transient responses are shown in Fig. 9-11.

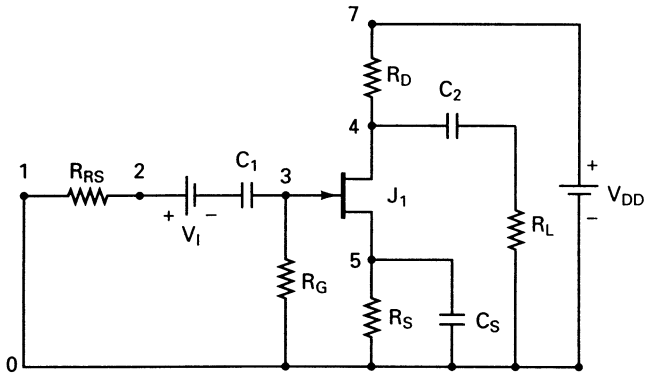


Figure 9-10 Equivalent circuit for transient analysis bias calculation.

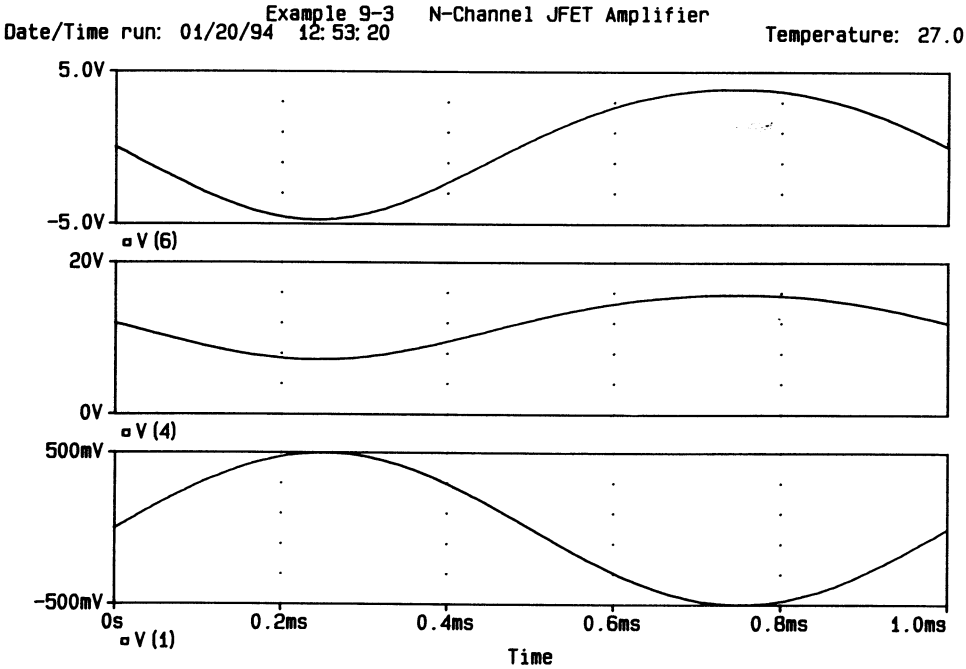


Figure 9-11 Transient responses for Example 9-3.

If the JFET in Fig. 9-8 is replaced by the subcircuit model of Figure 9-12, plot the frequency response of the output voltage. The frequency is varied from 10 Hz to 100 MHz with a decade increment and 10 points per decade.

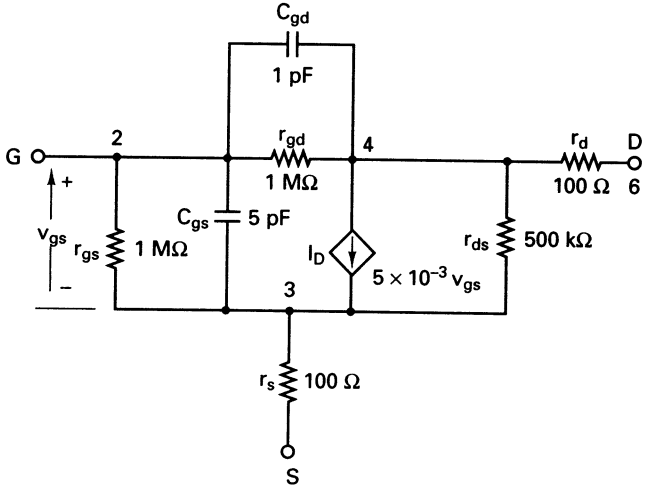


Figure 9-12 Subcircuit model for JFET of Example 9-4.

Solution The listing of the circuit file follows.

Example 9-4 An *n*-channel JFET amplifier

```
▲ .OPTIONS  NOPAGE  NOECHO
  * Input voltage has 0.5 V peak for frequency response.
  VIN  1  0  AC  0.5V
  VDD  7  0  DC  20V
  * Dummy voltage source of 0V
  VI  8  2  DC  0V
  VX  6  9  DC  0V
▲▲ RRS  1  8  50
   RG  3  0  0.5MEG
   RD  7  4  3.5K
   RS  5  0  1.5K
   RL  9  0  20K
   C1  2  3  1UF
   C2  4  6  1UF
   CS  5  0  10UF
   * Calling subcircuit for TRANS
   XQ1 4  3  5  TRANS
   * Subcircuit definition for TRANS
   .SUBCKT  TRANS  6  2  5
   RD  4  6  100
   RS  3  5  100
   RGS 2  3  1MEG
   CGS 2  3  5PF
   RGD 2  4  1MEG
   CGS 2  4  1PF
```

```
RDS 4  3  500K
*   Voltage-controlled current source with a gain of 5E-3
G1  4  3  2  3  5E-3
.ENDS  TRANS
*  Ac analysis for 100 Hz to 100 MHz with a decade increment and
*  10 points per decade
.AC  DEC  10  10HZ  100MEGHZ
*  Plot the results of the ac analysis for the magnitudes and phases of
*  output voltage and the magnitudes of input and load currents.
.PLOT  AC  VM(6) VP(6)
.PLOT  AC  IM(VI) IM(VX)
.PROBE
.END
```

The frequency response for Example 9-4 is shown in Fig. 9-13. The .PLOT statement generates graphical plots in the output file. If the .PROBE command is included, there is no need for the .PLOT command.

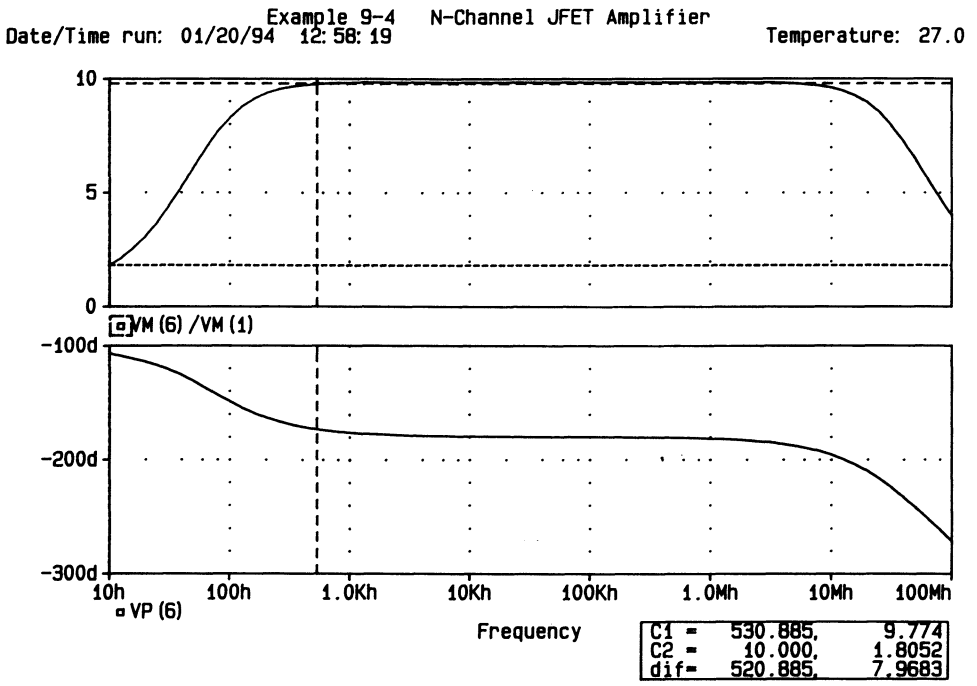


Figure 9-13 Frequency response for Example 9-4.

Example 9-5

A *p*-channel JFET bootstrapped amplifier is shown in Fig. 9-14. The output is taken from node 5. Calculate and print the voltage gain, the input resistance, and the output resistance. The model parameters of the JFET are IS=100E−14, RD=10, RS=10, BETA=1E−3, and VTO=5.

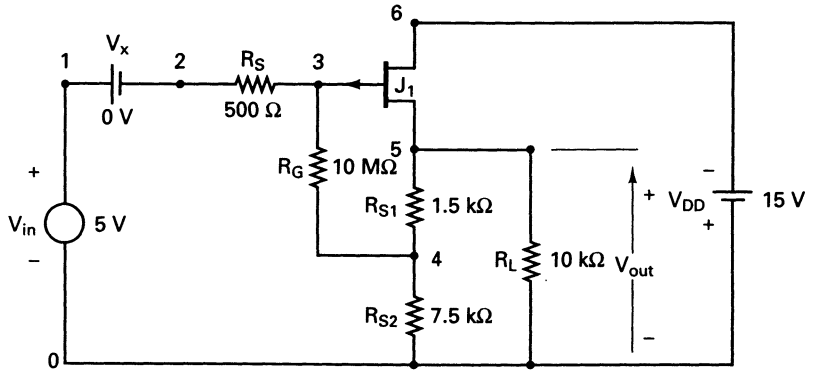


Figure 9-14 A *p*-channel JFET bootstrapped amplifier.

Solution The listing of the circuit follows.

Example 9-5 Bootstrapped JFET amplifier

```
▲ VDD  0   6   15V
  *   Input voltage of 5 V dc
  VIN  1   0    DC   5V
  *   A dummy voltage source of 0 V
  VX   1   2   DC  0V
▲▲ RS   2   3    500
   RG   3   4   10MEG
   RS1  5   4   1.5K
   RS2  4   0   7.5K
   RL   5   0    10K
   *  p-channel JFET of model JMOD
   JX   6   3   5  JMOD
   *  Model statement for p-channel JFET
   .MODEL JMOD PJF (IS=100E-14 RD=10 RS=10 BETA=1E-3 VTO=5)
▲▲▲ *   Transfer function analysis between the output and input voltages
    .TF  V(5)  VIN
.END
```

The results of the transfer function analysis are

```
****      SMALL-SIGNAL CHARACTERISTICS
     V(5)/VIN = -9.257E-01
     INPUT RESISTANCE AT VIN =  4.375E+07
     OUTPUT RESISTANCE AT V(5) =  3.521E+02
         JOB CONCLUDED
         TOTAL JOB TIME            9.50
```

9-5 METAL OXIDE SILICON FIELD-EFFECT TRANSISTORS

The PSpice model of an *n*-channel MOSFET [1–3] is shown in Fig. 9-15. The small-signal model and the static (or dc) model generated by PSpice are shown in

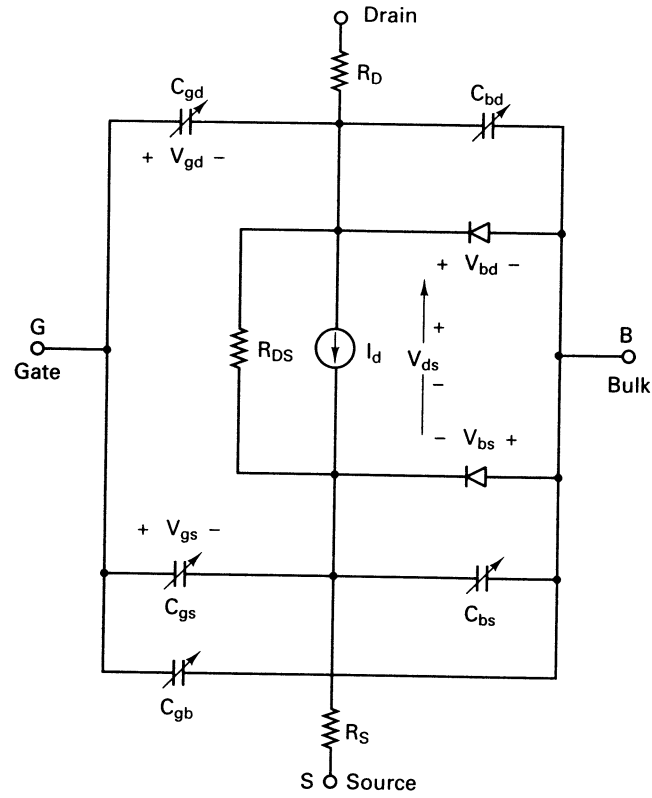


Figure 9-15 PSpice *n*-channel MOSFET model.

Figs. 9-16 and 9-17, respectively. The model parameters for a MOSFET device and the default values assigned by PSpice are given in Table 9-2. The model equations of MOSFETs that are used by PSpice are described in Schichman and Hodges [1], Vladimirescu and Liu [3], and the *PSpice Manual* [7].

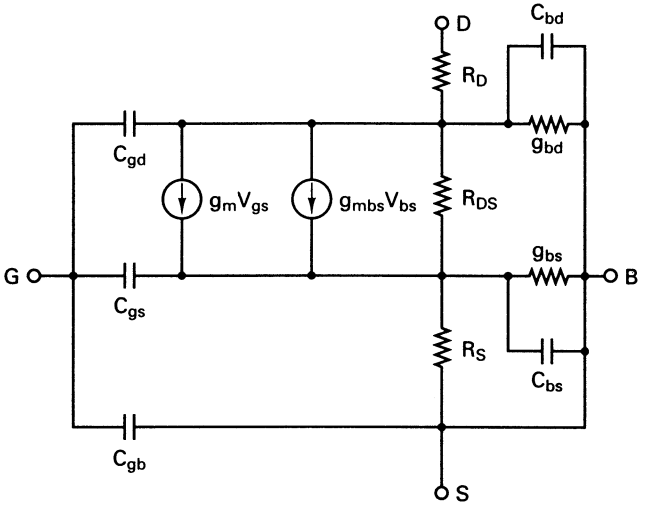


Figure 9-16 Small-signal *n*-channel MOSFET model.

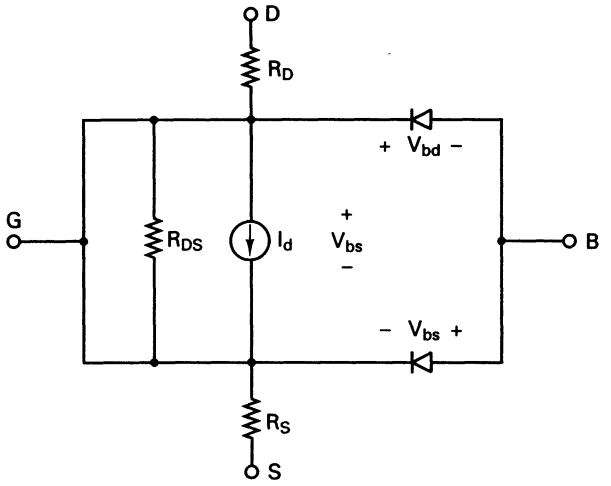


Figure 9-17 Static *n*-channel MOSFET model.

TABLE 9-2 MODEL PARAMETERS OF MOSFETS

Name	Model parameters	Units	Default	Typical
LEVEL	Model type (1, 2, or 3)		1	
L	Channel length	meters	DEFL	
W	Channel width	meters	DEFW	
LD	Lateral diffusion length	meters	0	
WD	Lateral diffusion width	meters	0	
VTO	Zero-bias threshold voltage	Volts	0	0.1
KP	Transconductance	Amps/Volts^2	2E−5	2.5E−5
GAMMA	Bulk threshold parameter	Volts$^{1/2}$	0	0.35
PHI	Surface potential	Volts	0.6	0.65
LAMBDA	Channel-length modulation (LEVEL = 1 or 2)	Volts^{-1}	0	0.02
RD	Drain ohmic resistance	Ohms	0	10
RS	Source ohmic resistance	Ohms	0	10
RG	Gate ohmic resistance	Ohms	0	1
RB	Bulk ohmic resistance	Ohms	0	1
RDS	Drain-source shunt resistance	Ohms	∞	
RSH	Drain-source diffusion sheet resistance	Ohms/square	0	20
IS	Bulk *p-n* saturation current	Amps	1E−14	1E−15
JS	Bulk *p-n* saturation current/area	Amps/meters^2	0	1E−8
PB	Bulk *p-n* potential	Volts	0.8	0.75
CBD	Bulk-drain zero-bias *p-n* capacitance	Farads	0	5PF
CBS	Bulk-source zero-bias *p-n* capacitance	Farads	0	2PF
CJ	Bulk *p-n* zero-bias bottom capacitance/length	Farads/meters^2	0	
CJSW	Bulk *p-n* zero-bias perimeter capacitance/length	Farads/meters	0	
MJ	Bulk *p-n* bottom grading coefficient		0.5	

(*continued*)

TABLE 9-2 *Continued*

Name	Model parameters	Units	Default	Typical
MJSW	Bulk *p-n* sidewall grading coefficient		0.33	
FC	Bulk *p-n* forward-bias capacitance coefficient		0.5	
CGSO	Gate-source overlap capacitance/channel width	Farads/meters	0	
CGDO	Gate-drain overlap capacitance/channel width	Farads/meters	0	
CGBO	Gate-bulk overlap capacitance/channel length	Farads/meters	0	
NSUB	Substrate doping density	$1/centimeter^3$	0	
NSS	Surface-state density	$1/centimeter^2$	0	
NFS	Fast surface-state density	$1/centimeter^2$	0	
TOX	Oxide thickness	meters	∞	
TPG	Gate material type: +1 = opposite of substrate, −1 = same as substrate, 0 = aluminum		+1	
XJ	Metallurgical junction depth	meters	0	
UO	Surface mobility	$centimeters^2/Volts \cdot seconds$	600	
UCRIT	Mobility degradation critical field (LEVEL = 2)	Volts/centimeter	1E4	
UEXP	Mobility degradation exponent (LEVEL = 2)		0	
UTRA	(Not used) mobility degradation transverse field coefficient			
VMAX	Maximum drift velocity	meters/second	0	
NEFF	Channel charge coefficient (LEVEL = 2)		1	
XQC	Fraction of channel charge attributed to drain		1	
DELTA	Width effect on threshold		0	
THETA	Mobility modulation (LEVEL = 3)	$Volts^{-1}$	0	
ETA	Static feedback (LEVEL = 3)		0	
KAPPA	Saturation field factor (LEVEL = 3)		0.2	
KF	Flicker noise coefficient		0	1E−26
AF	Flicker noise exponent		1	1.2

The model statement for *n*-channel MOSFETs has the general form

```
.MODEL  MNAME  NMOS  (P1=A1  P2=A2  P3=A3 ... PN=AN)
```

and the statement for *p*-channel MOSFETs has the form

```
.MODEL  MNAME  PMOS  (P1=A1  P2=A2  P3=A3 ... PN=AN)
```

where MNAME is the model name; it can begin with any character, and its word size is normally limited to eight characters. NMOS and PMOS are the type symbols of *n*-channel and *p*-channel MOSFETs, respectively. P1, P2, . . . and A1, A2, . . . are the parameters and their values, respectively.

In Table 9-2 L and W are the channel length and width, respectively. AD and AS are the drain and source diffusion areas. L is decreased by twice LD to get the effective channel length. Similarly, W is decreased by twice WD to get the effective channel width. L and W can be specified for the device, the model, or in the .OPTION statement. PSpice sets priority in selecting their values. The value specified for the device supersedes that for the model, which supersedes that in the .OPTION statement.

AD and AS are the drain and source diffusion areas. PD and PS are the drain and source diffusion perimeters. The drain *p-n*-saturation current can be specified either by IS in an absolute value, or by JS, which is multiplied by AD and AS. The zero-bias depletion capacitances can be specified (1) by CBD and CBS in absolute values, (2) by CJ, which is multiplied by AD and AS, or (3) by CJSW, which is multiplied by PD and PS.

Contact and bulk resistances are included in series with the drain, source, gate, and bulk (substrate). The MOSFET is modeled as an intrinsic device. RDS is a shunt resistance in parallel with the drain-source channel. These ohmic resistances can be specified in absolute values of RD, RS, RG, and RB. Alternatively, one could specify these resistances by RSH, which is multiplied by NRD, NRS, NRG, and NRB, respectively. NRD, NRS, NRG, and NRB are the relative resistivities of the drain, source, gate, and substrate in squares.

PD, PS, NRG, and NRB default to 0. NRD and NRS default to 1. Defaults for L, W, AD, and AS may be set in the .OPTIONS statement. The default value of AD or AS is 0. The default value of L or W is 100 μm.

The dc characteristics are defined by parameters VTO, KP, LAMBDA, PHI, and GAMMA, which are computed by PSpice by using the fabrication-process parameters NSUB, TOX, NSS, NFS, TPG, and so on. The values of VTO, KP, LAMDA, PHI, and GAMMA, which are specified in the model statement, supersede the values calculated by PSpice based on fabrication-process parameters. *VTO is positive for enhancement type n-channel MOSFETs and for depletion type p-channel MOSFETs. VTO is negative for enhancement type p-channel MOSFETs and for depletion type n-channel MOSFETs.*

PSpice incorporates three MOSFET device models. The LEVEL parameter selects among different models for the intrinsic MOSFET. If LEVEL = 1, the Schichman-Hodges model [1] is used. If LEVEL = 2, an advanced version of the Schichman-Hodges model, which is a geometry-based analytical model and incorporates extensive second-order effects [3], is used. If LEVEL = 3, a modified version of the Schichman-Hodges model, which is a semiempirical short-channel model [3], is used.

The LEVEL 1 model, which employs fewer fitting parameters, gives approximate results. However, it is useful for a quick and rough estimate of the circuit performances and it is normally adequate for the analysis of basic electronic circuits. The LEVEL 2 model, which can take into consideration various

parameters, requires a great amount of CPU time for the calculations and could cause convergence problems. The LEVEL 3 model introduces a smaller error as compared to the LEVEL 2 model, and the CPU time is also approximately 25% less. The LEVEL 3 model is designed for MOSFETs with short channels.

The symbol for a metal-oxide silicon field-effect transistor (MOSFET) is *M*. The name of a MOSFET must start with *M* and takes the general form

```
M⟨name⟩  ND   NG   NS   NB   MNAME
+       [L=⟨value⟩] [W=⟨value⟩]
+       [AD=⟨value⟩] [AS=⟨value⟩]
+       [PD=⟨value⟩] [PS=⟨value⟩]
+       [NRD=⟨value⟩] [NRS=⟨value⟩]
+       [NRG=⟨value⟩] [NRB=⟨value⟩]
```

where ND, NG, NS, and NB are the drain, gate, source, and bulk (or substrate) nodes, respectively. MNAME is the model name, and it can begin with any character; its word size is normally limited to eight characters. Positive current is the current that flows into a terminal. That is, the current flows from the drain node through the device to the source node for an *n*-channel MOSFET.

Some MOSFET Statements

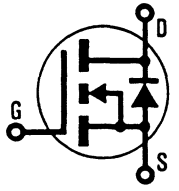
```
M1    4   2   7    0 MMOD   L=10U W=20U
.MODEL   MMOD   NMOS
M13   15   3   0   0   IRF150
.MODEL IRF150   NMOS (LEVEL=3 TOX=.10U L=3.0U LD=.5U W=2.0 WD=0
+XJ=1.2U
+       NSUB=4E14 IS=2.1E-14 RB=0 RD=.01 RS=.03 RDS=1E6 VTO=3.25
+       U0=550 THETA=.1 ETA=0 VMAX=1E6 CBS=1P CBD=4000P PB=.7 MJ=.5
+       RG=4.9 CGSO=1690P CGDO=365P CGBO=1P)
M2A   0   2   20   20   IRF9130
.MODEL IRF9130   PMOS (LEVEL=3 TOX=.1U L=3.0U LD=.5U W=1.3 WD=0
+XJ=1.2U
+       NSUB=4E14 IS=2.1E-14 RB=0 RD=.03 RS=.2 RDS=5E5 VTO=-3.7
+       U0=600 THETA=.1 ETA=0 VMAX=1E6 CBS=1P CBD=2000P PB=.7 MJ=.5
+       RG=5 CGSO=520P CGDO=180P CGBO=1P)
MA    0   2   15   15   PMOD   L=20U W=20U AD=100U AS=200U PD=50U
+                             PS=50U NRD=10 NRS=20 NRG=10
.MODEL PMOD   PMOS
```

9-6 MOSFET PARAMETERS

The data sheet for the *n*-channel MOSFET of type IRF150 is shown in Fig. 9-18. The library file EVAL.LIB of the student version of PSpice supports models for the *n*-type MOSFET of type IRF150 and the *p*-type MOSFET of type IRF9140. As an example, we shall generate approximate values of some parameters [8, 9] from the data sheet of IRF150.

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF150 IRF151 IRF152 IRF153



N-Channel

100 Volt, 0.055 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

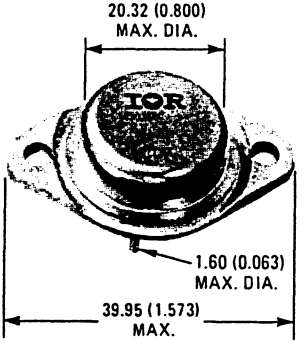
Features:

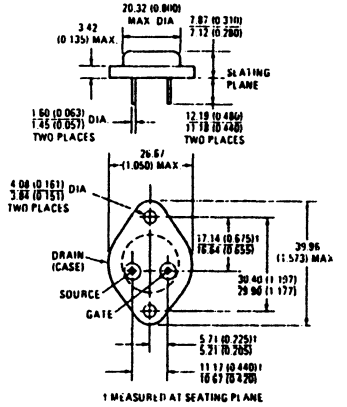
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF150	100V	0.055Ω	40A
IRF151	60V	0.055Ω	40A
IRF152	100V	0.08Ω	33A
IRF153	60V	0.08Ω	33A

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

Figure 9-18 Data sheet for MOSFET type IRF150 (Courtesy of International Rectifier).

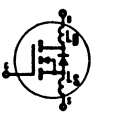
Absolute Maximum Ratings

Parameter		IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		160	160	132	132	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF150 IRF152	100	–	–	V	V_{GS} = 0V
		IRF151 IRF153	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF150 IRF151	40	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF152 IRF153	33	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF150 IRF151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		IRF152 IRF153	–	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 20A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	1000	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	350	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 24V, I_D = 20A, Z_o = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	27	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	36	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Figure 9-18 *Continued*

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF150 IRF151	–	–	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF152 IRF153	–	–	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF150 IRF151	–	–	160	A	
		IRF152 IRF153	–	–	132	A	
V_{SD}	Diode Forward Voltage ②	IRF150 IRF151	–	–	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		IRF152 IRF153	–	–	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.3	–	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

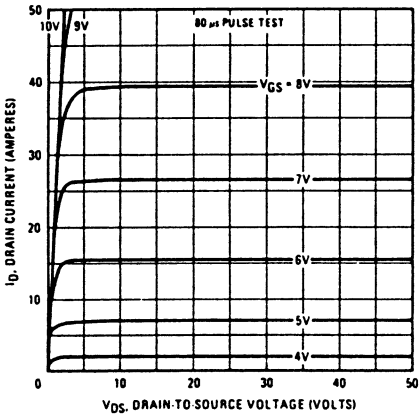


Fig. 1 — Typical Output Characteristics

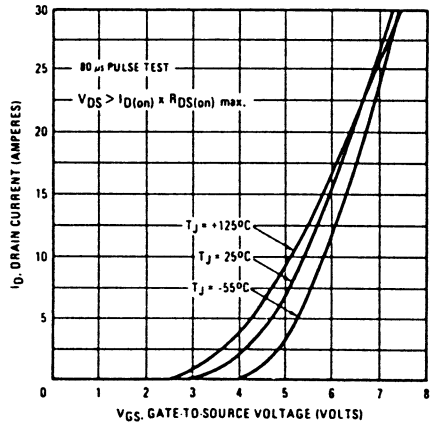


Fig. 2 — Typical Transfer Characteristics

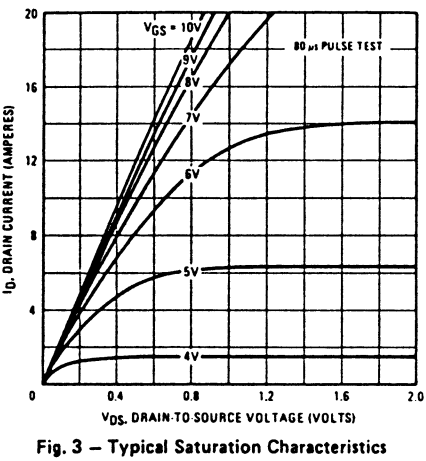


Fig. 3 — Typical Saturation Characteristics

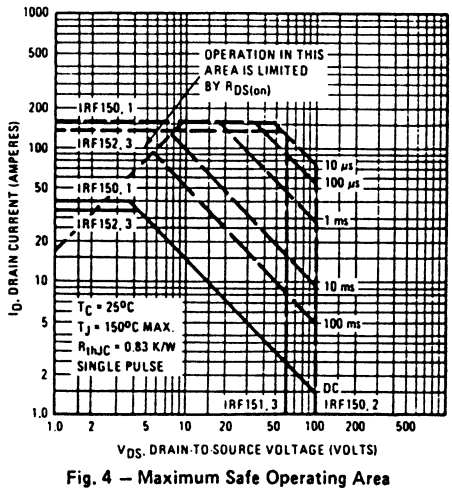


Fig. 4 — Maximum Safe Operating Area

Figure 9-18 *Continued*

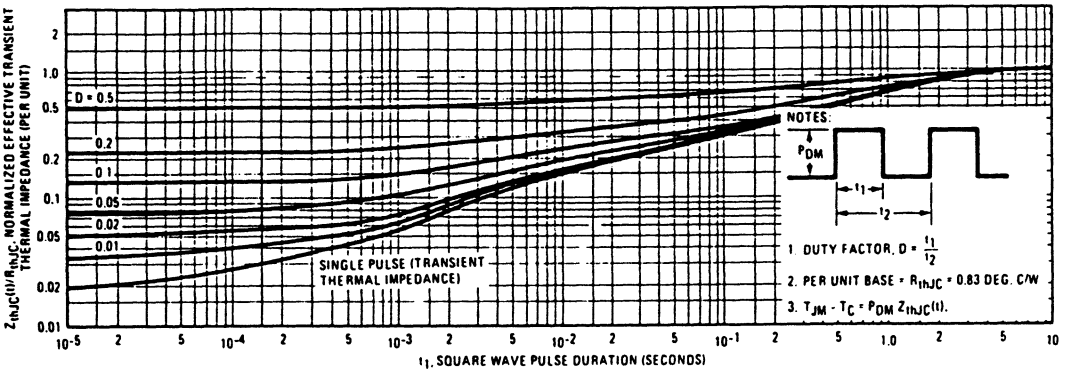


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

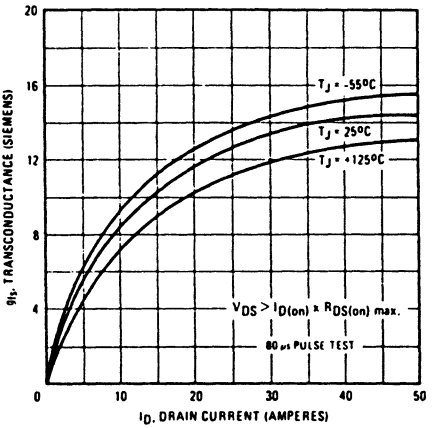


Fig. 6 — Typical Transconductance Vs. Drain Current

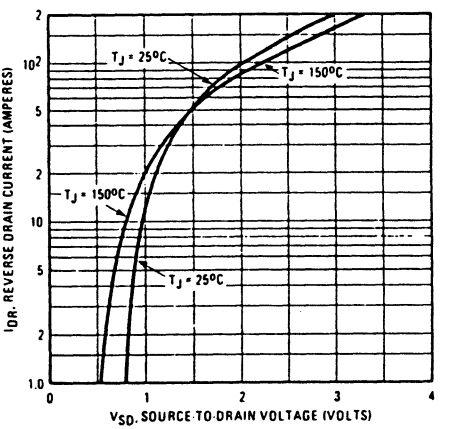


Fig. 7 — Typical Source-Drain Diode Forward Voltage

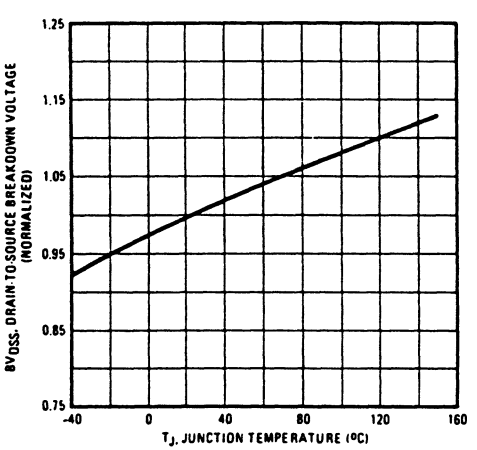


Fig. 8 — Breakdown Voltage Vs. Temperature

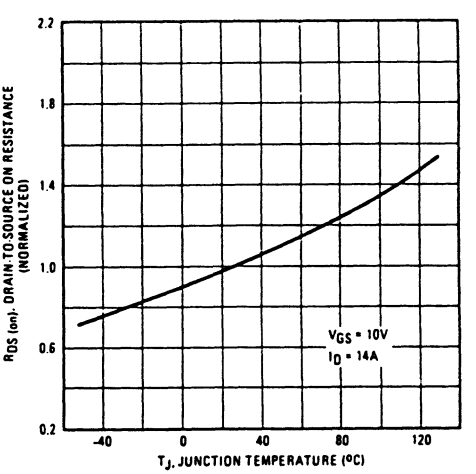


Fig. 9 — Normalized On-Resistance Vs. Temperature

Figure 9-18 *Continued*

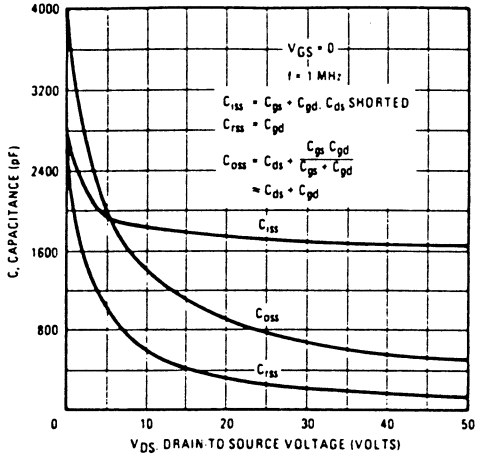


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

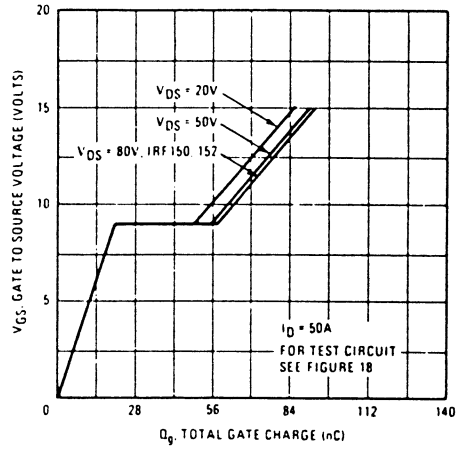


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

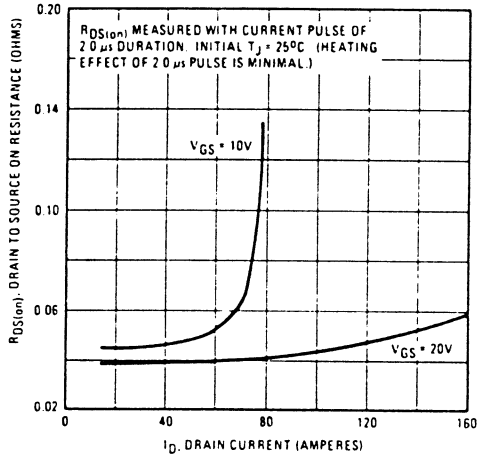


Fig. 12 – Typical On-Resistance Vs. Drain Current

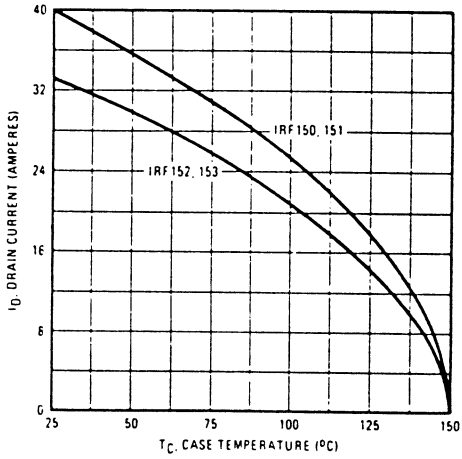


Fig. 13 – Maximum Drain Current Vs. Case Temperature

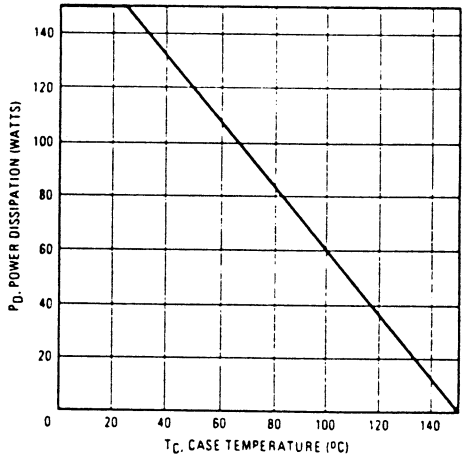


Fig. 14 – Power Vs. Temperature Derating Curve

Figure 9-18 *Continued*

From the data sheet we get $I_{DSS} = 250\ \mu A$ at $V_{GS} = 0$ V, $V_{DS} = 100$ V. $V_{Th} = 2$ to 4 V. Geometric mean, $V_{Th} = VTO = \sqrt{2 \times 4} = 2.83$ V. The constant K_p can be found from

$$I_D = K_p(V_{GS} - V_{Th})^2 \tag{9-3}$$

For $I_D = I_{DSS} = 250\ \mu A$, and $V_{Th} = 2.83$ V, Eq. (9-3) gives $K_p = 250\ \mu A/2.83^2 = 31.2\ \mu A/V^2$. K_p is related to channel length L and channel width W by

$$K_p = \frac{\mu_a C_o}{2}\left(\frac{W}{L}\right) \tag{9-4}$$

where C_o is the capacitance per unit area of the oxide layer, a typical value for a power MOSFET being 3.5×10^{-11} F/cm^2 at a thickness of 0.1 nm (assumed), and μ_a is the surface mobility of electrons, 600 cm^2/(V · s).

The ratio W/L can be found from Eq. (9-4),

$$\frac{W}{L} = \frac{2K_p}{\mu_a C_o} = \frac{2 \times 31.2 \times 10^{-6}}{600 \times 3.5 \times 10^{-11}} = 3000$$

Let $L = 1$ nm and $W = 3\ \mu$m. $C_{rss} = 350 - 500$ pF at $V_{GS} = 0$, $V_{DS} = 25$ V. Geometric mean, $C_{rss} = C_{gd} = \sqrt{350 \times 500} = 418.3$ pF at $V_{DG} = 25$ V.

For a MOSFET, the values of C_{gs} and C_{gd} remain relatively constant with changing V_{GS} or V_{DS}. They are determined mainly by the thickness and type of the insulating oxide. Although, the curves of the capacitances versus drain-source voltage show some variations, we will assume constant capacitances. Thus, $C_{gdo} = 418.3$ pF. $C_{iss} = 2000$ to 3000 pF. Geometric mean $C_{iss} = \sqrt{2000 \times 3000} = 2450$ pF. Since C_{iss} is measured at $V_{GS} = 0$ V, $C_{gs} = C_{gso}$. That is,

$$C_{iss} = C_{gso} + C_{gd}$$

which gives $C_{gso} = C_{iss} - C_{sd} = 2450 - 418.3 = 2032$ pF $= 2.032$ nF. Thus the PSpice model statement for MOSFET IRF150 is

```
.MODEL IRF150 NMOS (VTO=2.83 KP=31.2U L=1N W=3U CGDO=0.418N CGSO=2.032N)
```

The model can be used to plot the characteristics of the MOSFET. It may be necessary to modify the parameter values to conform with the actual characteristics. It should be noted that the parameters would differ from those given in the PSpice library, because their values are dependent on the constants used in derivations. Students are encouraged to run a circuit file with the PSpice library model and compare the results obtained with the above model statement.

9-7 EXAMPLES OF MOSFET AMPLIFIERS

The large number of parameters involved is an indication of the complexity of modeling a MOSFET. An accurate modeling requires a SPICE library file of a MOSFET. The parameters that are determined from the data sheet in Section 9-6

are the approximate values only. If a model parameter is not available, its typical value as indicated in Table 9-2 should be used. The following examples illustrate the PSpice simulation of MOSFET circuits.

Example 9-6

An *n*-channel enhancement-type MOSFET amplifier with series-shunt feedback is shown in Fig. 9-19. Plot the magnitude of output voltage. The frequency is varied from 10 Hz to 100 MHz in decade steps with 10 points per decade. The peak input voltage is 100 mV. The model parameters of the MOSFET are VTO=1, KP=6.5E−3, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF. Print the details of the bias and operating points.

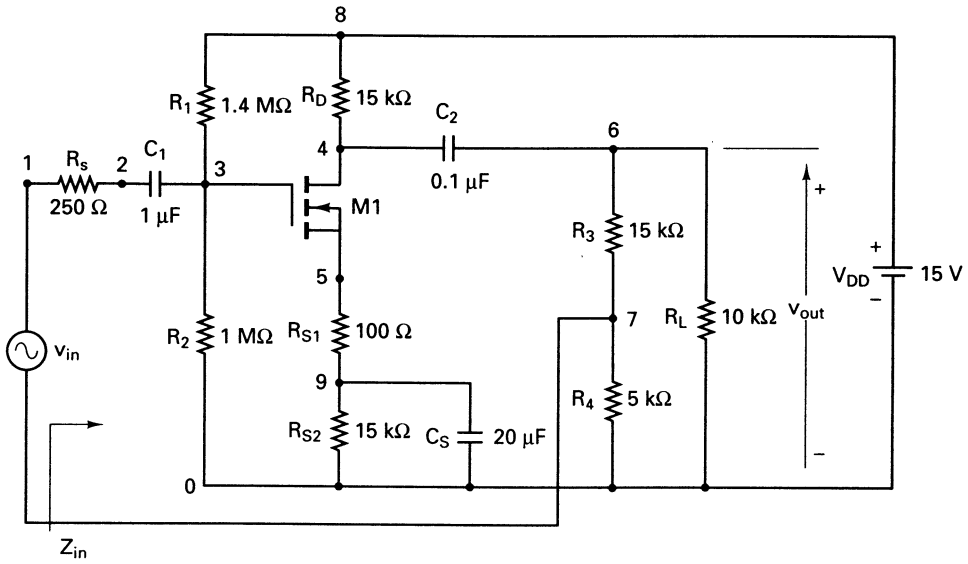


Figure 9-19 A MOSFET feedback amplifier.

Solution The listing of the circuit file follows.

Example 9-6 A MOSFET feedback amplifier

```
▲ *    Input voltage of 100 mV peak for frequency response
  VIN  1  7  AC  100mV
  VDD  8  0  15V
▲▲ RS   1  2  250
   C1   2  3  1UF
   R1   8  3  1.4MEG
   R2   3  0  1MEG
   RD   8  4  15K
   RS1  5  9  100
   RS2  9  0  15K
   CS   9  0  20UF
   C2   4  6  0.1UF
   R3   6  7  15K
```

```
    R4    7   0   5K
    RL    6   0   10K
    *     MOSFET M1 with model MQ is connected to 4 (drain), 3 (gate), 5
    *     (source) and 5 (substrate).
    M1 4   3   5   5   MQ
    *      Model for MQ
    .MODEL MQ NMOS (VTO=1 KP=6.5E-3 CBD=5PF CBS=2PF RD=5 RS=2 RB=0
    +     RG=0 RDS=1MEG CGS0=1PF CGD0=1PF CGB0=1PF)
▲▲▲ *     Ac analysis for 10 Hz to 100 MHz with a decade increment and 10
      *     points per decade
      .AC   DEC   10   10HZ   100MEGHZ
      *     Plot the results of ac analysis: voltage at node 6.
      .PLOT   AC   VM(6)
      *     Print the details of the dc operating point.
      .OP
      .PROBE
.END
```

The details of the bias and operating points are given next.

```
 ****      SMALL-SIGNAL BIAS SOLUTION                TEMPERATURE =  27.000 DEG C
 NODE      VOLTAGE      NODE      VOLTAGE      NODE      VOLTAGE      NODE      VOLTAGE
(   1)     0.0000      (   2)     0.0000      (   3)     6.2500      (   4)     10.1000
(   5)     4.9323      (   6)     0.0000      (   7)     0.0000      (   8)     15.0000
(   9)     4.8997
    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT
    VIN           0.000E+00
    VDD          -3.329E-04
    TOTAL POWER DISSIPATION  4.99E-03  WATTS

 ****      OPERATING POINT INFORMATION               TEMPERATURE =  27.000 DEG C
**** MOSFETS
NAME          M1
MODEL         MQ
ID            3.32E-04
VGS           1.32E+00
VDS           5.17E+00
VBS           0.00E+00
VTH           1.00E+00
VDSAT         3.17E-01
GM            2.06E-03
GDS           1.00E-06
GMB           0.00E+00
CBD           1.83E-12
CBS           2.00E-12
CGSOV         1.00E-16
CGDOV         1.00E-16
CGBOV         1.00E-16
```

```
CGS          0.00E+00
CGD          0.00E+00
CGB          0.00E+00
        JOB CONCLUDED
        TOTAL JOB TIME          17.41
```

The frequency response for Example 9-6 is shown in Fig. 9-20. If the .PROBE command is included, there is no need for the .PLOT command.

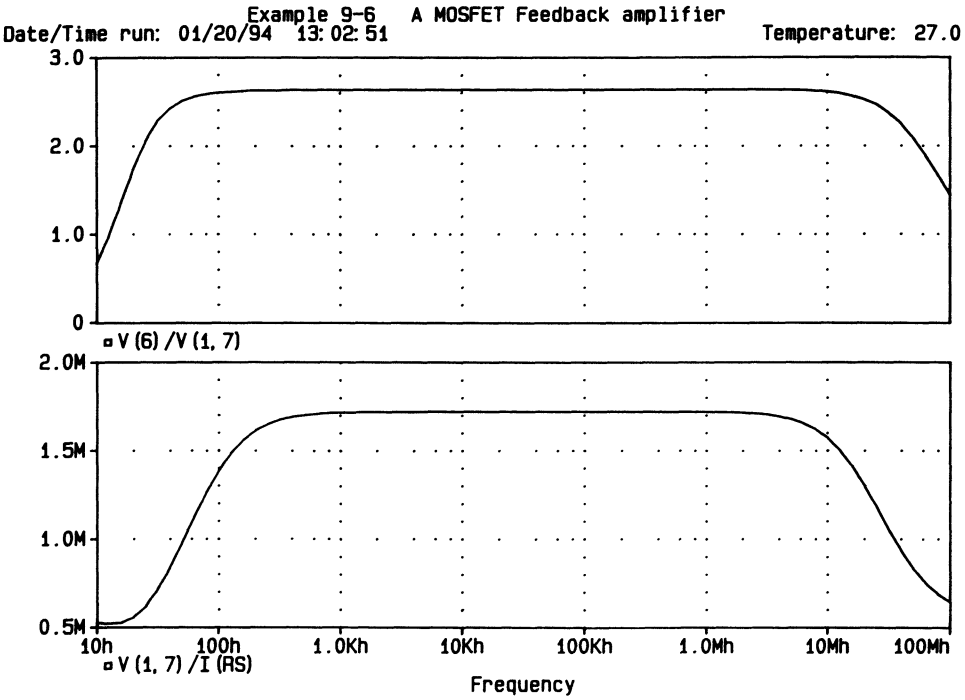


Figure 9-20 Frequency response for Example 9-6.

Example 9-7

For Fig. 9-19, plot the magnitude response of output impedance. The frequency is varied from 10 Hz to 100 MHz in decade steps with 10 points per decade.

Solution The output impedance of the MOSFET feedback amplifier in Fig. 9-19 can be determined by short-circuiting the input source and connecting a test current source between terminals 0 and 6, as shown in Fig. 9-21. Let the peak value of the test current be 1 mA. The voltage at node 6 is a measure of the output impedance: Z_{out} = V(6)/1 mA = V(6) kΩ.

The listing of the circuit file follows.

Example 9-7 Output impedance of a MOSFET feedback amplifier

```
* Input source VIN is shorted.
VIN  1  9  AC  0V
*  Test current of 1 mA peak for frequency response
```

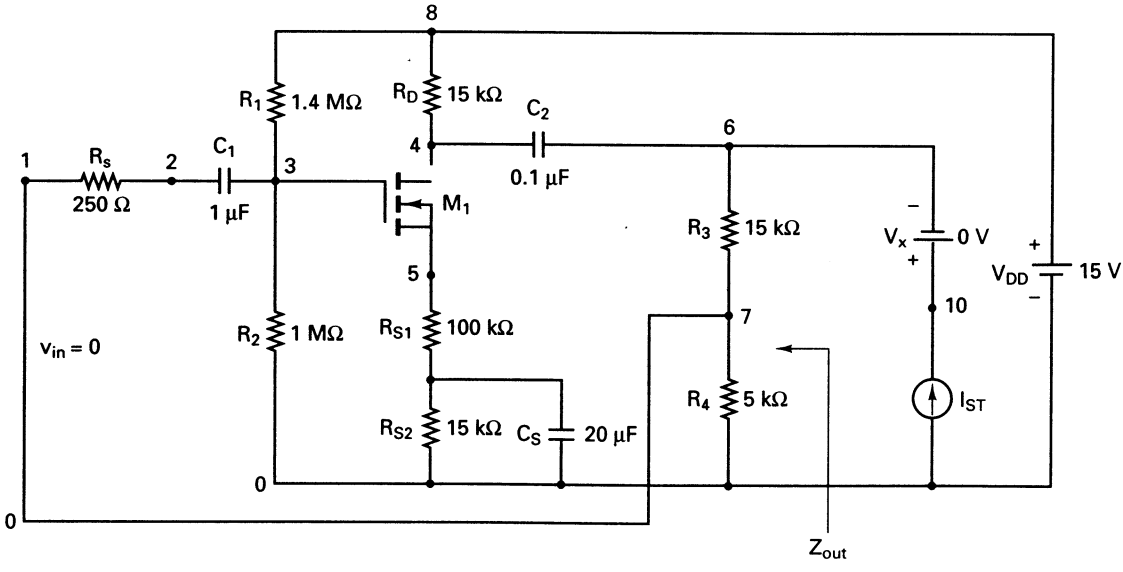


Figure 9-21 Equivalent circuit for output impedance calculation (Example 9-7).

```
IST  0  10  AC  1MA
*  A dummy source of 0 V dc
VX   10  6  DC 0V
VDD  8   0  15V
RS   1   2  250
C1   2   3  1UF
R1   8   3  1.4MEG
R2   3   0  1MEG
RD   8   4  15K
RS1  5   9  100
RS2  9   0  15K
CS   9   0  20UF
C2   4   6  0.1UF
R3   6   7  15K
R4   7   0  5K
RL   6   0  10K
*    M1 with model MQ, whose substrate is connected to node 5
M1 4  3  5  5  MQ
*    Model for n-channel MOSFET with model name MQ
.MODEL MQ NMOS (VTO=1 KP=6.5E-3 CBD=5PF CBS=2PF RD=5 RS=2 RB=0
+   RG=0 RDS=1MEG CGSO=1PF CGDO=1PF CGBO=1PF)
*    Ac analysis for 10 Hz to 100 MHz with a decade increment and 10
*    points per decade
.AC  DEC  10  10HZ  10MEGHZ
*    Plot the results of the ac analysis: voltage at node 6.
.PLOT  AC  VM(6)
.PROBE
.END
```

The frequency response of the output impedance for Example 9-7 is shown in Fig. 9-22. If the .PROBE command is included, there is no need for the .PLOT command.

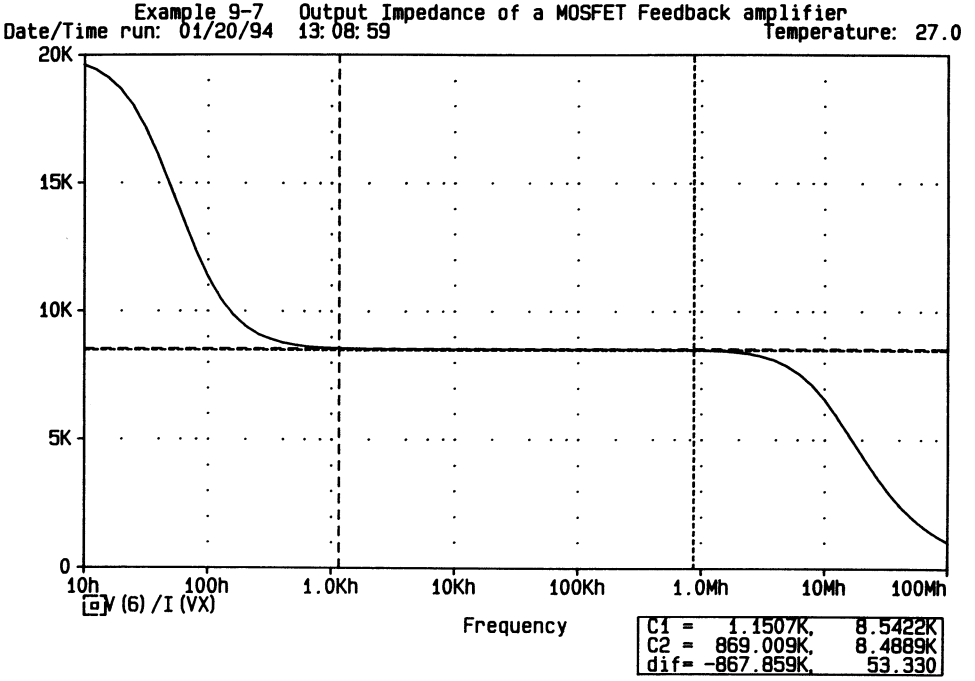


Figure 9-22 Output impedance for Example 9-7.

Example 9-8

A CMOS inverter circuit is shown in Fig. 9-23(a). The output is taken from node 3. The input voltage is shown in Fig. 9-23(b). Plot the transient response of the output voltage from 0 to 80 μs in steps of 2 μs. If the input voltage is 5 V, calculate

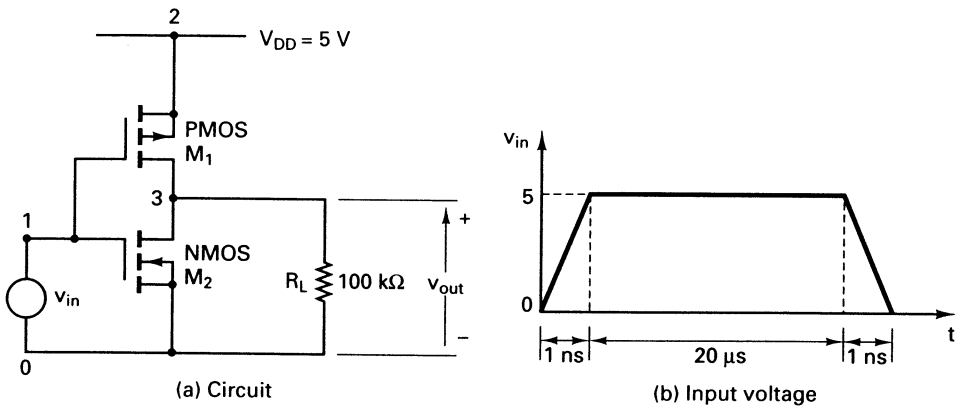


Figure 9-23 A CMOS inverter (Example 9-8).

the voltage gain, the input resistance, and the output resistance. Print the small-signal parameters of the MOS and NMOS. The model parameters of the PMOS are L=1U, W=20U, VTO=−2, KP=4.5E−4, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF. The model parameters of the NMOS are L=1U, W=5U, VTO=2, KP=4.5E−5, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF.

Solution The listing of the circuit file follows.

Example 9-8 A CMOS inverter

```
▲ VDD  2  0  5V
  *  The input voltage is 5 V for dc analysis and pulse waveform for
  *  transient analysis.
  VIN  1  0  DC  5V  PULSE (0  5V  0  1NS  1NS  20US 40US)
▲▲ RL   3  0  100K
   *   PMOS with model PMOD
   M1   3  1  2  2  PMOD  L=1U  W=20U
   .MODEL PMOD PMOS (VTO=-2 KP=4.5E-4 CBD=5PF CBS=2PF RD=5 RS=2 RB=0
   +  RG=0 RDS=1MEG CGSO=1PF CGDO=1PF CGBO=1PF)
   M2   3  1  0  0  NMOD  L=1U  W=5U
   *   NMOS with model NMOD
   .MODEL NMOD NMOS (VTO=2 KP=4.5E-5 CBD=5PF CBS=2PF RD=5 RS=2 RB=0
   +  RG=0 RDS=1MEG CGSO=1PF CGDO=1PF CGBO=1PF)
   *  Transient analysis from 0 to 80μs in steps of 1 μs
▲▲▲ .TRAN   1US  80US
     *  Transfer-function analysis
     .TF  V(3)  VIN
     *  Print details of operating points.
     .OP
     .PLOT TRAN  V(3)  V(1)
     .PROBE
.END
```

```
 ****      OPERATING POINT INFORMATION              TEMPERATURE =  27.000 DEG C
**** MOSFETS
NAME          M1          M2
MODEL         MQ          NMOD
ID         -5.00E-06   1.53E-11
VGS         0.00E+00   5.00E+00
VDS        -5.00E+00   2.27E-08
VBS         0.00E+00   0.00E+00
VTH        -2.00E+00   2.00E+00
VDSAT       0.00E-00   3.00E+00
GM          0.00E-00   5.09E-12
GDS         1.00E-06   6.76E-04
GMB         0.00E+00   0.00E+00
CBD         1.86E-12   5.00E-12
CBS         2.00E-12   2.00E-12
CGSOV       2.00E-17   5.00E-18
CGDOV       2.00E-17   5.00E-18
```

```
CGBOV          1.00E-18    1.00E-18
CGS            0.00E+00    0.00E+00
CGD            0.00E+00    0.00E+00
CGB            0.00E+00    0.00E+00

****      SMALL-SIGNAL CHARACTERISTICS
     V(3)/VIN = -7.422E-09
     INPUT RESISTANCE AT VIN = 1.000E+20
     OUTPUT RESISTANCE AT V(3) = 1.462E+03
         JOB CONCLUDED
         TOTAL JOB TIME            48.33
```

The frequency response for Example 9-8 is shown in Fig. 9-24. If the .PROBE command is included, there is no need for the .PLOT command. The .OPTIONS statement is essential to avoid convergence problems, and it is often necessary to adjust the .OPTIONS parameters (e.g., ABSTOL, RELTOL, and VNTOL) in order to let the simulation converge.

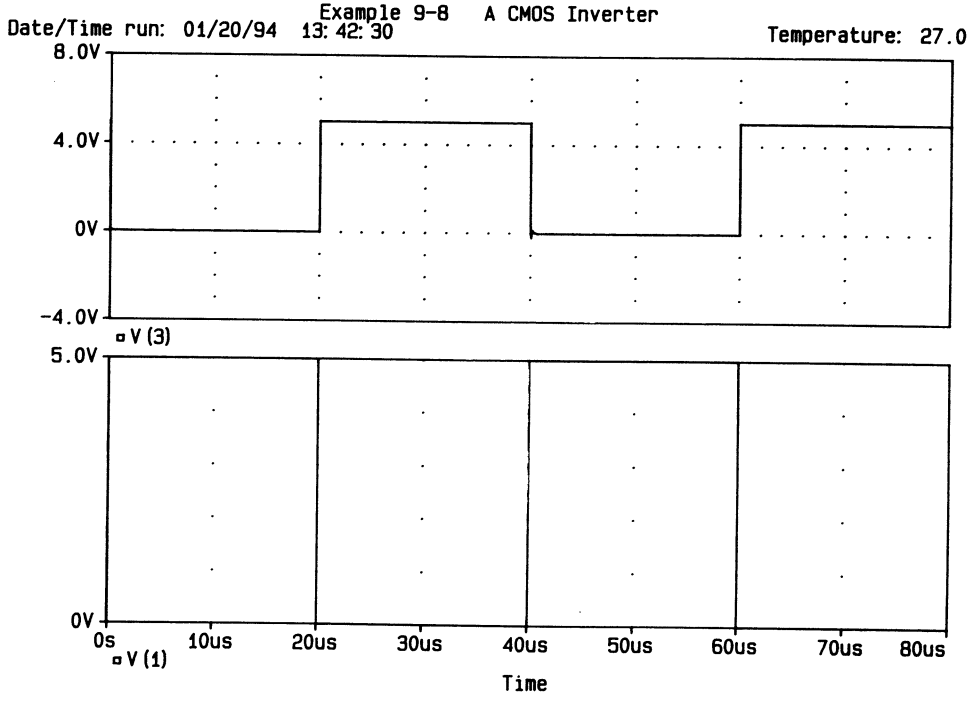


Figure 9-24 Frequency response for Example 9-8.

9-8 GALLIUM ARSENIDE MESFETs

The PSpice model of an *n*-channel GaAsFET (gallium arsenide FET) is shown in Fig. 9-25 [5, 6]. The small-signal model, which is generated by PSpice, is shown in Fig. 9-26. The model parameters for a GaAsFET device and the default values

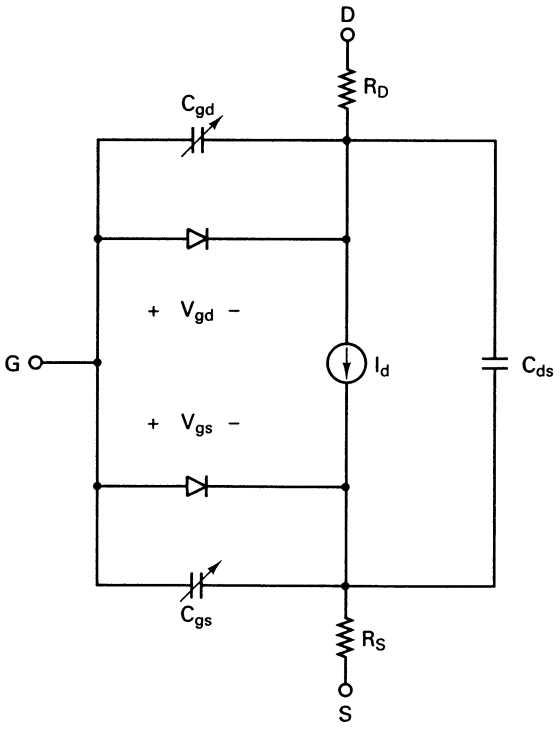


Figure 9-25 PSpice *n*-channel GaAsFET model.

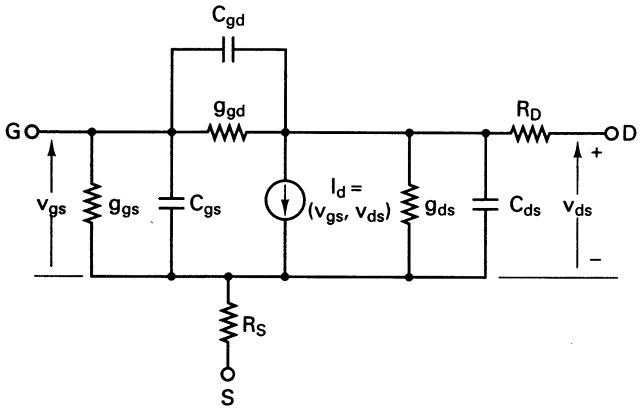


Figure 9-26 Small-signal *n*-channel GaAsFET model.

assigned by PSpice are listed in Table 9-3. The model equations of GaAsFETs that are used by PSpice are described in Curtice [5], Sussman-Fort et al. [6], and the *PSpice Manual* [7].

The model statement of *n*-channel GaAsFETs has the general form

```
.MODEL  BNAME  GASFET (P1=A1  P2=A2  P3=A3 ... PN=AN)
```

where GASFET is the type symbol of *n*-channel GaAsFETs. BNAME is the model name. It can begin with any character and its word size is normally limited

TABLE 9-3 MODEL PARAMETERS OF GaAs MESFETs

Name	Area	Model parameters	Units	Default	Typical
VTO		Threshold voltage	Volts	−2.5	−2.0
ALPHA		Tan *h* constant	$Volts^{-1}$	2.0	1.5
BETA		Transconductance coefficient	$Amps/Volts^2$	0.1	25U
LAMBDA		Channel-length modulation	Volts	0	1E−10
RG	*	Gate ohmic resistance	Ohms	0	1
RD	*	Drain ohmic resistance	Ohms	0	1
RS	*	Source ohmic resistance	Ohms	0	1
IS		Gate *p-n* saturation current	Amps	1E−14	
M		Gate *p-n* grading coefficient		0.5	
N		Gate *p-n* emission coefficient		1	
VBI		Threshold voltage	Volts	1	0.5
CGD		Gate-drain zero-bias *p-n* capacitance	Farads	0	1FF
CGS		Gate-source zero-bias *p-n* capacitance	Farads	0	6FF
CDS		Drain-source capacitance	Farads	0	0.3FF
TAU		Transit time	seconds	0	10PS
FC		Forward-bias depletion capacitance coefficient		0.5	
VTOTC		VTO temperature coefficient	Volts/°C	0	
BETATCE		BETA exponent temperature coefficient	%/°C	0	
KF		Flicker noise coefficient		0	
AF		Flicker noise exponent		1	

to eight characters. P1, P2, . . . and A1, A2, . . . are the parameters and their values, respectively.

RD, RS, and RG represent the contact and bulk resistances per unit area of the drain, source, and gate, respectively. The GaAsFET is modeled as an intrinsic device. The area value, which is the relative device area, is specified in the .MODEL statement and changes the actual resistance values. The default value of the area is 1.

The symbol for a gallium arsenide MESFET (GaAs MESFET or GaAsFET) is *B*. The name of a GaAs MESFET must start with *B*, and it takes the general form

```
B(name) ND  NG  NS  BNAME  [(area) value]
```

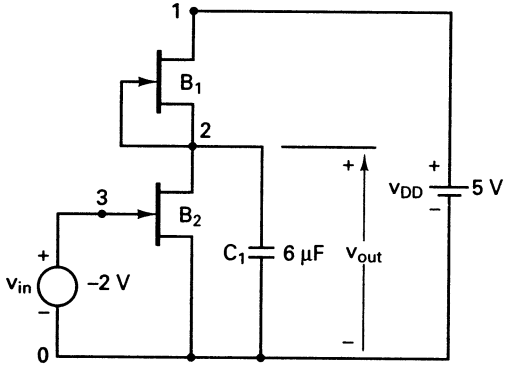
where ND, NG, ND are the drain, gate, and source nodes, respectively. BNAME, which is the model name, can begin with any character, and its word size is normally limited to eight characters. Positive current flows into a terminal.

Some GaAs MESFET Statements

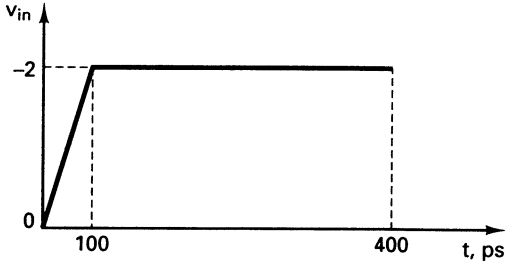
```
BIX  2  5  7  NMOD
.MODEL NMOD GASFET
BIM 15  1  0  GMOD
.MODEL GMOD GASFET (VTO=-2.5 BETA=60U VBI=0.5 ALPHA=1.5 TAU=10PS)
B5  7  9  3   NMOM 1.5
.MODEL MNOM GASFET (VTO=-2.5 BETA=32U VBI=0.5 ALPHA=1.5)
```

Example 9-9

A GaAsFET inverter with active load is shown in Fig. 9-27(a). The input voltage is a pulse waveform, as shown in Fig. 9-27(b). Plot the transient response of the output voltage for a time duration of 240 ps in steps of 2 ps. Plot the dc transfer characteristic if the input voltage is varied from −2.5 V to 1 V in steps of 0.1 V. The model parameters of the GaAsFET are VTO=−2, BETA=60U, VBI=0.5, ALPHA=1.5, and TAU=10PS, and those of B2 are VTO=−2, BETA=3U, VBI=0.5, and ALPHA=1.5. Calculate the dc voltage gain, the input resistance, and the output resistance. Print the small-signal parameters for the dc analysis.



(a) Circuit



(b) Input voltage

Figure 9-27 GaAsFET inverter with active load.

Solution The listing of the circuit file follows.

Example 9-9 A GaAsFET inverter with active load

```
▲ VDD  1  0  5V
  *   Pulsed input voltage
  VIN  3  0  DC  -2V  PWL (0  0  100PS -2V  1NS -2V)
▲▲ *   GaAsFET, which is connected to 1 (drain), 2 (gate) and
   *   2 (source), has a model of GF1.
   B1   1  2  2  GF1
   B2   2  4  0  GF2
   C1   2  0  6F  IC=0V
   RS   3  4   50
   *    Model for GF1
   .MODEL GF1 GASFET (VTO=-2.5 BETA=65U VBI=0.5 ALPHA=1.5 TAU=10PS)
   .MODEL GF2 GASFET (VTO=-2.5 BETA=32.5U VBI=0.5 ALPHA=1.5)
▲▲▲ *   Transient analysis for 0 to 240 ps with 2-ps increment
     .TRAN  2PS  240PS  UIC
     .DC VIN  -2.5  1  0.1
     *   Plot the results of transient analysis.
     .PLOT TRAN  V(3)  V(2)
     .PLOT  DC  V(2)
     *   Dc transfer characteristics
     .TF   V(2)  VIN
```

```
*     Small-signal parameters for dc analysis
.OP
.PROBE
.END
```

```
****     SMALL-SIGNAL BIAS SOLUTION                TEMPERATURE =  27.000 DEG C
NODE     VOLTAGE     NODE     VOLTAGE     NODE     VOLTAGE     NODE     VOLTAGE
(   1)    5.0000     (   2)    4.8787     (   3)   -1.0000     (   4)   -1.0000

    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT
    VDD          -7.313E-05
    VIN           6.899E-12
    TOTAL POWER DISSIPATION  3.66E-04  WATTS
```

```
****     OPERATING POINT INFORMATION               TEMPERATURE =  27.000 DEG C
**** GASFETS
NAME          B1          B2
MODEL         GF1         GF2
ID            7.31E-05    7.31E-05
VGS           0.00E+00   -1.00E+00
VDS           1.21E-01    4.88E+00
GM            5.85E-05    9.75E-05
```

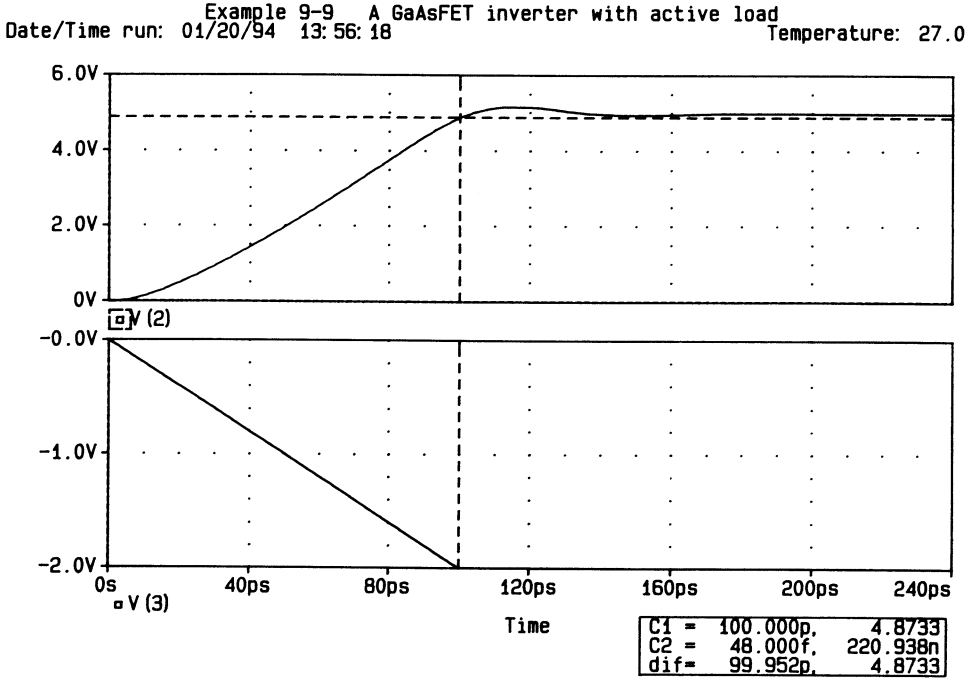


Figure 9-28 Transient response for Example 9-9.

```
GDS          5.90E-04     1.93E-10
CGS          0.00E+00     0.00E+00
CGD          0.00E+00     0.00E+00
CDS          0.00E+00     0.00E+00

****     SMALL-SIGNAL CHARACTERISTICS
     V(2)/VIN = -1.654E-01
     INPUT RESISTANCE AT VIN = 4.618E+11
     OUTPUT RESISTANCE AT V(2) = 1.696E+03
```

The transient response and the dc transfer characteristics for Example 9-9 are shown in Fig. 9-28. If the .PROBE command is included, there is no need for the .PLOT command.

SUMMARY

The model statements for FETs can be summarized as follows:

```
B⟨name⟩ ND  NG   NS  BNAME  [(area) value]
.MODEL  BNAME   GASFET (P1=V1 P2=V2 P3=V3 ...PN=VN)
J⟨name⟩ ND  NG   NS  JNAME [(area) value]
.MODEL  JNAME   NJF  (P1=V1 P2=V2 P3=V3 ...PN=VN)
.MODEL  JNAME   PJF  (P1=V1 P2=V2 P3=V3 ...PN=VN)
N⟨name⟩ ND  NG  NS   NB  MNAME
+       [L=⟨value⟩]  [W=⟨value⟩]
+       [AD=⟨value⟩]  [AS=⟨value⟩]
+       [PD=⟨value⟩]  [PS=⟨value⟩]
+       [NRD=⟨value⟩]  [NRS=⟨value⟩]
+       [NRG=⟨value⟩]  [NRB=⟨value⟩]
.MODEL  MNAME  NMOS (P1=V1 P2=V2 P3=V3 ...PN=VN)
.MODEL  MNAME  PMOS (P1=V1 P2=V2 P3=V3 ...PN=VN)
```

REFERENCES

1. H. Schichman and D. A. Hodges, "Modeling and simulation of insulated gate field effect transistor switching circuits," *IEEE Journal of Solid-State Circuits,* Vol. SC-3, September 1968, pp. 285–289.
2. J. F. Meyer, "MOS models and circuit simulation," *RCA Review,* Vol. 32, March 1971, pp. 42–63.
3. A. Vladimirescu and Sally Liu, *The simulation of MOS integrated circuits using SPICE2,* Memorandum no. M80/7, February 1980, University of California, Berkeley.
4. L. M. Dang, "A simple current model for short channel IGFET and its application to circuit simulation," *IEEE Journal of Solid-State Circuits,* Vol. SC-14, No. 2, 1979, pp. 358–367.

5. W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Transactions on Microwave Theory and Techniques,* Vol. MTT-23, May 1980, pp. 448–456.
6. S. E. Sussman-Fort, S. Narasimhan, and K. Mayaram, "A complete GaAs MESFET computer model for SPICE," *IEEE Transactions on Microwave Theory and Techniques,* Vol. MTT-32, April 1984, pp. 471–473.
7. *PSpice Manual.* Irvine, Calif.: MicroSim Corporation, 1992.
8. S. Natarajan, "An effective approach to obtain model parameters for BJTs and FETs from data books," *IEEE Transactions on Education,* Vol. 35, No. 2, 1992, pp. 164–169.
9. M. H. Rashid, *SPICE for Power Electronics and Electric Power.* Englewood Cliffs, N.J.: Prentice Hall, 1993.

PROBLEMS

9-1. For the amplifier circuit in Fig. 6-8, calculate and plot the frequency responses of the output voltage and the input current. The frequency is varied from 10 Hz to 10 MHz in decade steps with 10 points per decade.

9-2. A shunt-shunt feedback is applied to the amplifier circuit in Fig. 9-8. This is shown in Fig. P9-2. Calculate and print the frequency responses of the output voltage and the input current. The frequency is varied from 10 Hz to 10 MHz in decade steps with 10 points per decade. The model parameters are IS=1N, VTO=−4, BETA=0.5M, CGDO=5.85P, CGSO=3.49P, and LAMBDA=2.395E−3.

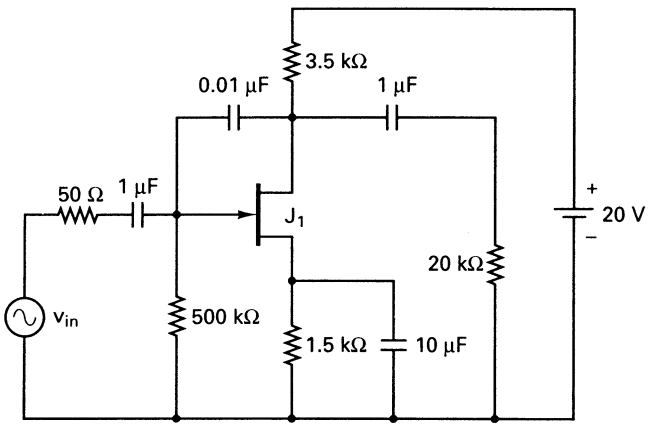


Figure P9-2

9-3. Repeat Example 9-5 if the transistor is an *n*-channel JFET. The model parameters are IS=100E−14, RD=10, RS=10, BETA=1E−3, and VTO=−2. Assume $R_{S2} = 0$.

9-4. For the *n*-channel enhancement-type MOSFET in Fig. P9-4, plot the output characteristics if V_{DS} is varied from 0 to 15 V in steps of 0.1 V and V_{GS} is varied from 0 to 6 V in steps of 1 V. The model parameters are L=10U, W=20U, VTO=2.5, KP=6.5E−3, RD=5, RS=2, RB=0, RG=0, and RDS=1MEG.

9-5. For Problem 9-4, plot the input characteristics if V_{GS} is varied from 0 to 6 V in steps of 0.1 V and V_{DS} = 15 V.

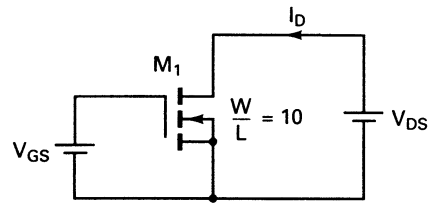


Figure P9-4

9-6. An inverter circuit is shown in Fig. P9-6. For the input voltage as shown in Fig. 9-23(b), plot the transient response of the output voltage from 0 to 80 μs in steps of 2 μs. If the input voltage is 5 V dc, calculate the voltage gain, the input resistance, and the output resistance. Print the small-signal parameters of the PMOS. The model parameters of the PMOS are VTO=−2.5, KP=4.5E−3, CBD=5PF, CBS=2PF, CGSO=1PF, CGDO=1PF, and CGBO=1PF.

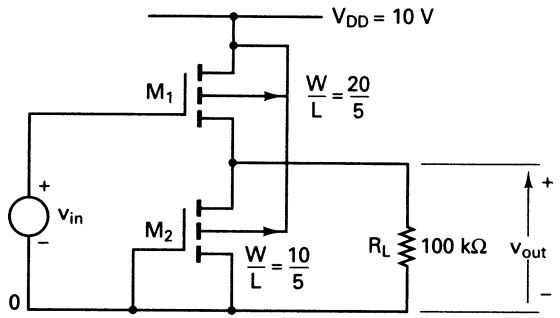


Figure P9-6

9-7. For the NMOS AND-logic circuit in Fig. P9-7, plot the transient response of the output voltage from 0 to 100 μs in steps of 1 μs. The model parameters of the *p*-channel depletion-type MOSFETs are VTO=2, KP=4.5E−3, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF.

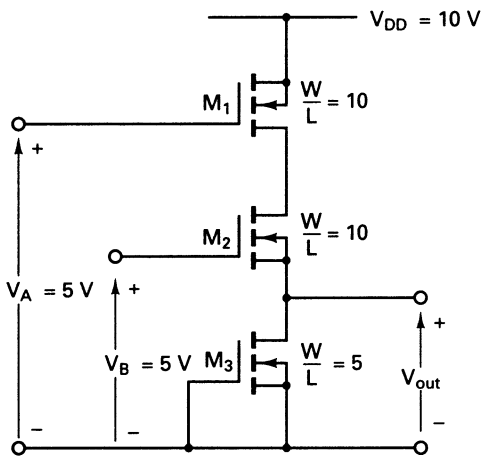


Figure P9-7

9-8. For the NMOS NAND-logic gate circuit in Fig. P9-8, plot the transient response of the output voltage from 0 to 100 μs in steps of 1 μs. The model parameters of the PMOS are VTO=−2.5, KP=4.5E−3, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF. The model parameters of the NMOS are VTO=2.5, KP=4.5E−3, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF.

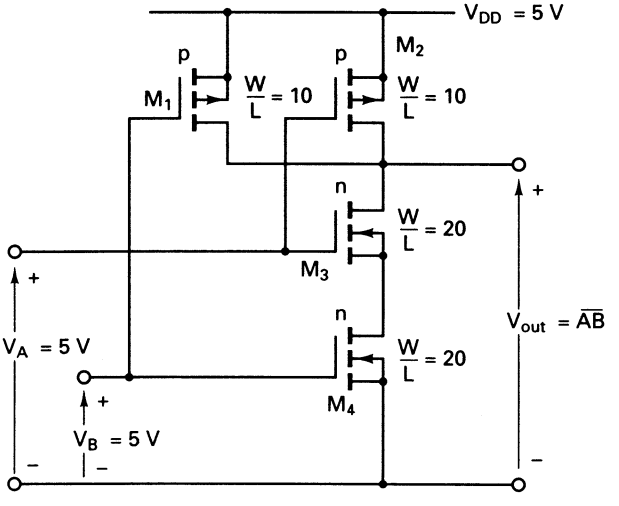


Figure P9-8

9-9. A MOSFET amplifier with active load is shown in Fig. P9-9. Plot the magnitudes of the output voltage and the input current. The frequency is varied from 10 Hz to 100 MHz with a decade increment and 10 points per decade. The peak input voltage is 200 mV. The model parameters of the NMOS are VTO=2.5, KP=4.5E−2, CBD=5PF, CBS=2PF, RD=5, RS=2, RB=0, RG=0, RDS=1MEG, CGSO=1PF, CGDO=1PF, and CGBO=1PF. Print the details of the bias point and the small-signal parameters of the NMOS.

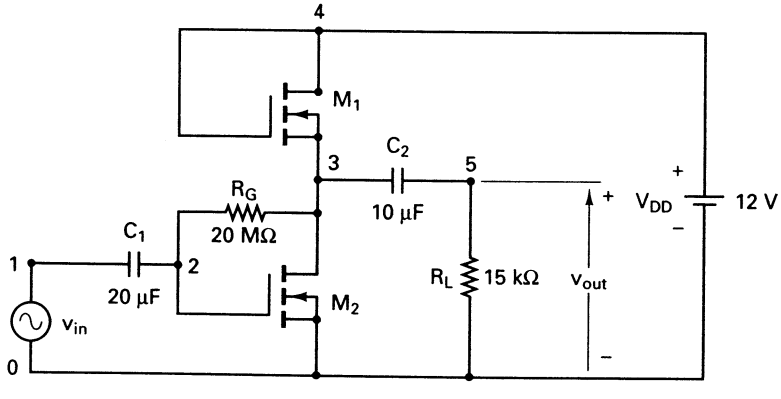


Figure P9-9

9-10. Use PSpice to perform a Monte Carlo analysis for six runs and for the frequency of Problem 9-2. The model parameter is $R=1$ for resistors. The lot deviation for all resistances is $\pm 15\%$. The transistor parameter having uniform deviations is

$$\text{VTO} = -4 \pm 1.5$$

(a) The greatest difference from the nominal run is to be printed.
(b) The maximum value of the output voltage is to be printed.
(c) The minimum value of the output voltage is to be printed.

9-11. Use PSpice to perform the worst-case analysis for Problem 9-10.

9-12. Use PSpice to perform a Monte Carlo analysis for six runs and for the transient response of Problem 9-6. The transistor parameter having uniform deviations is

$$\text{VTO} = -2.5\text{V} \pm 1.2\text{V}$$

(a) The greatest difference from the nominal run is to be printed.
(b) The maximum value of the output voltage is to be printed.
(c) The minimum value of the output voltage is to be printed.

9-13. Use PSpice to perform the worst-case analysis for Problem 9-12.

9-14. Use PSpice to perform a Monte Carlo analysis for five runs and for the transient response of Problem 9-7. The transistor parameter having uniform deviations is

$$\text{VTO} = 2\text{V} \pm 1.5\text{V}$$

(a) The greatest difference from the nominal run is to be printed.
(b) The maximum value of the output voltage is to be printed.
(c) The minimum value of the output voltage is to be printed.

9-15. Use PSpice to perform the worst-case analysis for Problem 9-14.

9-16. Use PSpice to perform a Monte Carlo analysis for five runs and for the transient response of Problem 9-8. The transistor parameter having uniform deviations is

$$\text{VTO} = -2.5\text{V} \pm 1.5\text{V}$$

(a) The greatest difference from the nominal run is to be printed.
(b) The maximum value of the output voltage is to be printed.
(c) The minimum value of the output voltage is to be printed.

9-17. Use PSpice to perform the worst-case analysis for Problem 9-16.

9-18. Use PSpice to perform a Monte Carlo analysis for five runs and for the frequency response of Problem 9-9. The transistor parameter having uniform deviations is

$$\text{VTO} = 2.5\text{V} \pm 1.5\text{V}$$

(a) The greatest difference from the nominal run is to be printed.
(b) The maximum value of the output voltage is to be printed.
(c) The minimum value of the output voltage is to be printed.

9-19. Use PSpice to perform the worst-case analysis for Problem 9-18.