# Chapter 5 Field Effect Transistors (FET)

most common

enhancement mode metal-oxide-semiconductor (MOS FET)

other types

depletion mode metal-oxide-semiconductor (also MOSFET)

junction field effect transistor (JFET)

MOSFET's

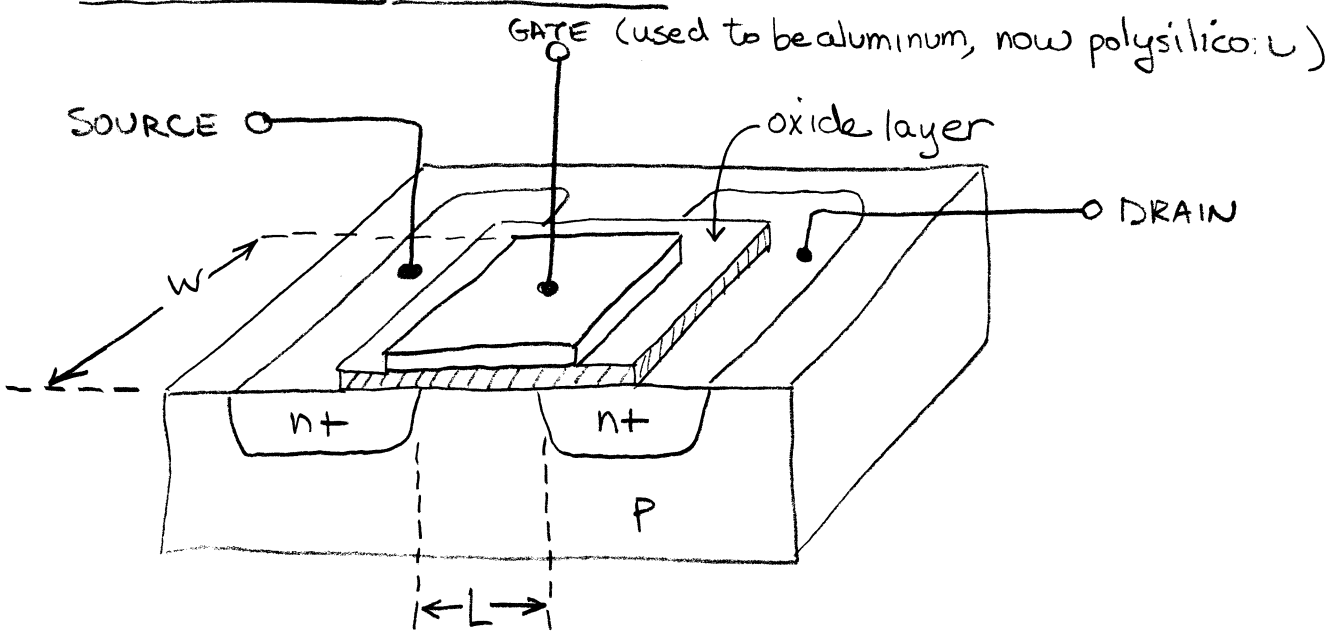
smaller size

fewer processing steps

BJT's

larger currents

## Basic structure of a MOSFET



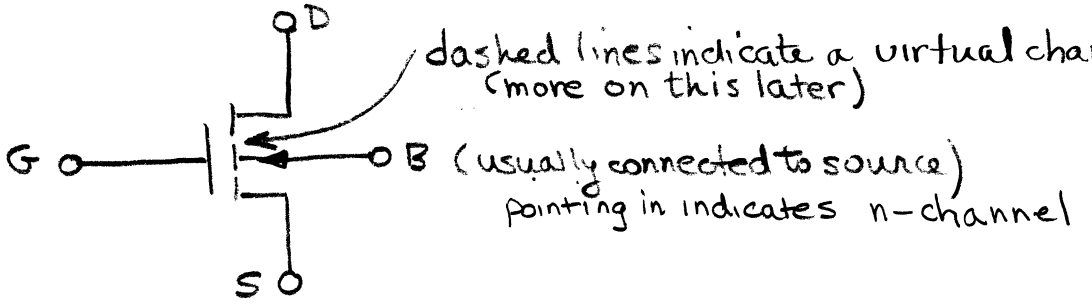

L, W define the area of the gate

$0.2 \leq L \leq 10\,\mu m$ $0.5 \leq W \leq 500\,\mu m$

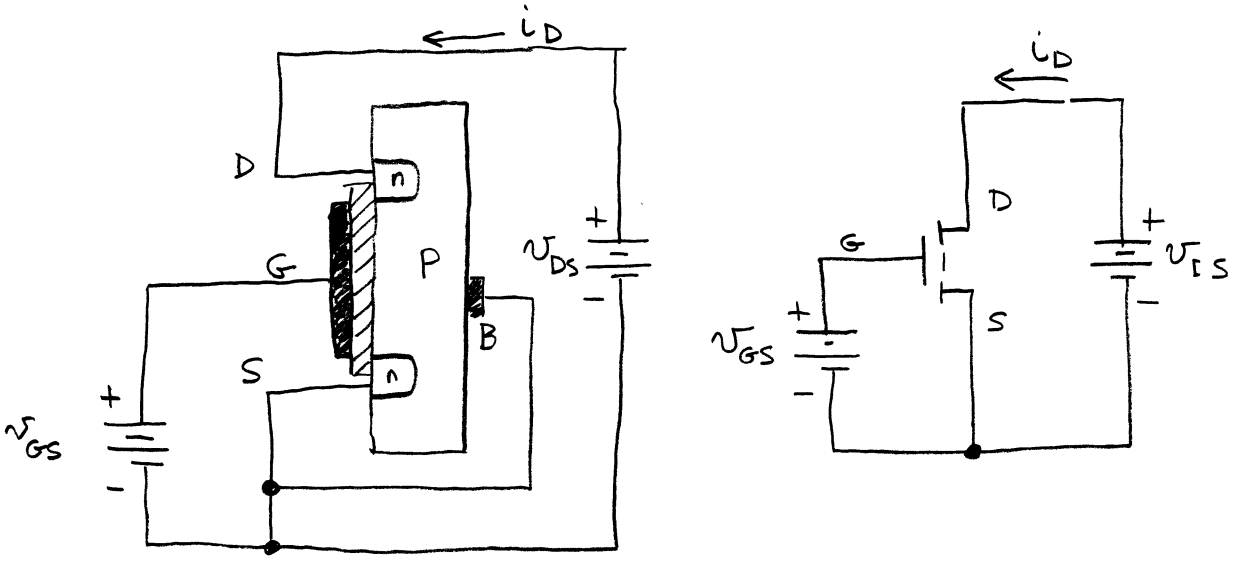
silicon oxide layer 0.05 – 0.1 μm thick

IC designer can adjust L, W

Circuit symbol




Operation in the cutoff region

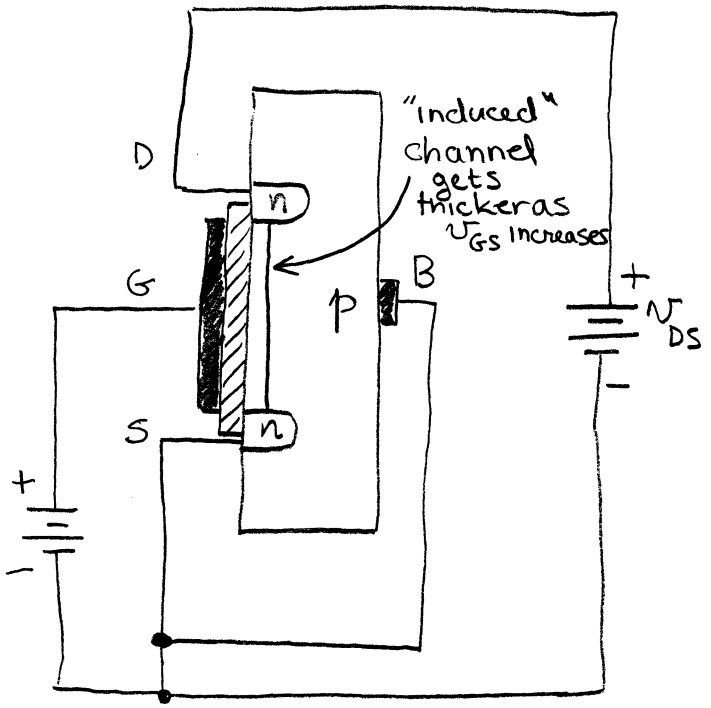


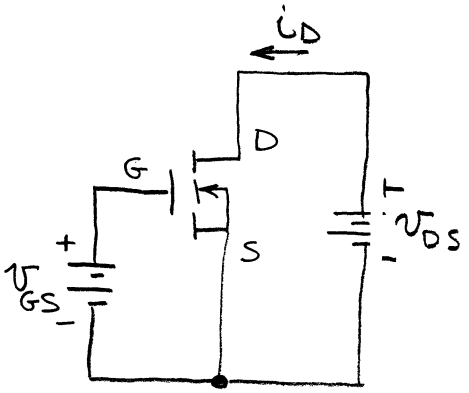

There are p-n junctions at drain-body & source-body
Drain-Source junction is reverse biased so $i_D \approx 0$
and we say the device is cutoff.

When $v_{GS}$ reaches a threshold voltage $V_{to}$
a channel of n-type material is "induced" in the region under the gate.

$$i_D = 0 \text{ for } v_{GS} \leq V_{to}$$

# Operation in the triode region




triode region

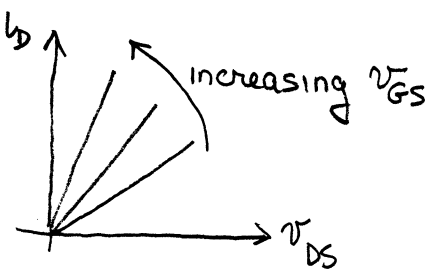
$v_{GS} \geq V_{to}$

$v_{DS} < v_{GS} - V_{to}$

The electric field from the gate repels holes and attracts electrons (which can flow in the forward direction across :-B) "inducing" a virtual channel under the gate.

For small values of $v_{DS}$, $i_D \propto v_{DS}$

It's also proportional to the excess gate voltage $v_{GS} - V_{to}$




In the triode region

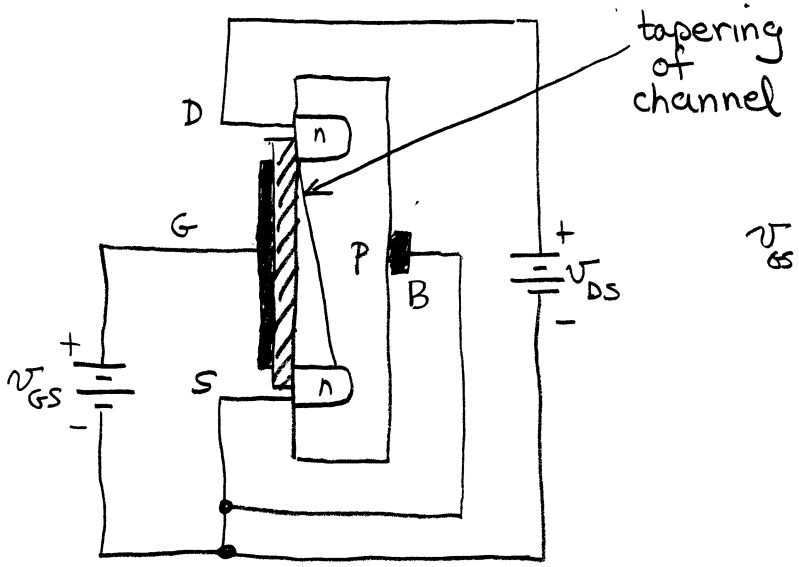
$$i_D = K\left[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2\right]$$

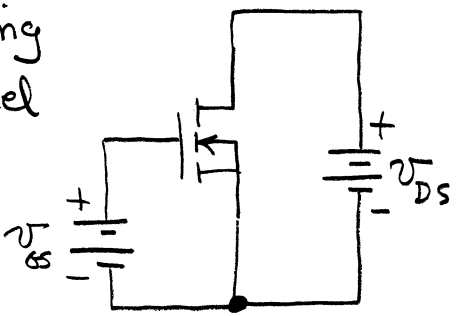
where $K = \left(\frac{W}{L}\right)\frac{kP}{2}$ ← process dependent

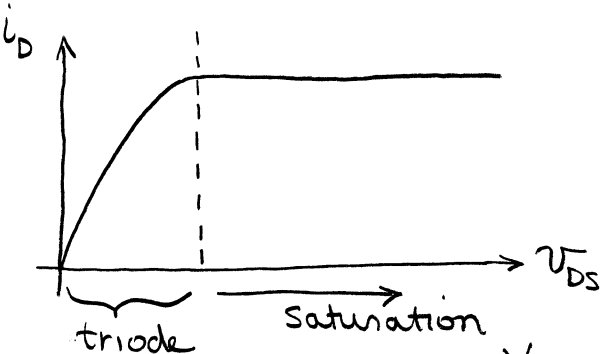
In this region MOSFETs behave like voltage-controlled resistors.

If $v_{DS}$ increases, the channel "thickness" will vary with position. Because $v_{Gchannel}$ decreases as we get closer to the drain the channel tapers. This leads to saturation.

Operation in the saturation region



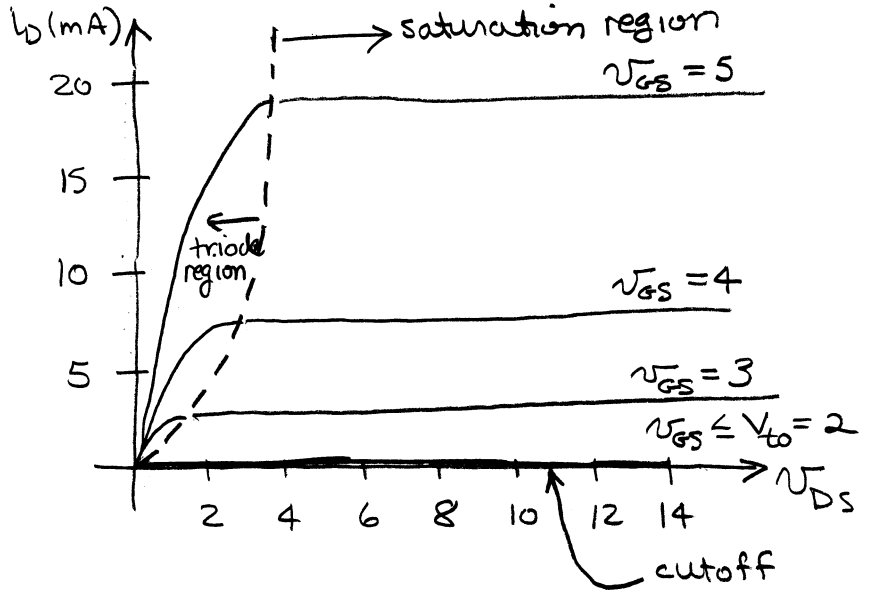

In the saturation region

$$i_D = k(v_{GS} - V_{to})^2$$

where $v_{GS} \geq V_{to}$

$v_{DS} \geq v_{GS} - V_{to}$

MOSFET characteristics




The channel thickness at the drain is zero when $v_{GD} = V_{to}$.

$$v_{GD} = V_{to}$$

$$v_{GS} - v_{DS} = V_{to}$$

$$v_{GS} = V_{to} + v_{DS}$$

But $i_D = K(v_{GS} - V_{to})^2$ in saturation

substituting

$$i_D = K(V_{to} + v_{DS} - V_{to})^2 = K v_{DS}^2$$

which is the equation of the parabola plotted above.

# PSpice modeling of MOSFETs

To model MOSFETs we need to add a new parameter $\lambda$.

For short channels the channel length L can be modified by the depletion region around the drain becoming thicker. This effectively decreases the channel length as $v_{DS}$ increases.

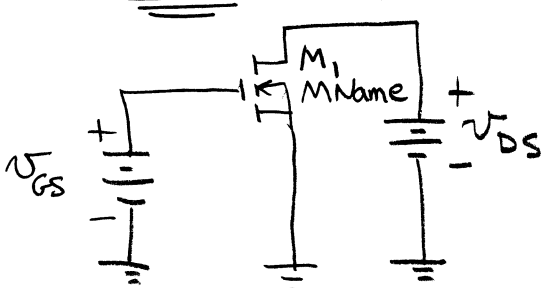
Use breakout part MbreakN3

Use edit/model/edit instance model

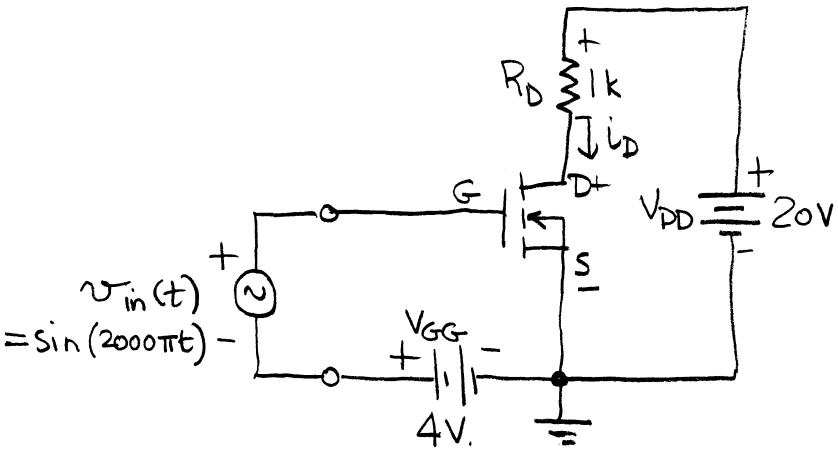
Enter

```
model MName NMOS
KP= 50u
Vto = 2
LAMBDA = 0.05
```

Do a DC nested sweep.



# 5.2 Load-line analysis of NMOS amplifier

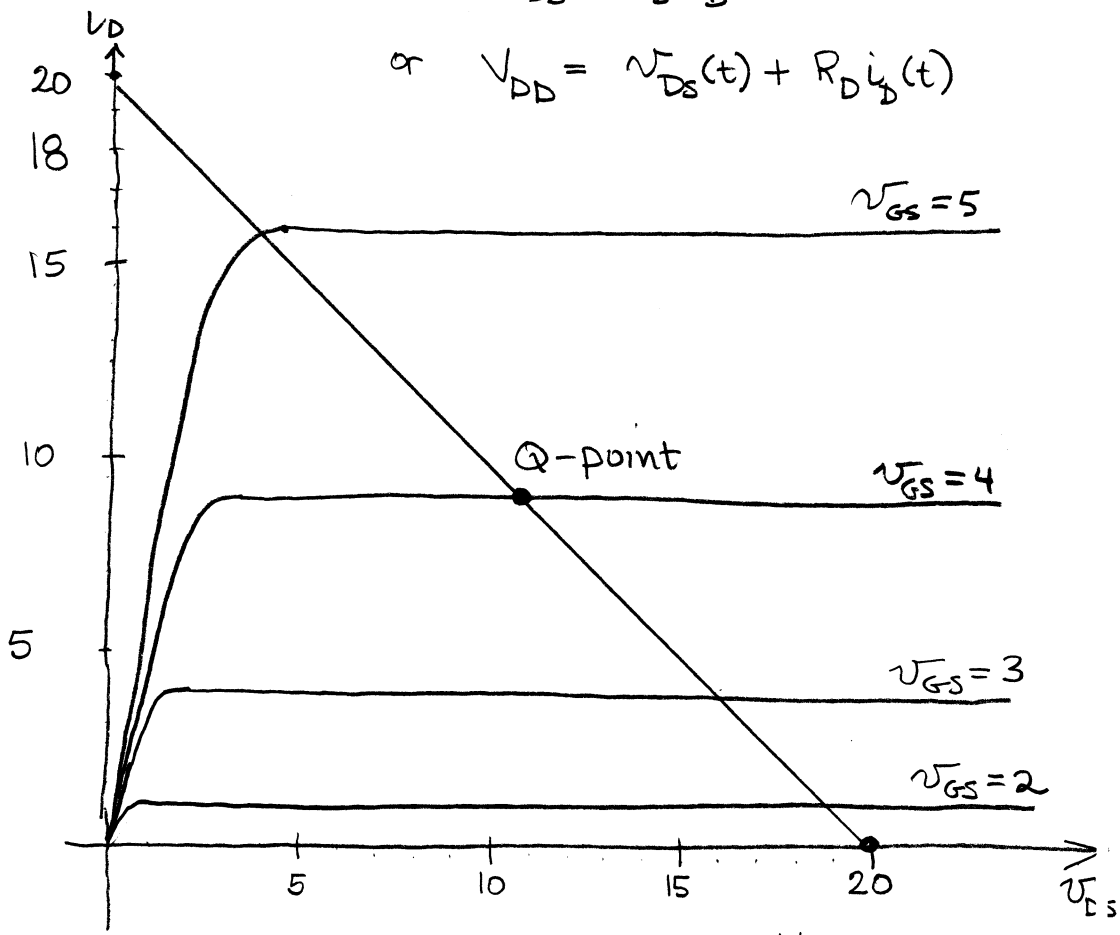



KVL on input loop $\quad -V_{GG} - v_{in}(t) + v_{GS}(t) = 0.$

or $\quad v_{GS}(t) = V_{GG} + v_{in}(t)$

KVL on drain loop $\quad -v_{DS} - i_D R_D + V_{DD} = 0$

or $\quad V_{DD} = v_{DS}(t) + R_D i_D(t)$




For load line $V_{OC} = 20V$, $I_{SC} = \frac{V_{DD}}{R_D} = \frac{20V}{1k} = 20mA$

If $v_{in} = 0$ $v_{GS} = V_{GG} = 4V$ establishing Q-point.

Now let $v_{in}$ vary.

For $v_{in} = +1$ volt, we move to $v_{GS} = 1 + 4 = 5$V.

at $v_{GS} = 5$ on load line

$v_{DS} = 4$V, $i_D \sim 15.8$ mA

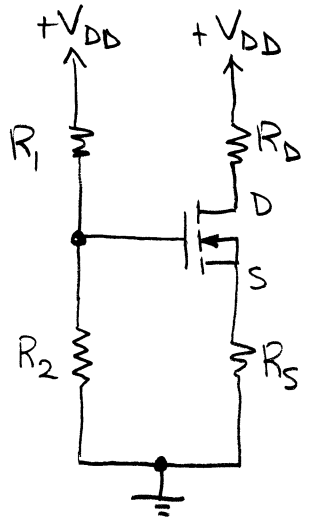
For $v_{in} = -1$ volt, we move to $v_{GS} = -1 + 4 = 3$V

at $v_{GS} = 3$V on load line

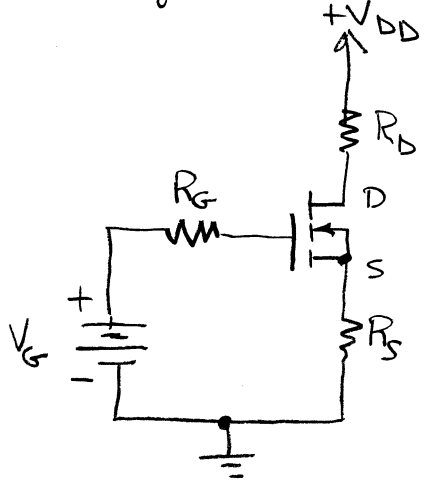
$v_{DS} = 16$V, $i_D \sim 4$ mA

## 5.3 Bias circuits

Because of device to device variation and distortion considerations we use a <u>fixed- plus self bias</u> circuit very similar to that used for BJT amplifiers.




Thevenize gate circuit




By inspection

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

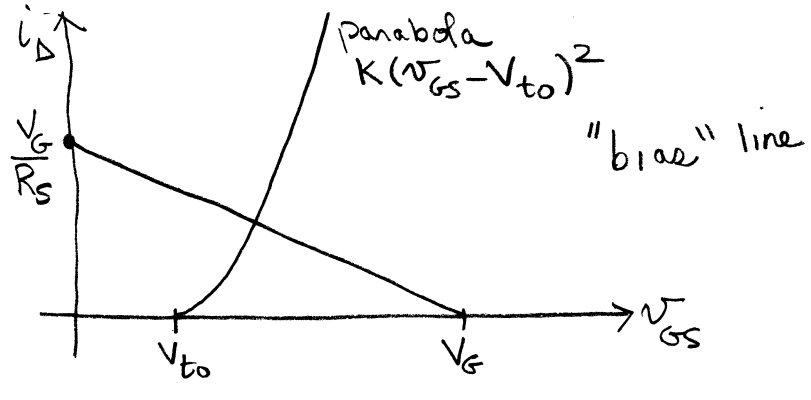
$$R_G = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

For the gate circuit $-V_G + i_G R_G + v_{GS} + i_D R_S = 0$ ($i_G \to 0$)

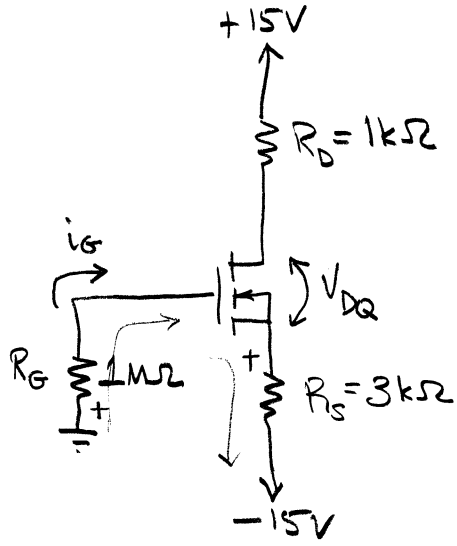
★ Assuming biased in saturation region $i_D = K(v_{GS} - V_{to})^2$

We can plot this

load line for gate circuit is called "bias" line



5.22




MOSFET has
$V_{to} = 1V$
$\lambda = 0$
$K = 0.25 mA/V^2$

Find $I_{DQ}, V_{DSQ}$

Do KVL of gate circuit

$$+ \cancel{i_G}^{0} R_G + v_{GS} + i_S R_S - 15 = 0,$$

$$v_{GS} + i_S R_S = 15$$

but $i_D = K(v_{GS} - V_{to})^2$ and, since $i_D = i_S$

substituting $\therefore \quad v_{GS} + K(v_{GS} - V_{to})^2 R_S = 15$

$$v_{GS} + 0.25\frac{mA}{V^2}(v_{GS} - 1)^2 (3k) = 15$$

$$v_{GS} + \frac{3}{4}(v_{GS} - 1)^2 = 15$$

$$4 v_{GS} + 3(v_{GS}^2 - 2v_{GS} + 1) = 60$$

$$3 v_{GS}^2 - 2 v_{GS} - 57 = 0$$

$$v_{GS} = \frac{-(-2) \pm \sqrt{(-2)^2 - 4(3)(-57)}}{2(3)}$$

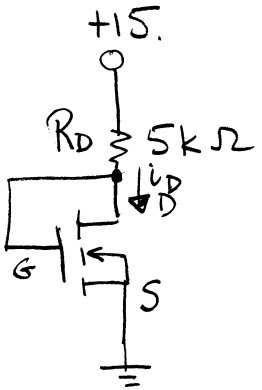
$$= \frac{2 \pm \sqrt{4 + 684}}{6} = \frac{2 \pm \sqrt{688}}{6}$$

$$v_{GS} = +4.7\,V, \; -4.04\,V$$

MUST be $V_{GS} = +4.7$ Volts. $\Rightarrow i_D = K(v_{GS} - V_{to})^2 = \frac{1}{4}(4.7 - 1)^2 = 3.43 mA$

$V_{DQ} = 30 - (3.43)(1) - (3.43)(3) = 16.28V.$

For the circuit shown below $V_{to} = 2V$, $K = 0.3\ mA/V^2$.
Determine $I_D$ and $V_{DS}$.




$i_D = K(v_{GS} - V_{to})^2$ in saturation region (1)

$v_{GS} = v_G - 0$ since source grounded.

$v_{GS} = 15 - i_D R_D$ since $v_G = v_D$

$i_D = \dfrac{15 - v_{GS}}{R_D}$

$\therefore \quad \dfrac{15 - v_{GS}}{5} = 0.3(v_{GS} - 2)^2$ by substitution into (1)

$15 - v_{GS} = 1.5(v_{GS}^2 - 4v_{GS} + 4)$

$15 - v_{GS} = 1.5v_{GS}^2 - 6v_{GS} + 6$

$1.5v_{GS}^2 - 5v_{GS} - 9 = 0.$

$$v_{GS} = \frac{-(-5) \pm \sqrt{(-5)^2 - 4(1.5)(-9)}}{2(1.5)} = \frac{5 \pm \sqrt{25 + 54}}{3}$$

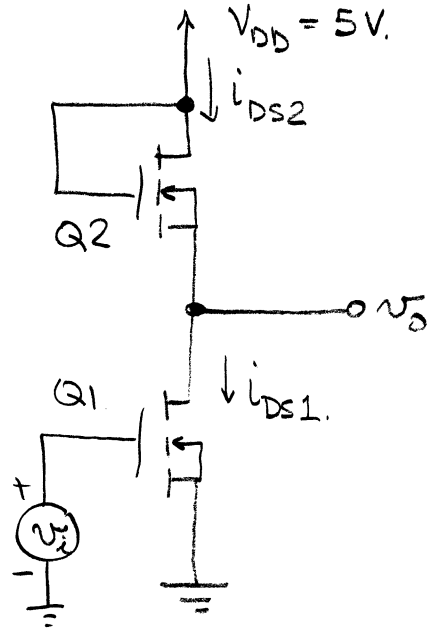
$v_{GS} = +4.63, -1.30$

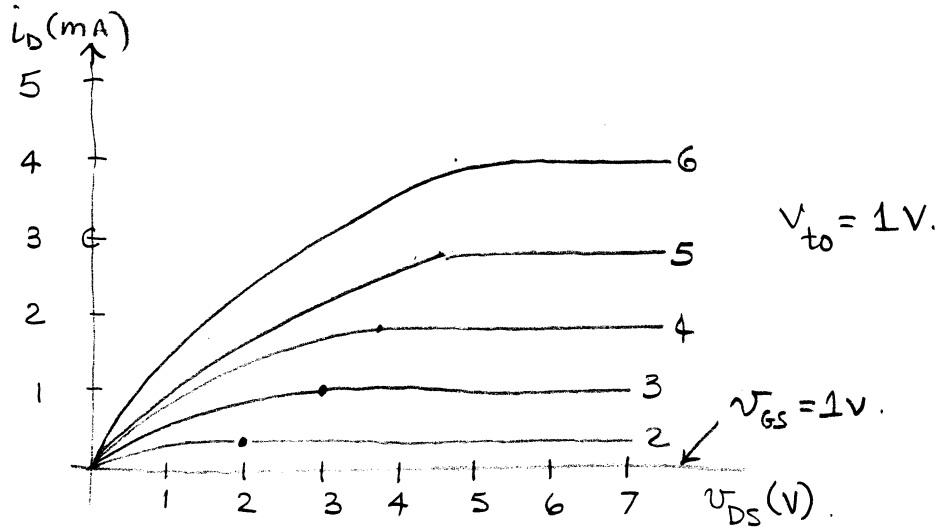
Pick $v_{GS} = +4.63$ ($v_{GS} > v_{to}$ in saturation region)

Then $i_D = \dfrac{15 - (4.63)}{5k} = 2.07\ mA$

$v_{DS} = 15 - (2.07)(5k) = 4.63V.$

3.6.2.




$V_{to} = 1V.$

(a) obtain $i_{DS1}$ as a function of $v_{DS1}$

$$v_{DS2} = V_{DD} - v_{DS1}.$$

$$i_{DS2} = K(v_{DS2} - V_{to})^2$$

both transistors are identical (Assume saturation)

$$i_{DS2} = K(V_{DD} - v_{DS1} - V_{to})^2$$

(b) The result from (b) represents a non-linear load line for Q1. Plot the load line on the characteristic curve assuming $V_{to} = 1V$ and $K = \frac{3}{16} \times 10^{-3}\ A/V^2$.

from (a) $i_{DS2} = K(V_{DD} - v_{DS1} - V_{to})^2$

using the problem's values.

$$i_{DS2} = \frac{3}{16}(5 - v_{DS1} - 1)^2 \text{ mA}$$

$$i_{DS2} = \frac{3}{16}(4 - v_{DS1})^2 \text{ mA}$$

Note that $i_{DS2} = i_{DS1}$

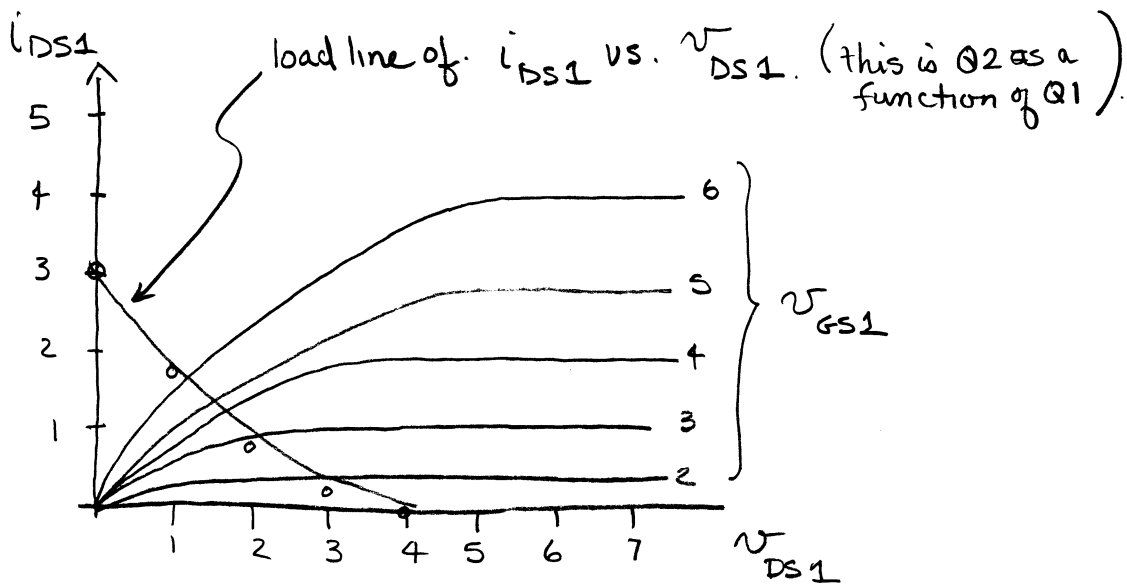
$v_{DS1} = 0$ $\quad i_{DS2} = \frac{3}{16}(4-0)^2 = 3\text{ mA}.$

$v_{DS1} = 1$ $\quad i_{DS2} = \frac{3}{16}(4-1)^2 = \frac{27}{16}\text{ mA} = 1.7\text{ mA}.$

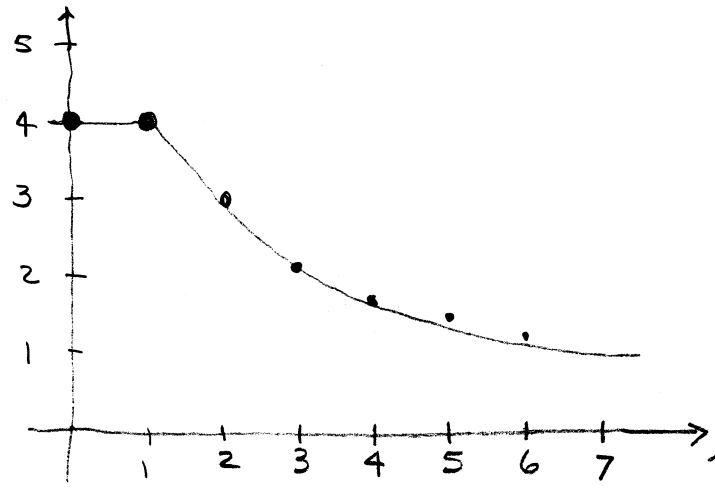
$v_{DS2} = 2$ $\quad i_{DS2} = \frac{3}{16}(4-2)^2 = \frac{12}{16}\text{ mA} = 0.75\text{ mA}$

$v_{DS2} = 3$ $\quad i_{DS2} = \frac{3}{16}(4-3)^2 = \frac{3}{16}\text{ mA} = 0.1875\text{ mA}.$

$v_{DS} = 4$ $\quad i_{DS} = 0.$



(c) Plot $V_o$ vs. $v_i$




if $v_{in} = 0$ Q1 is in cutoff since $v_{gs} < v_{to}$
then $v_o = v_{DS1} = 4$ volts.

if $v_{in} = 1$ Q1 is just turning on, no change
$v_{DS1} = 4$ volts.

if $v_{in} = 2$ we read off intersection of $v_{GS} = 2$
with non-linear load line.
by inspection $v_{DS1} \cong 3V$.

if $v_{in} = 3$ $v_{GS} = 3$ and
by inspection $v_{DS1} \cong 2.1V$.

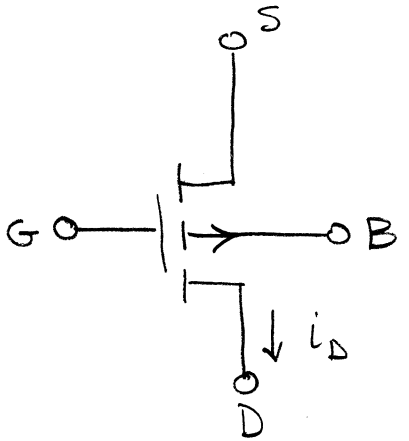
if $v_{in} = 4$ $v_{GS} = 4$ and by inspection $v_{DS1} \cong 1.75$

if $v_{in} = 5$ $v_{GS} = 5$ and by inspection $v_{DS1} \cong 1.5V$.

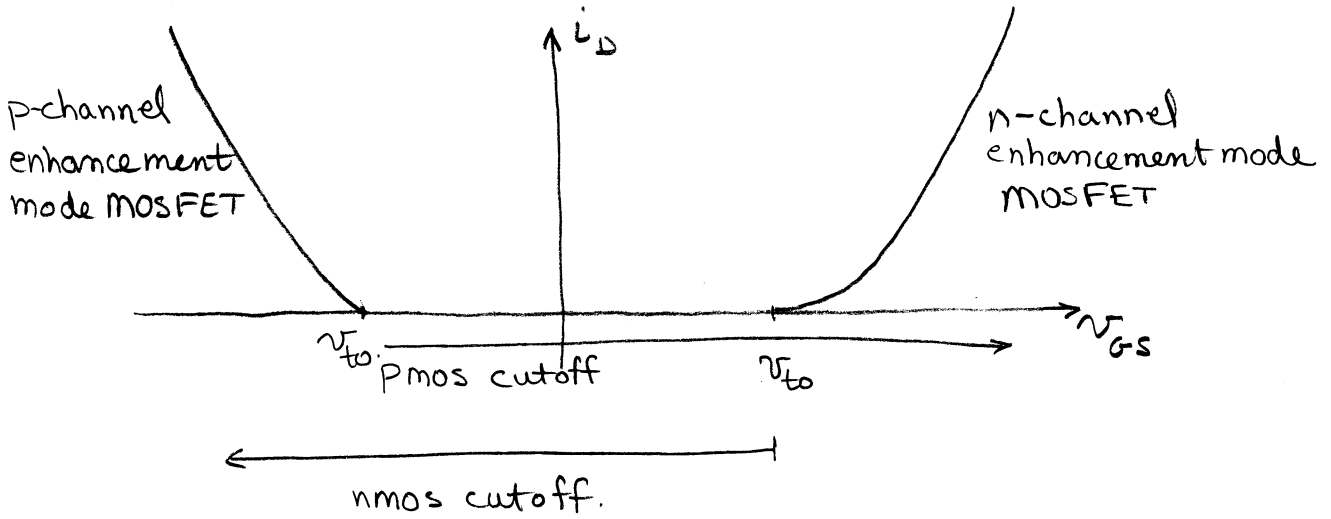
if $v_{in} = 6$ $v_{GS} = 6$ and by inspection $v_{DS} \cong 1.25V$

Technically this could be an NMOS amplifier or inverter

# p-channel MOSFETs. (p. 332 of text).




Equations are exactly the same except voltage polarities and current directions are reversed.



# 5.4 Small-signal equivalent circuits

for small signal analysis let

$$i_D(t) = I_{DQ} + i_d(t) \qquad v_{GS}(t) = V_{GSQ} + v_{gs}(t)$$

Assume that the MOSFET is biased in saturation so that

$$i_D = K(v_{GS} - V_{to})^2$$

Substituting the small signal values into this equation gives

$$I_{DQ} + i_d(t) = K\left[V_{GSQ} + v_{gs}(t) - V_{to}\right]^2$$

Expanding

$$I_{DQ} + i_d(t) = K\left[V_{GSQ} - V_{to}\right]^2 + 2K\left(V_{GSQ} - V_{to}\right)v_{gs}(t) + K v_{gs}^2(t)$$

$I_{DQ}$: DC bias terms

$K\left[V_{GSQ} - V_{to}\right]^2$: cancel

$K v_{gs}^2(t)$

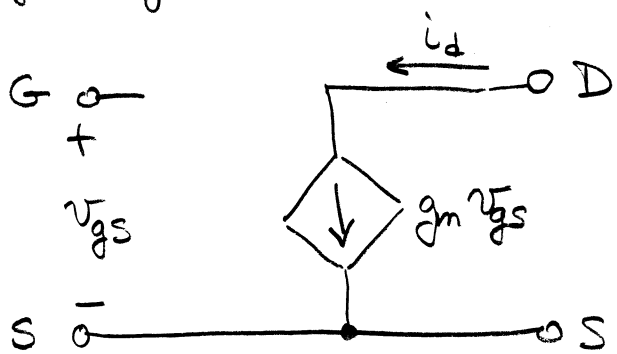
Assume small signal such that $|v_{gs}(t)| \ll |V_{GSQ} - V_{to}|$

This allows last term to be dropped

$$\therefore \quad i_d(t) = \underbrace{2K\left(V_{GSQ} - V_{to}\right)}_{\text{define } g_m = 2K\left(V_{GSQ} - V_{to}\right)} v_{gs}(t)$$

$$\therefore \quad i_d(t) = g_m v_{gs}(t)$$

small-signal equivalent circuit

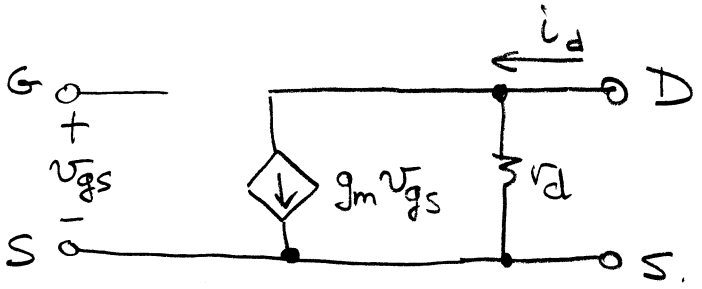



$$g_m = 2\sqrt{K I_{DQ}}$$

more formally define using Taylor series expansion

$$g_m \equiv \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=0} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}}$$

$$\frac{1}{r_d} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}}$$



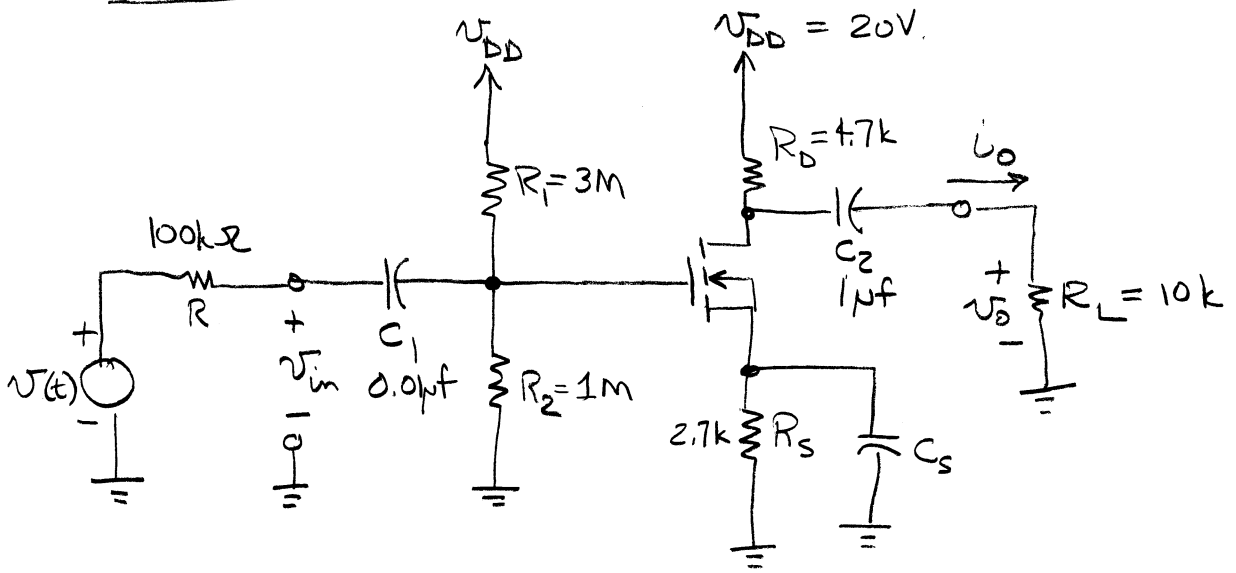

$$i_d(v_{gs}, v_{ds}) = i_d(v_{GSQ}, v_{DSQ}) + \left.\frac{\partial i_d}{\partial v_{GS}}\right|_{Q\text{ point}} \Delta v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\text{-point}} \Delta v_{ds} + \Delta i_d(v_{gs}, v_{ds})$$

$$\therefore \quad \Delta i_d(v_{gs}, v_{ds}) = \left.\frac{\partial i_D}{\partial v_{GS}}\right| \Delta v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right| \Delta v_{ds}$$

$$= g_m \Delta v_{gs} + \frac{1}{r_d} \Delta v_{ds}$$

where $\Delta i_D$, $\Delta v_{gs}$ and $\Delta v_{ds}$ are small signal quantities

## 5.5 Common Source Amplifier




Example 5.28. Analyze in mid-band where $v(t) = 100 \sin(2000\pi t)$

Do bias first. Given $KP = 50\mu A/V^2$, $V_{to} = 2V$, $\lambda = 0$, $L = 10\mu m$, $W = 400\mu m$.

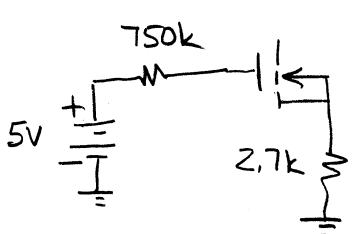
$$K = \left(\frac{W}{L}\right)\frac{KP}{2} = \left(\frac{400\,\mu m}{10\,\mu m}\right)\frac{50\mu A/V^2}{2} = 1mA/V^2$$

Analyze bias circuit by Thevenize

$$V_G = V_{DD}\frac{R_2}{R_1+R_2} = (20V)\frac{1M}{1M+3M} = 20\left(\frac{1}{4}\right) = 5V$$

$$R_G = \frac{R_1 R_2}{R_1+R_2} = \frac{(1M)(3M)}{1M+3M} = \frac{3}{4}M.$$

bias circuit




$$-5V + 750k\,(I_G \to 0) + V_{GS} + I_S R_S = 0$$

$I_S \to I_{D,Q}$

$$\therefore\ V_{GS} + I_{D,Q} R_S = 5$$

and $I_{D,Q} = K(V_{GS} - V_{to})^2$.

substituting

$$V_{GS} + K(V_{GS} - V_{to})^2 R_S - 5 = 0.$$

$$V_{GS} + (1\,mA/V^2)(2.7k)(V_{GS} - 2)^2 - 5 = 0$$

$$V_{GS} + 2.7(V_{GS}^2 - 4V_{GS} + 4) - 5 = 0$$

$$2.7V_{GS}^2 - 9.8V_{GS} + 5.8 = 0$$

$$V_{GS} = \frac{-(-9.8) \pm \sqrt{(-9.8)^2 - 4(2.7)(5.8)}}{2(2.7)}$$

$$= \frac{9.8 \pm \sqrt{33.4}}{5.4} = \frac{9.8 \pm 5.78}{5.4}$$

$$V_{GS} = 2.89,\ 0.79\,V$$

Choosing $V_{GS,Q} = 2.89$ since $V_{to} = 2V$

$$I_{D,Q} = K(V_{GS} - V_{to})^2 = \frac{1\,mA}{V^2}(2.89 - 2)^2 = 0.79\,mA$$

$$V_{DS,Q} = 20 - (0.79mA)(4.7k) - (0.79mA)(2.7k)$$

$$V_{DS,Q} = 14.15\ Volts$$

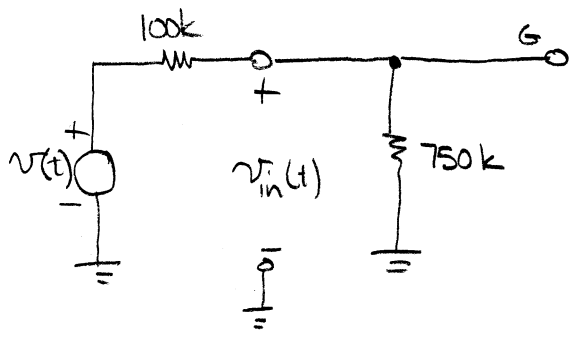
Now do small signal analysis

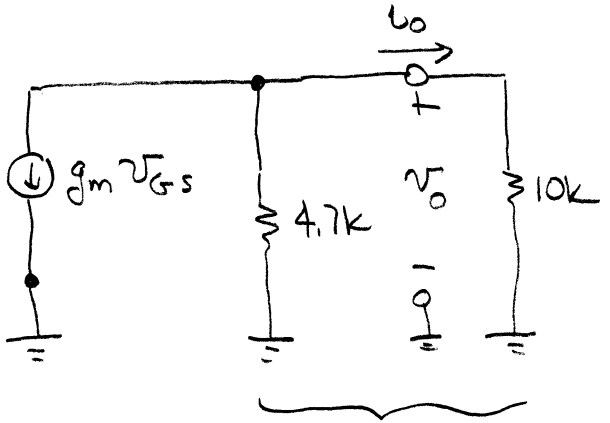
$$g_m = \sqrt{2KP}\sqrt{\frac{W}{L}}\sqrt{I_{D,Q}}$$

$$= \sqrt{2\left(1.05\frac{mA}{V^2}\right)}\sqrt{\frac{400\mu m}{10\mu m}}\sqrt{0.79mA} = 1.78\,mS$$

because $\lambda = 0$ $\quad r_d = \infty$

In midband




$$R_L' = \frac{(4.7k)(10k)}{4.7k + 10k} = 3197\Omega$$

By inspection

$$v_o = -g_m v_{GS} R_L'$$

$$= -(0.00178) v_{GS} (3197) = -5.69 v_{GS}$$

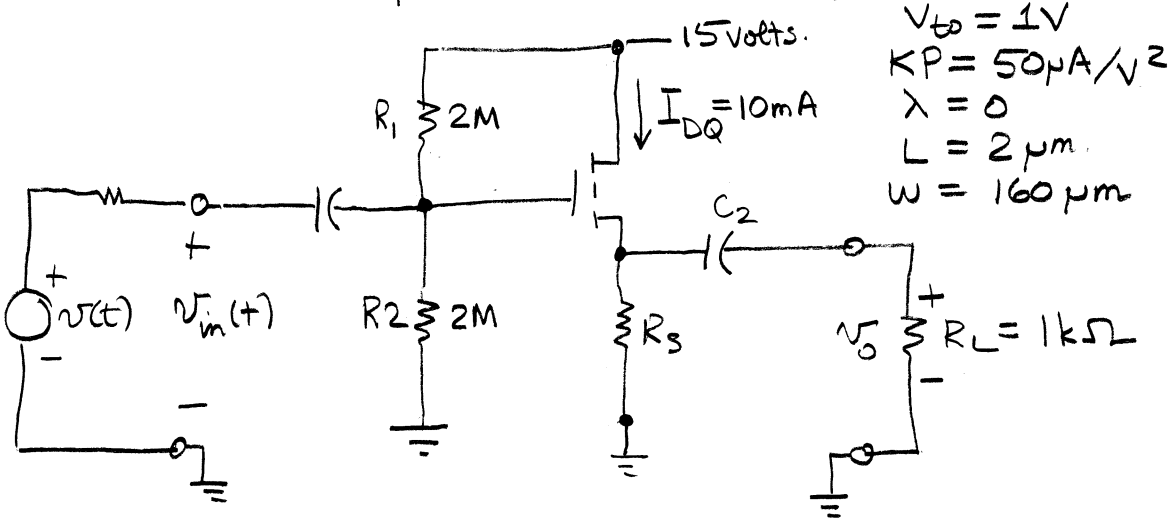
$$\frac{v_o}{v_{in}} = \frac{-5.69 v_{GS}}{v_{in}} = -5.69 \frac{v_{in}}{v_{in}} = -5.69$$

$$R_{in} = \frac{v_{in}}{i_{in}} = 750k.$$

$$R_o = \frac{v_o}{i_o}\bigg|_{\substack{\text{looking} \\ \text{into amp.}}} = \frac{+g_m v_{GS} R_D}{g_m v_{GS}} \simeq 4.7k.$$

## 5.6 The Source Follower

This is basically identical to the common source analysis EXCEPT the output is taken from the source.




$V_{to} = 1V$
$KP = 50\mu A/V^2$
$\lambda = 0$
$L = 2\mu m$
$W = 160\mu m$

**DC Analysis:** $K = \left(\frac{W}{L}\right)\frac{KP}{2} = \left(\frac{160\mu m}{2\mu m}\right)\frac{50\mu A/V^2}{2} = 2mA/V^2$

Now let's calculate the $V_{GS}$ that gives $I_{DQ} = 10mA$

$$I_D = K(V_{GS} - V_{to})^2$$

$$10mA = 2mA/V^2 (V_{GS} - 1)^2$$

$$5V^2 = (V_{GS} - 1)^2$$

$$\pm\sqrt{5} = V_{GS} - 1$$

$$V_{GS} = 1 \pm \sqrt{5} = 3.236, -1.236$$

choose this solution since $-1.236 < V_{to}$

Now find the gate voltage by Thevenizing as usual

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{2M}{2M + 2M}(15V) = 7.5V.$$

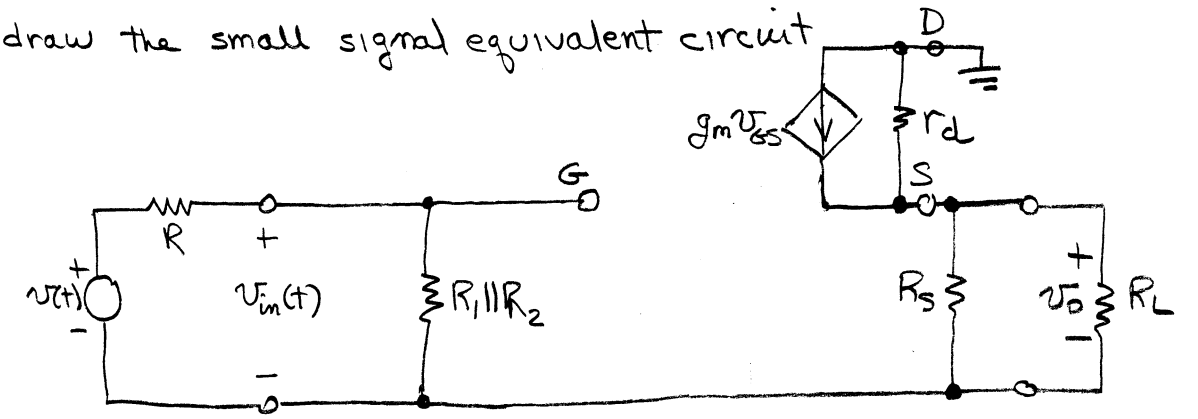
This gives us the information to calculate $R_S$.

$$V_{GS} = V_G - V_S$$

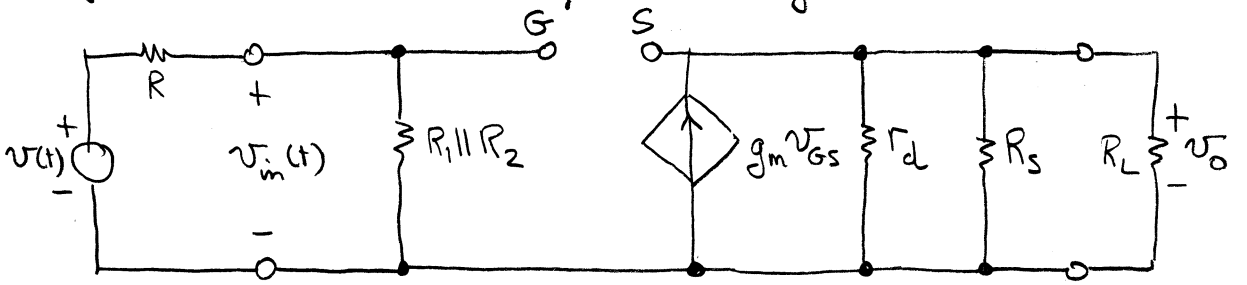
$$\text{or } V_S = V_G - V_{GS} = 7.5V - 3.236V = 4.264V.$$

$$R_S = \frac{V_S}{I_D} = \frac{4.264V}{10mA} = 426\Omega.$$

Now draw the small signal equivalent circuit




Note that the drain is grounded through the power supply. We can re-arrange this circuit to more easily see the analysis.




Now calculate the small signal parameters

$$g_m = \sqrt{2KP}\sqrt{\frac{W}{L}}\sqrt{I_{D,Q}} = \sqrt{2(50\times10^{-6})}\sqrt{\frac{160}{2}}\sqrt{10\times10^{-3}}$$

$$g_m = 8.944\times10^{-3}\ S$$

$\lambda = 0 \Rightarrow$ characteristics are flat in saturation region

and $\quad \frac{1}{r_d} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = 0$

Remaining analysis is straight forward;

$$R_L' = R_S \| R_L = 426 \| 1000 = 298.7\,\Omega$$

$$v_o = (+g_m v_{GS})(R_L') = (+8.944\times10^{-3} v_{GS})(298.7)$$

$$v_o = +2.672\, v_{GS}$$

Now do KVL (recall this is $v_{GS}$)

$$-v_{in} + v_{GS} + v_o = 0 \Rightarrow v_{GS} = v_{in} - v_o$$

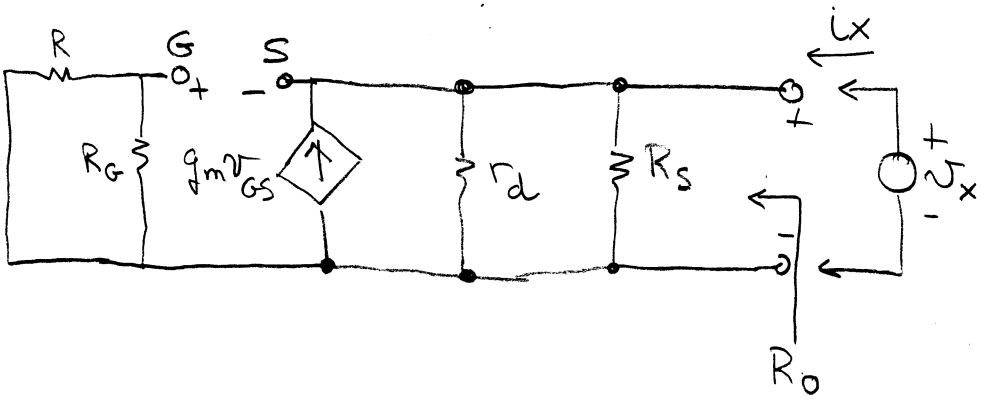
$$v_o = +2.672(v_{in} - v_o) = +2.672 v_{in} - 2.672 v_o$$

$$+3.672 v_o = +2.672 v_{in}$$

$$\frac{v_o}{v_{in}} = \frac{+2.672}{3.672} = +0.72$$

$R_{in} = R_1 \| R_2 = 2M \| 2M = 1M$

The output impedance is a little harder to calculate.




by definition $R_o = \frac{v_x}{i_x}$

by inspection $V_G = 0, \; V_S = +v_x$

$V_{GS} = V_G - V_S = -v_x$

Do KCL at output

$$\sum_{\text{into}} i = 0 \qquad +g_m(-v_x) - \frac{v_x}{r_d} - \frac{v_x}{R_s} + i_x = 0$$

$$\left(-g_m - \frac{1}{r_d} - \frac{1}{R_s}\right) v_x = -i_x$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_d} + \frac{1}{R_s}}$$

For this example:

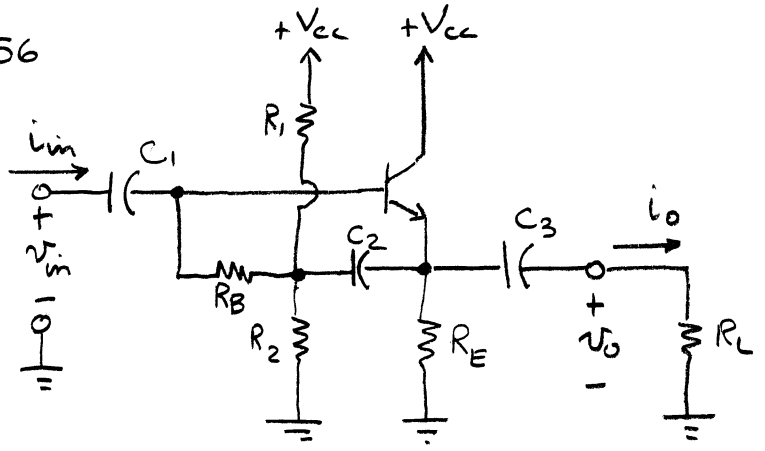
$$R_o = \frac{1}{.00894 + 0 + \frac{1}{426\Omega}} = 88.6\Omega$$

Calculate current gain

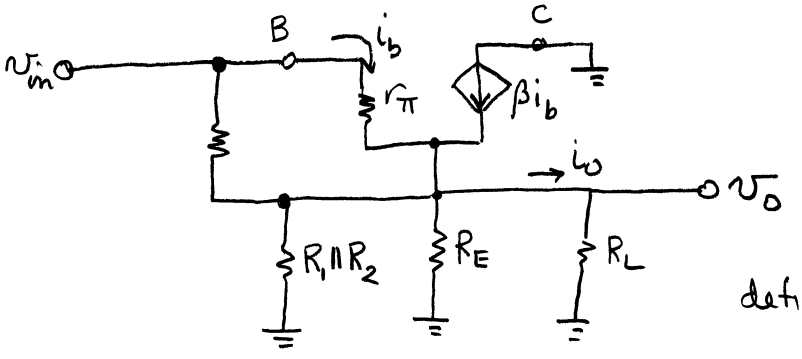
$$A_i = \frac{i_o}{i_{in}} = \frac{v_o/R_L}{v_{in}/R_{in}} = \left(\frac{v_o}{v_{in}}\right)\frac{R_{in}}{R_L} = (0.72)\left(\frac{1M}{1000}\right) = 720$$

$$A_p = A_i A_v = (720)(.72) = 518.4.$$

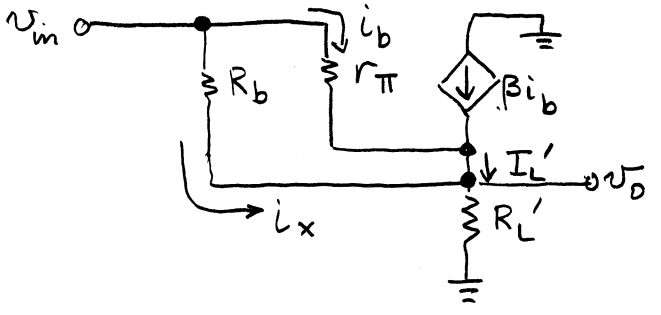
4.56




(a) Draw the small signal circuit in midband.




define $R_L' = R_1 \parallel R_2 \parallel R_E \parallel R_L$




$v_o = i_L' R_L'$

where

$i_L' = i_x + (\beta+1) i_b$

Since $r_\pi$ & $R_b$ have the same voltage across them:

$$v = i_x R_b = i_b r_\pi \quad \text{or} \quad i_x = i_b \frac{r_\pi}{R_b}$$

Then $$v_o = (i_x + I_L') R_L' = \left( i_b \frac{r_\pi}{R_b} + (\beta+1) i_b \right) R_L'$$

By inspection $$v_{in} = i_b r_\pi + v_o$$

$$\therefore A_v = \frac{v_o}{v_{in}} = \frac{i_b \left( \frac{r_\pi}{R_b} + (\beta+1) \right) R_L'}{i_b r_\pi + i_b \left( \frac{r_\pi}{R_b} + (\beta+1) \right) R_L'}$$

$$A_v = \frac{\left(1+\beta+\frac{r_\pi}{R_b}\right) R_L'}{r_\pi + R_L'\left(1+\beta+\frac{r_\pi}{R_b}\right)}$$

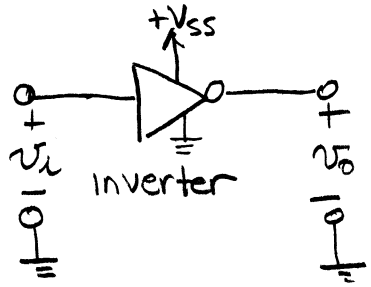
To compute $R_{in}$ we need $i_{in}$

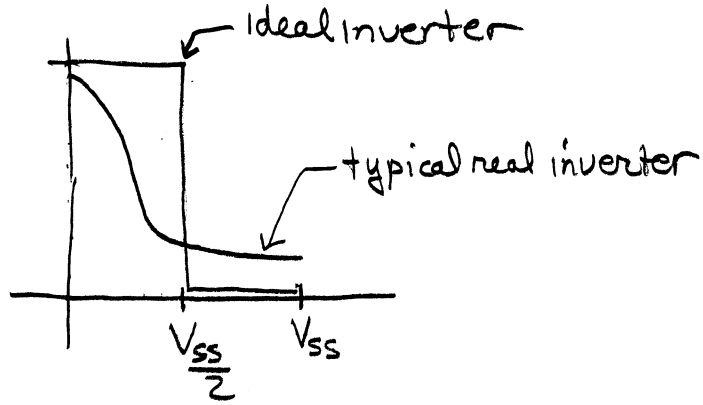
$$i_{in} = \frac{V_{in} - V_o}{R_b \| r_\pi} = \frac{V_{in} - A_v V_{in}}{R_b \| r_\pi}$$

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{V_{in}}{\frac{V_{in}(1-A_v)}{R_b \| r_\pi}} = \frac{R_b \| r_\pi}{1-A_v}$$

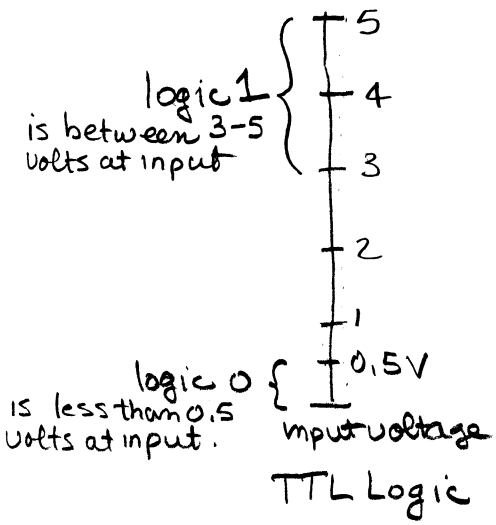
# 6.2 Electrical Specifications for Logic Gates.

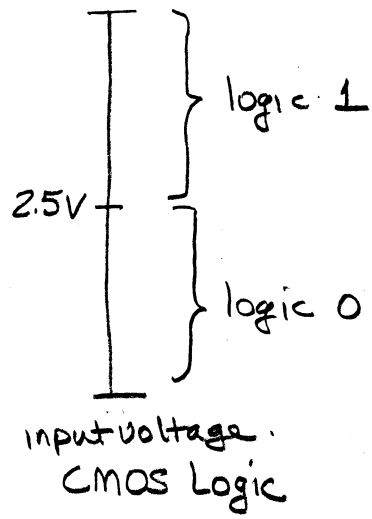
## Transfer Characteristics of Logic Inverters



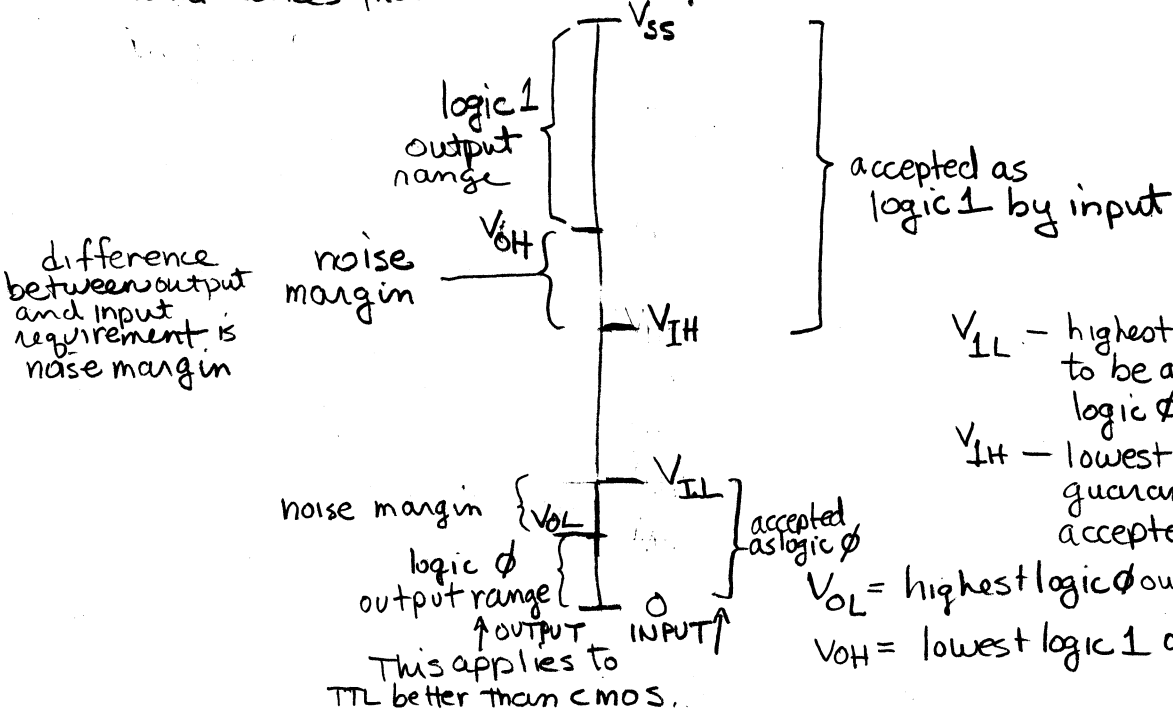

What inverters actually do at the input.




Anything above 2.5V at input is a logic 1.

What devices produce at the output:



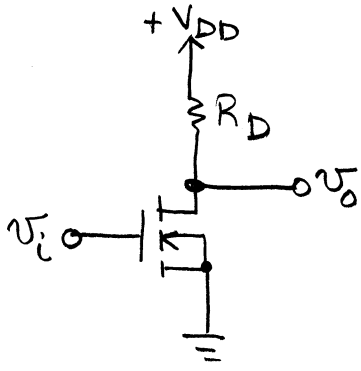

$V_{IL}$ – highest input guaranteed to be accepted as logic ∅

$V_{IH}$ – lowest input voltage guaranteed to be accepted as logic 1

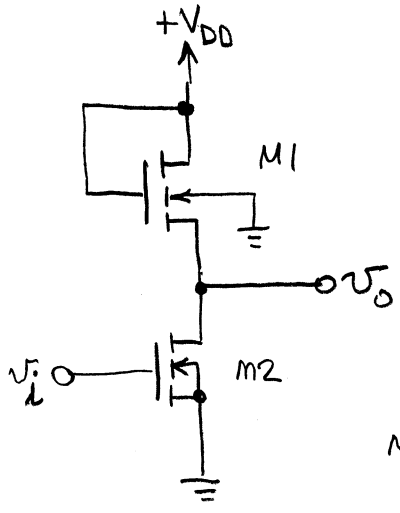
$V_{OL}$ = highest logic ∅ output produced

$V_{OH}$ = lowest logic 1 output produced

# Types of MOS inverter

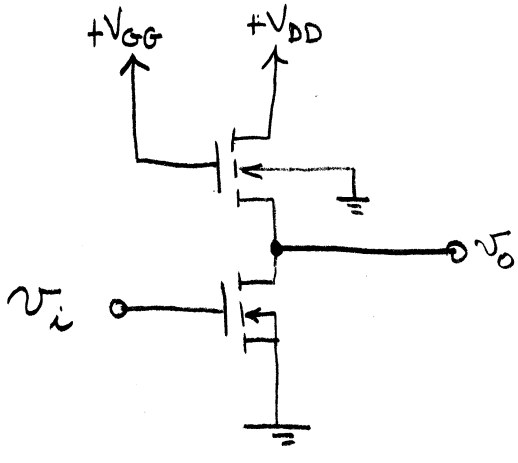



Resistor pull-up




active NMOS pull-up.

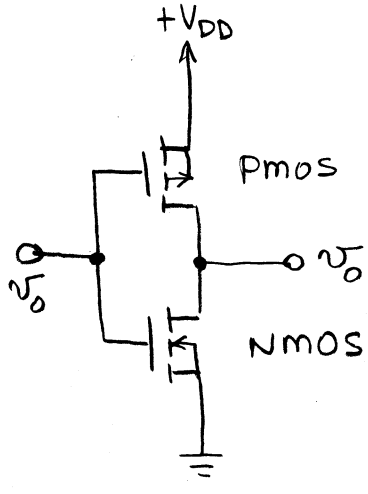
NOTE
Problem occurs when $v_o$ = High.
M1 $v_{GS}$=0 and load is OFF.
Makes circuit susceptible to noise in output.




active NMOS pull-up with separate bias source

Separate $V_G$ can eliminate output noise susceptibility

$V_{GG} > V_{DD}$

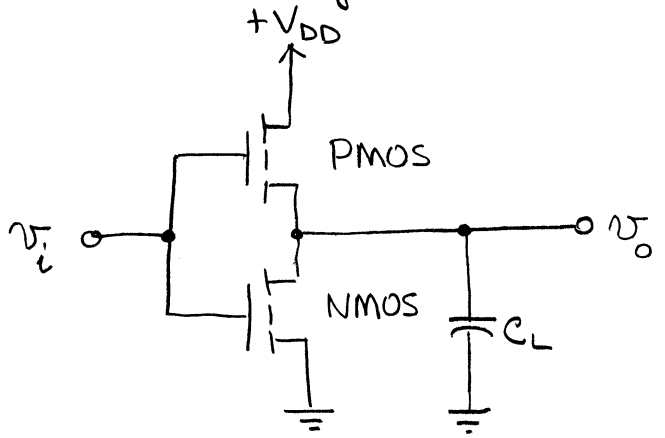


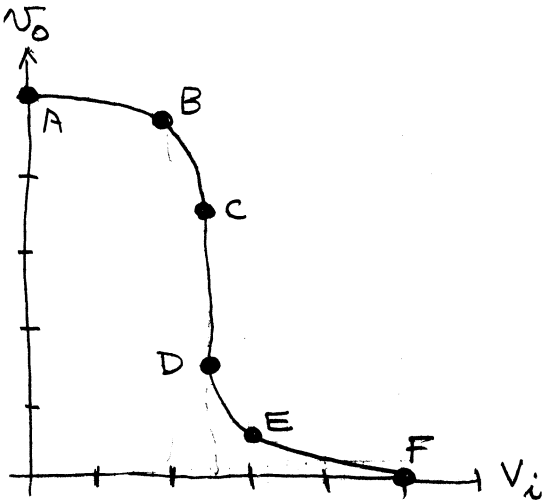

complementary MOS (CMOS)

Most modern logic is this type.

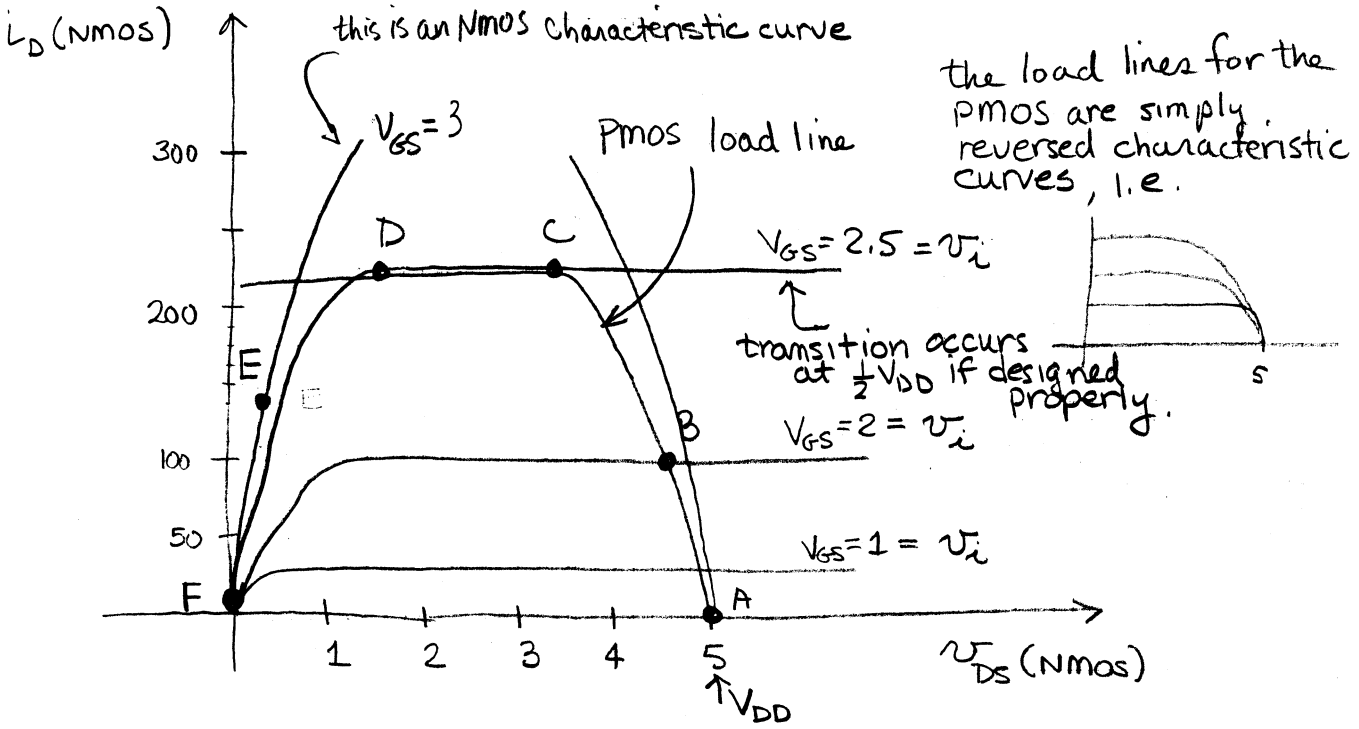
Symmetry between Pmos and NMOS characteristics requires careful selection of $\frac{W}{L}$ ratio.

## 6.5 Graphical analysis of CMOS inverter




We want to be in either A or F. states.




the load lines for the PMOS are simply reversed characteristic curves, i.e.



transition occurs at $\frac{1}{2}V_{DD}$ if designed properly.

A – $v_i = 0$ PMOS highly ON since $v_{GS} = -5$
NMOS cutoff since $v_{GS} = 0$

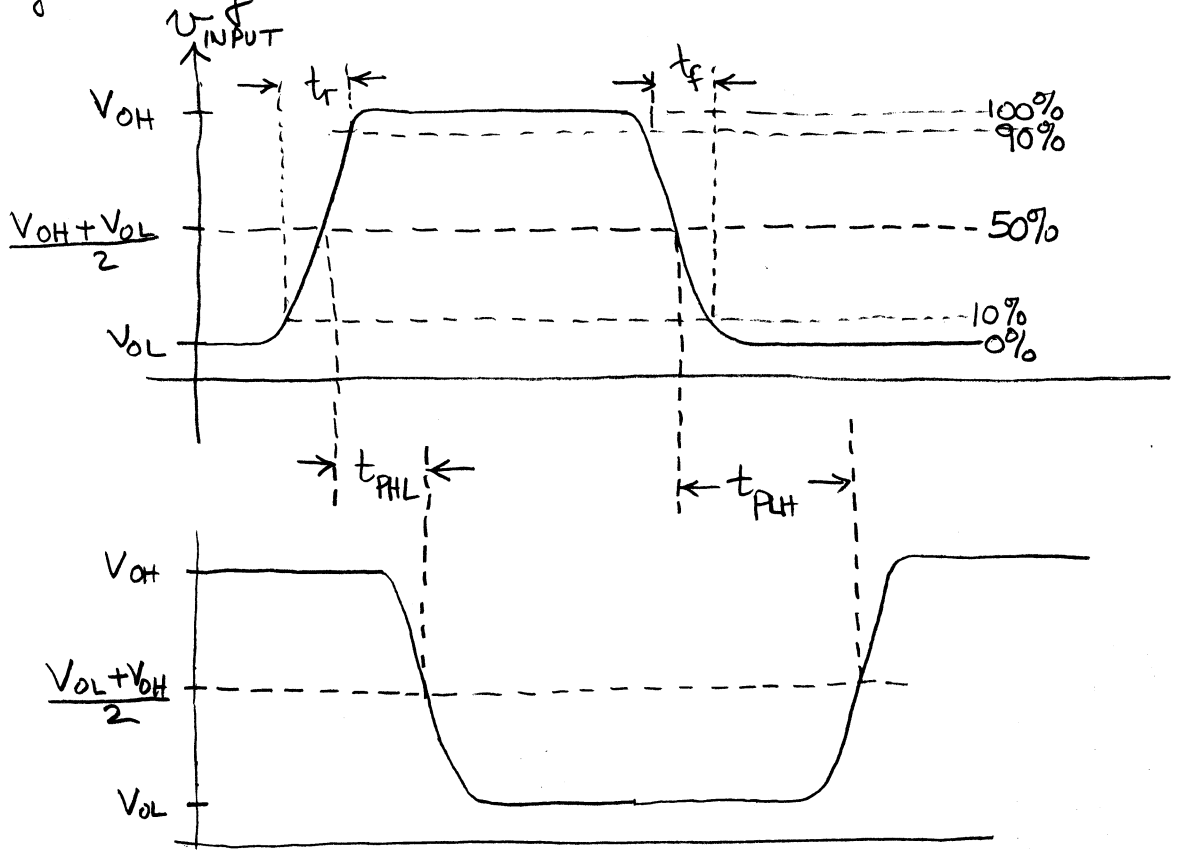
B $v_i > V_{to}$ of the NMOS but $v_i < \frac{V_{DD}}{2}$
NMOS in saturation region
PMOS in triode region

C → D PMOS load line and NMOS characteristics lie on a line. This is where the circuit switches rapidly from C → D.

E $\frac{V_{DD}}{2} \leq v_i \leq V_{DD} - V_{to}$ PMOS in saturation
NMOS in triode

F $v_i = V_{DD}$ PMOS cutoff
but NMOS highly ON

propagation delay

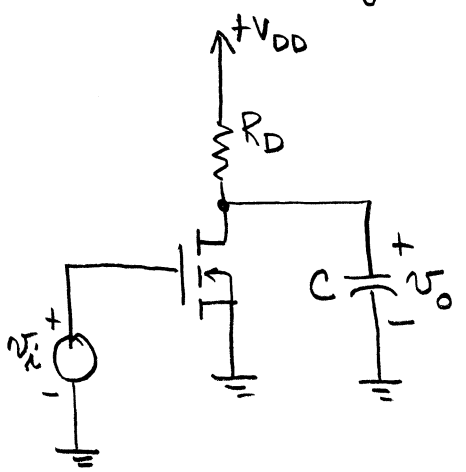



$t_{PHL}$ – propagation delay H→L output transition

$t_{PLH}$ – propagation delay L→H output transition

$$t_{PD} = \frac{t_{PHL} + t_{PLH}}{2}$$

can be calculated using the model

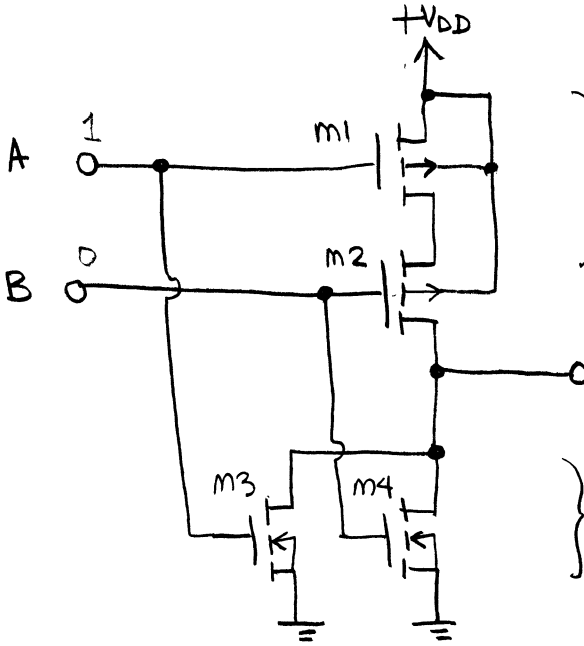



C is the load capacitance

On the order of 1 pf.

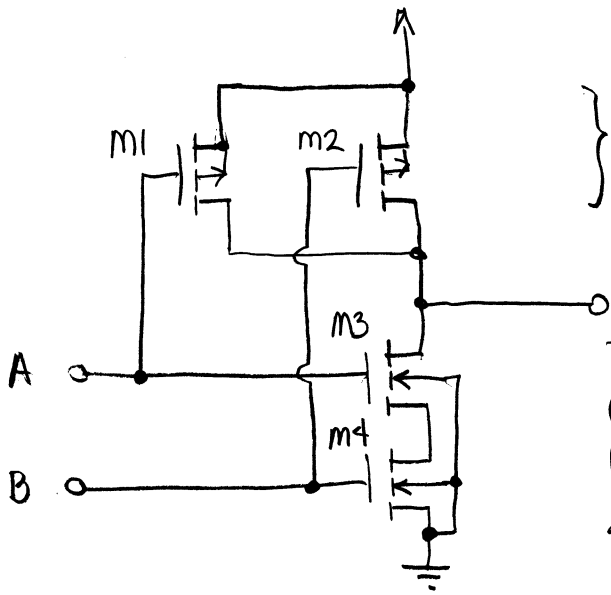
This leads into laplace transforms.

# cmos logic gates.




| A | B | A+B | $\overline{A+B}$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

output only high when A and B low so m1 & m2 are on




| A | B | AB | $\overline{AB}$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

output high whenever A or B = 0, but output low ONLY when both A and B are high.