**** 03/07/93 15:56:52 ********** Evaluation PSpice (Jan 1993) **********

CLASSROOM DEMO RLC CIRCUIT

**** CIRCUIT DESCRIPTION

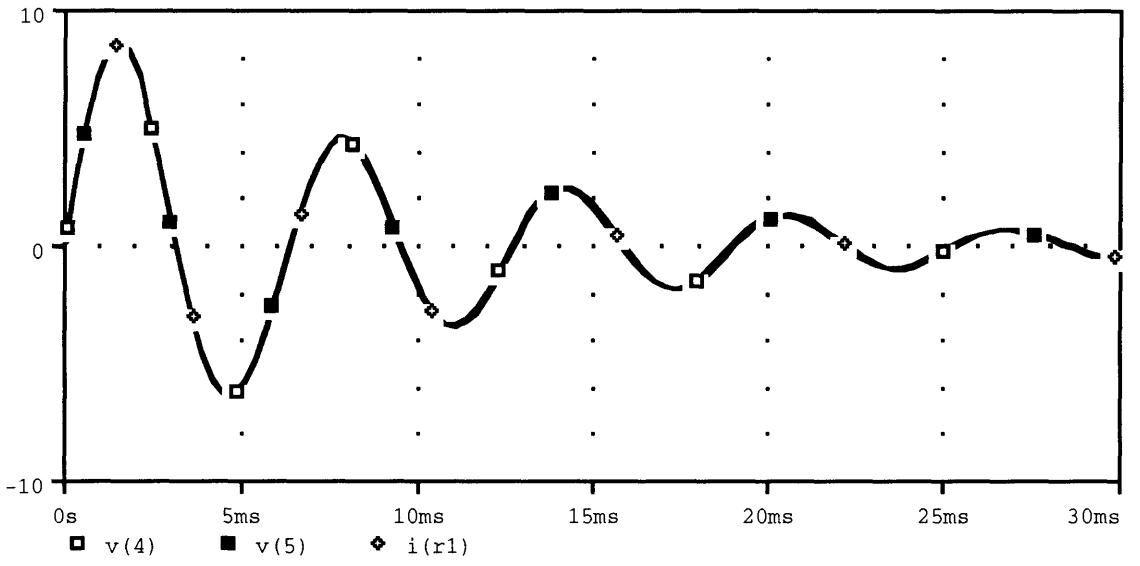
```
*******************************************************************************
Vs    1    0    PWL 0,0 1u,10
L1    1    2    1m
R1    2    3    0.2
C1    3    0    1000u

E1    4    0    LAPLACE {v(1)} = {((1000*s)/(s*s+200*s+1E6))}
R4    4    0    1

E30   5    0    value = {10.06*exp(-100*time)*sin(995*time)}
R30   5    0    1

.TRAN  30m 30m

.PROBE
.END
```

**** 03/07/93 15:56:52 ********** Evaluation PSpice (Jan 1993) **********

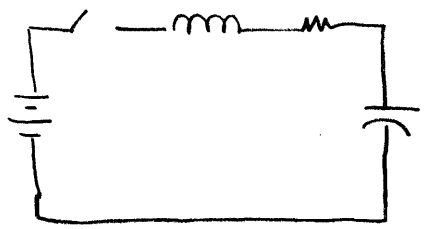
CLASSROOM DEMO RLC CIRCUIT

**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

```
*******************************************************************************
NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE

(  1)  0.0000 (  2)  0.0000 (  3)  0.0000 (  4)  0.0000

(  5)  0.0000


  VOLTAGE SOURCE CURRENTS
  NAME       CURRENT

  Vs         0.000E+00

  TOTAL POWER DISSIPATION  0.00E+00  WATTS

     JOB CONCLUDED

     TOTAL JOB TIME        31.63
```



"CLASSROOM DEMO RLC CIRCUIT" 03/07/93 15:56:52 27.0°



$$V(t)\,u(t) = L\frac{di}{dt} + Ri + \frac{1}{C}\int i\,dt$$

$$\frac{10}{s} = sLI(s) + RI(s) + \frac{I(s)}{sC}$$

$$I(s) = \frac{(10/s) - V(s)}{Ls + R + \frac{1}{sC}}$$

use transfer function

$$I(s) = V(s)\,\frac{1}{Ls + R + \frac{1}{sC}}$$

$$\frac{sC}{s^2LC + sRC + 1}$$

$$\frac{\frac{s}{L}}{s^2 + s\frac{R}{L} + \frac{1}{LC}} = \frac{s/L}{s^2 + s\frac{R}{L} + \frac{1}{LC}}$$

plotting transfer functions

voltage source
Ename +node -node LAPLACE{expression} = {transform_expression}.

current source
Gname.

result is to create a voltage at node which is expression multiplied by transform expression

typical use:

```
Vin  a  0  ac  1
Rin  a  0  1
E1   1  0  LAPLACE  {V(a)} = {10*s/((10+s)(1E4+s))}.
RE1  1  0  1
.AC  DEC  40  .01  100K.
.PROBE
.END.
```

**** 03/03/93 13:11:37 ********** Evaluation PSpice (Jan 1992) **********

Wheatstone bridge problem

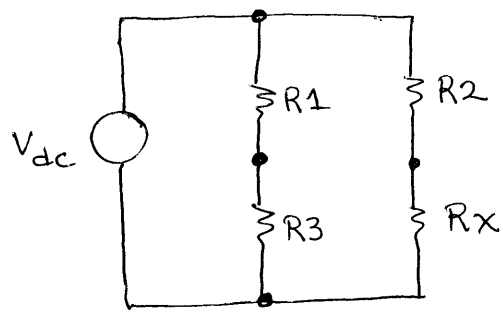
**** CIRCUIT DESCRIPTION

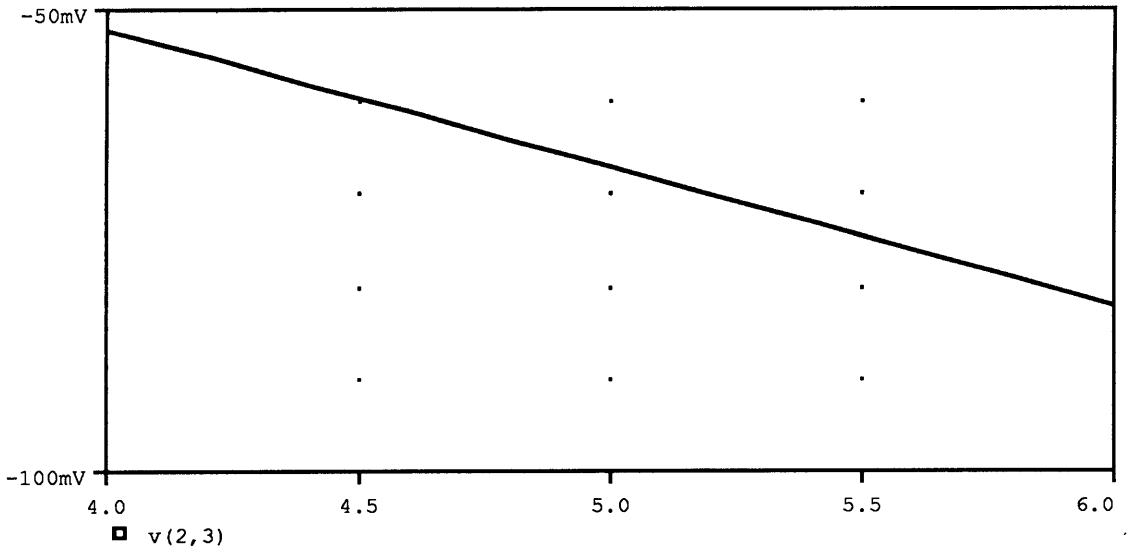
****

```
Vdc    1     0     15volts
R1     1     2     {Rratio}
R2     1     3     1000ohms
R3     2     0     500ohms
Rx     3     0     {R}     ;variable resistor Rx
.param  R=4.5
.param  Rratio=1000
.dc lin param R 4 6 0.2 param Rratio LIST 100000
.probe
.end
```

JOB CONCLUDED

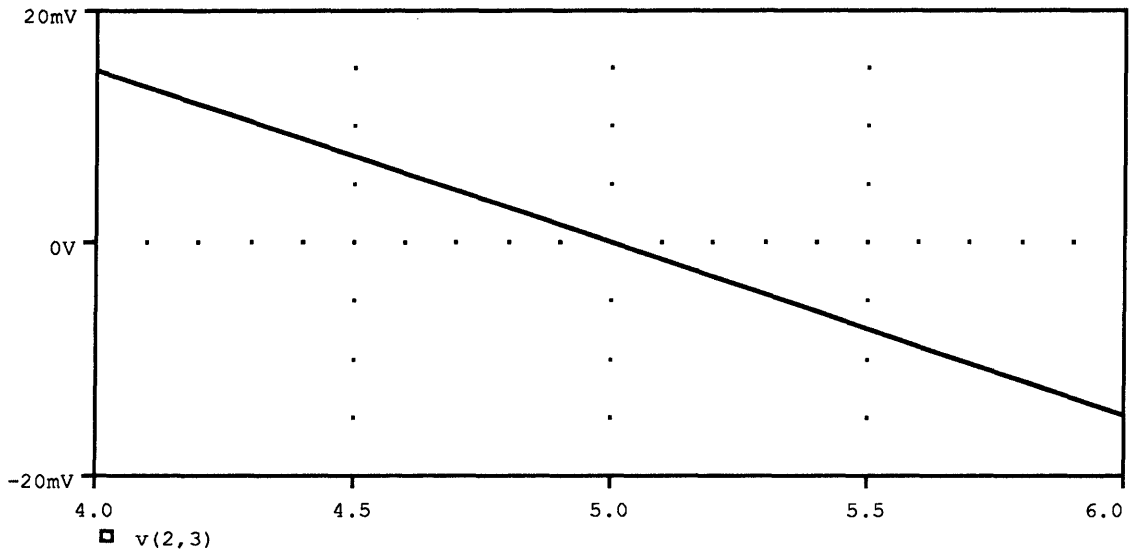
TOTAL JOB TIME .95





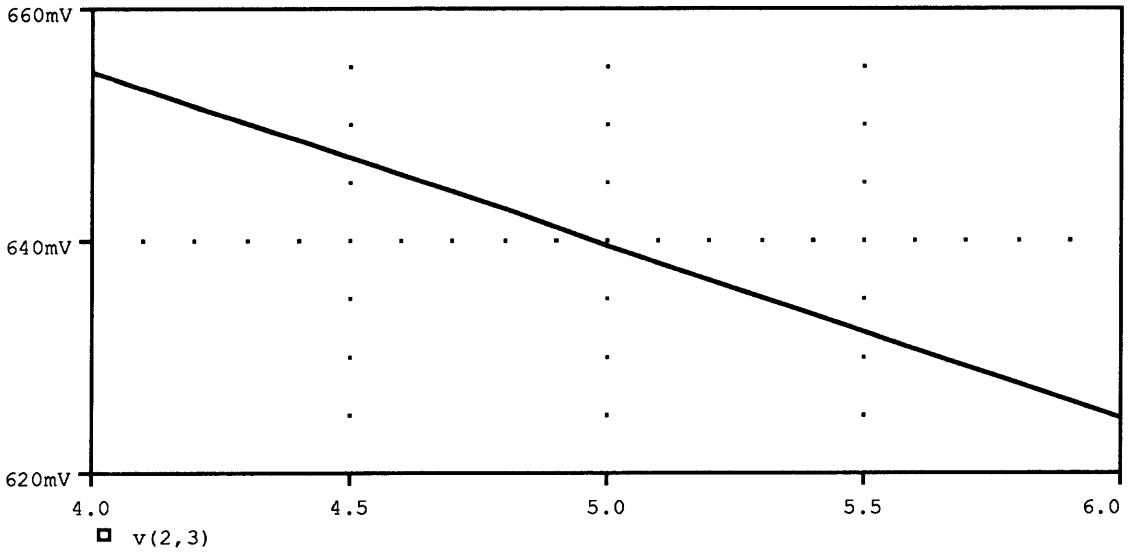
"Wheatstone bridge problem" 03/03/93 11:46:06 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

$R_{Ratio} = 1{,}000{,}000\ \Omega$



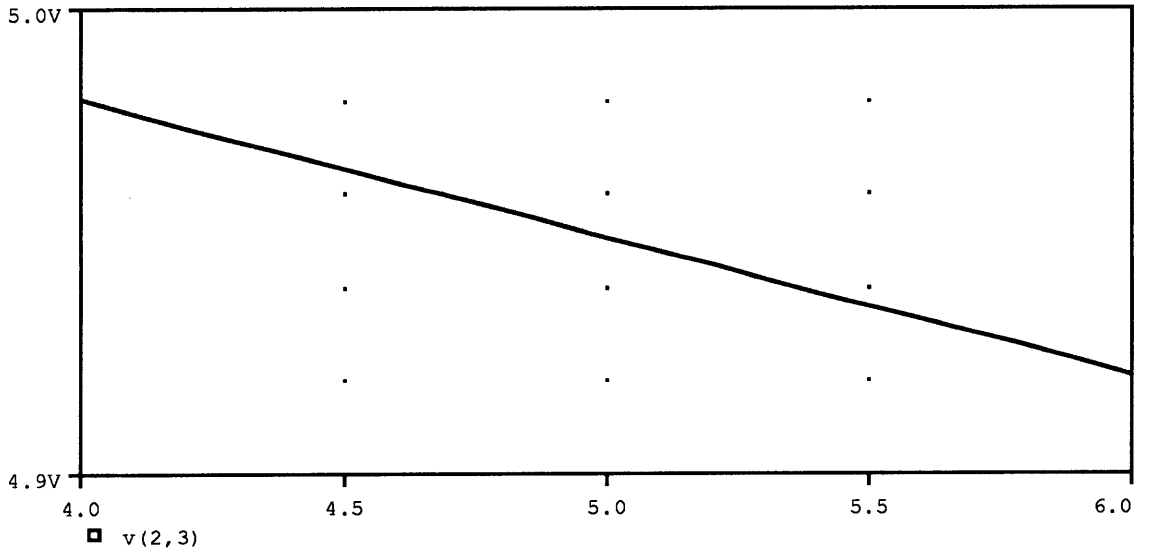
"Wheatstone bridge problem" 03/03/93 11:59:46 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

$R_{Ratio} = 100,000$



"Wheatstone bridge problem" 03/03/93 12:03:48 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

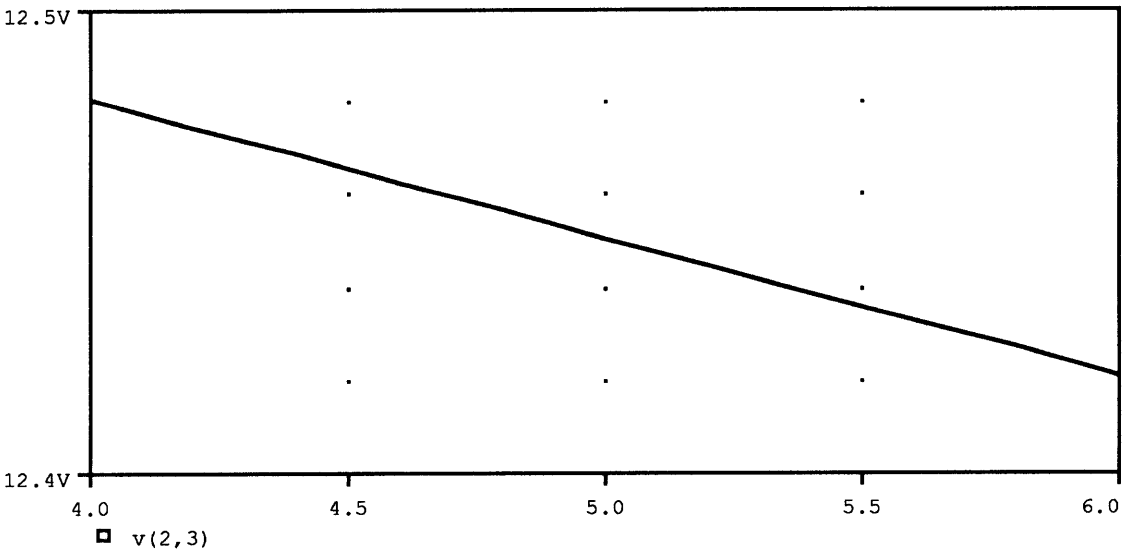
R = 10,000



"Wheatstone bridge problem" 03/03/93 12:05:48 27.0°

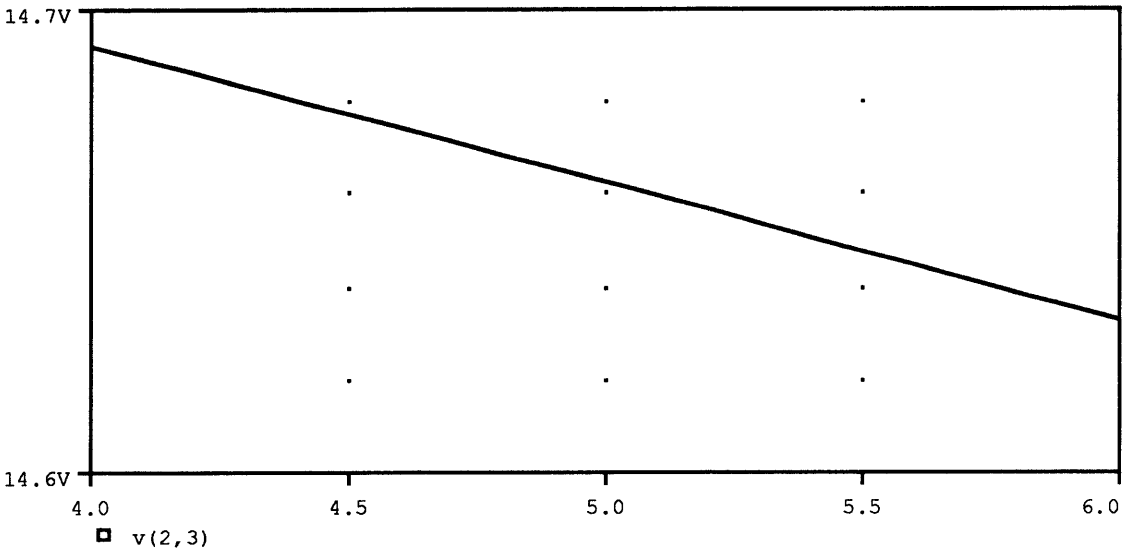
Evaluation Probe 5.1 © 1992 MicroSim Corp.

$R = 1,000$



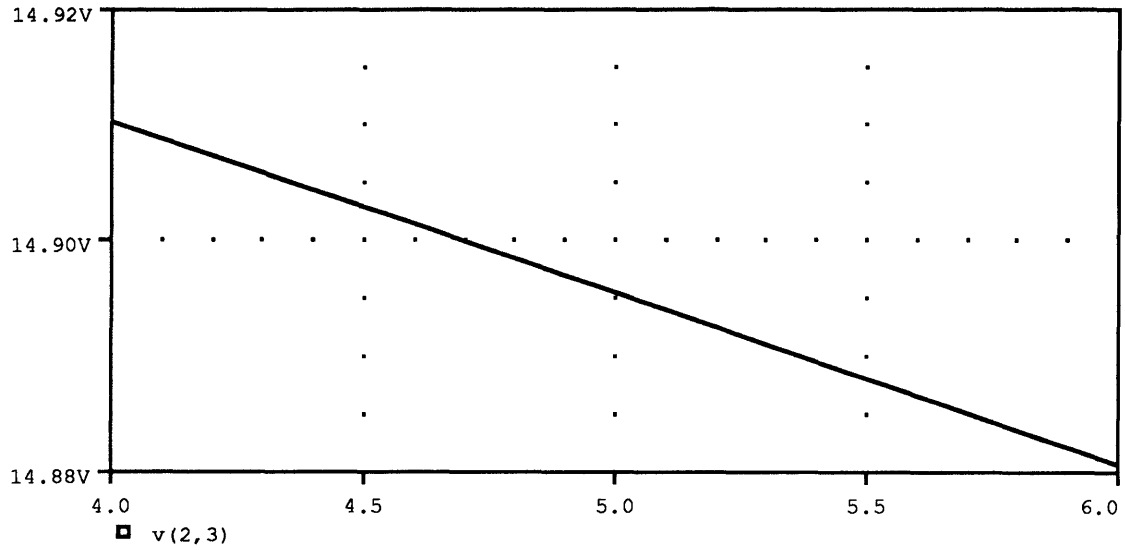
"Wheatstone bridge problem" 03/03/93 12:07:50 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

$R = 100\,\Omega$.



"Wheatstone bridge problem" 03/03/93 13:08:06 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

R = 10



"Wheatstone bridge problem" 03/03/93 13:09:45 27.0°
Evaluation Probe 5.1 © 1992 MicroSim Corp.

R = 1

**** 03/03/93 13:40:28 ********** Evaluation PSpice (Jan 1992) **********

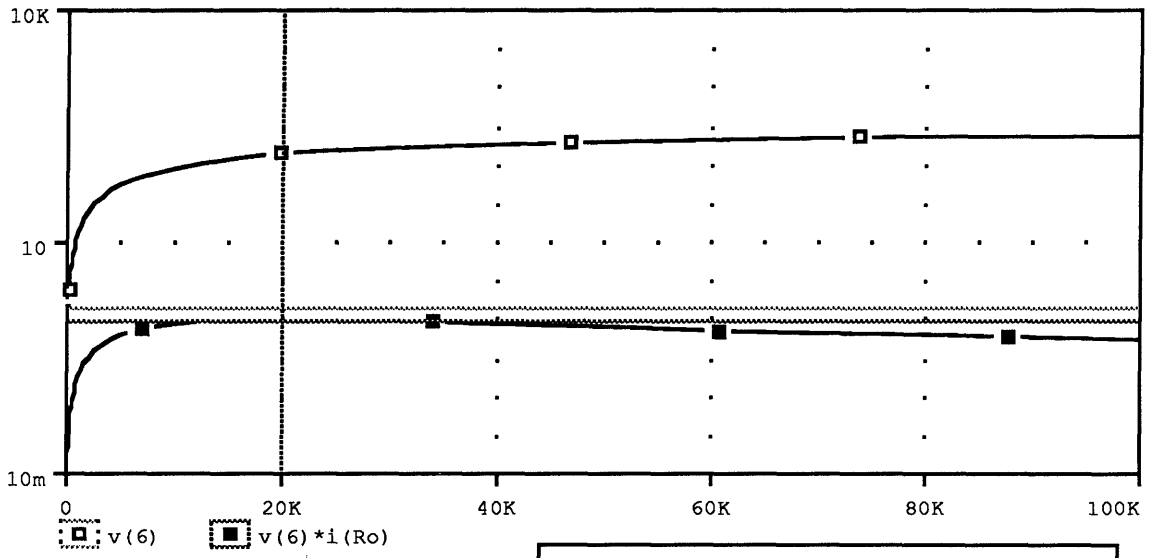
Problem 4.79 Nillson

**** CIRCUIT DESCRIPTION

```
********************************************************************************
Vdc    1     0     40volts
Vsens  2     5     ;sense voltage for controlled current source
Vload  4     6     ;sense voltage for power calculations
;      since no value is given for sense voltages they default to zero
F1     3     4     Vsens  30
;the direction is reversed because of the passive sign convention thru Vsens
R1     1     2     2k
R2     2     3     5k
R3     3     4     10k
R4     5     0     20k
R5     3     0     50k
R6     4     0     40k
Ro     6     0     {R}    ;variable load resistor
.param  R=5k
.dc dec param R 100 100k 10
.probe
.end
```

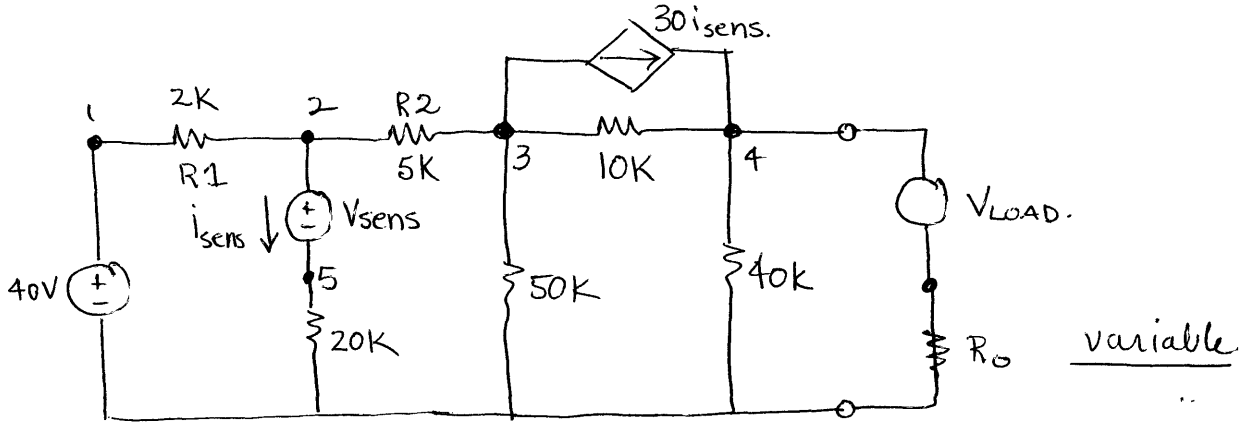
JOB CONCLUDED

TOTAL JOB TIME 1.78



C1 =	20.000K,	980.151m
C2 =	100.980,	1.4052
dif=	19.899K,	-425.014m

max 979.999 mW
@ 19.953k



100

EEAP 244 Homework

Name : Gabriel NG
Typed

Signature

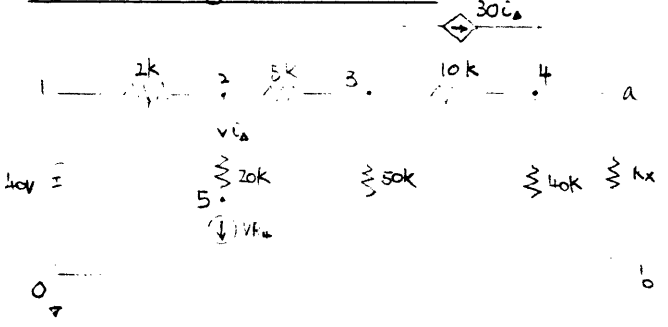
By signing this page I am indicating that this lab and the work described in this report is my own.

Title : Homework #1(Pspice program and analysis for problem 3-53 and 4-79)

Problem 4-79
Problem Statement : Find Ro in the circuit given in problem 4-79 that will maximize the power through Ro

Analysis : The above problem has been analyzed using pspice program by setting Ro to various values. Upon several trial and errors, maximum value of power through Ro occurs around 16000 to 24000 ohm. Further investigation is continued using a stepsize of 1000 ohm by running the pspice program again. The program text and the output file are shown below as necessary :

Schematic diagram of the circuit



Program text

```
* Circuit for problem 4.79 (homework #1)
* in this circuit, VR4 is used as a dummy voltage source
V0 1   0   dc  40
R1 1   2   2000
R2 2   3   5000
R3 3   4   10000
R4 2   5   20000
R5 3   0   50000
R6 4   0   40000
Rx 4   0   20000
VR4 5   0   dc    0
f1 3   4   VR4   30
.op
```

```
.probe
.end
```

Output file at (20000 ohm)

```
******* 03/04/93 ******* Evaluation PSpice (July 1989) ******* 18:55:56 *******

* Circuit for problem 4.79 (homework #1)

****     CIRCUIT DESCRIPTION

******************************************************************************

* in this circuit, VR4 is used as a dummy voltage source
V0  1    0    dc   40
R1  1    2    2000
R2  2    3    5000
R3  3    4    10000
R4  2    5    20000
R5  3    0    50000
R6  4    0    40000
Rx  4    0    20000
VR4 5    0    dc     0
f1  3    4    VR4    30
.op
.print dc V(3,4)
.probe
.end

******* 03/04/93 ******* Evaluation PSpice (July 1989) ******* 18:55:56 *******

* Circuit for problem 4.79 (homework #1)

****     SMALL SIGNAL BIAS SOLUTION      TEMPERATURE =   27.000 DEG C

******************************************************************************

NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE


(  1)   40.0000 (   2)   18.4000 (   3)  -31.0000 (   4)  140.0000

(   5)   0.0000

  VOLTAGE SOURCE CURRENTS
  NAME       CURRENT

  V0        -1.080E-02
  VR4        9.200E-04

  TOTAL POWER DISSIPATION   4.32E-01  WATTS
```

******* 03/04/93 ******* Evaluation PSpice (July 1989) ******* 18:55:56 *******

* Circuit for problem 4.79 (homework #1)

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** CURRENT-CONTROLLED CURRENT SOURCES

NAME f1
I-SOURCE 2.760E-02

JOB CONCLUDED

TOTAL JOB TIME 1.05

Graph : Shown in the following pages. Please consult those for references
Answers to the problem
(a) From the graph shown, maximum power through Ro occurs when Ro is 20000 ohm. Therefore, the value of Ro should be 20000 ohm.

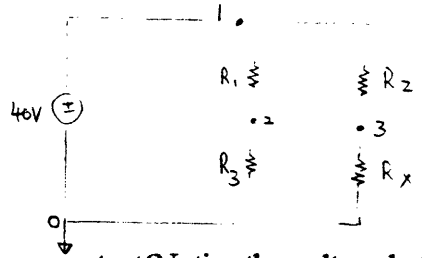
(b) From the graph shown, the corresponding power through Ro is 0.98 watt.

(c) percentage delivered to Ro is : 0.98/4.32 * 100% = 22.68%

Problem 3-53
Problem statement : Find the setting of R2/R1 so that the unknown resistor in the wheatstone bridge as shown can be measured up to four significant figures

Analysis : Problem mentioned above has been analyzed using pspice program as required. In the 1st one, The value of Rx is set between 4 to 5 ohm in each case. For each R2/R1 ratio to be investigated, the value of R3 is changed until the wheatstone bridge is in its equilibrium state, which means the voltage across node 2 and 3(or vice versa, depending on the sign) shown in the figure is zero.

Schematic diagram of the circuit



Program text(Notice the voltage between node 2 and 3 is zero)

```
* Circuit for problem 3.53(homework #1)
V1   1 0 dc   40
R1   1 2 1
R2   1 3 1000
R3   2 0 0.0045
Rx   3 0 4.5
.print dc v(3,2)
.probe
.end
```

Corresponding output file for the program shown above

******* 03/05/93 ******* Evaluation PSpice (July 1989) ******* 01:10:49 *******

* Circuit for problem 3.53(homework #1)

**** CIRCUIT DESCRIPTION

****

```
V1   1 0 dc   40
R1   1 2 1
R2   1 3 1000
R3   2 0 0.0045
Rx   3 0 4.5
.print dc v(3,2)
.probe
.end
******* 03/05/93 ******* Evaluation PSpice (July 1989) ******* 01:10:49 *******

* Circuit for problem 3.53(homework #1)


****    SMALL SIGNAL BIAS SOLUTION     TEMPERATURE =  27.000 DEG C

**********************************************************************

NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE

(  1)  40.0000 (  2)   .1792 (  3)   .1792

  VOLTAGE SOURCE CURRENTS
  NAME       CURRENT

  V1         -3.986E+01

  TOTAL POWER DISSIPATION  1.59E+03  WATTS

      JOB CONCLUDED

      TOTAL JOB TIME            .65
```

Answer to the problem : From the graph plotted, we can see if the R2/R1 ratio is 1000, 100, or 10, the resistance R3 needed is 0.0045, 0.045 and 0.45 respectively, which is not possible because the value of R3 has to lie between 1 to 11110 ohm. Furthermore, as the accuracy of R3 is less than 4, so for Rx to be measured up to four significant figures, the R2/R1 should have 4 significant figures. Therefore, the ratio R2/R1 should be 0.001 in order to satisfy the above two constraints.

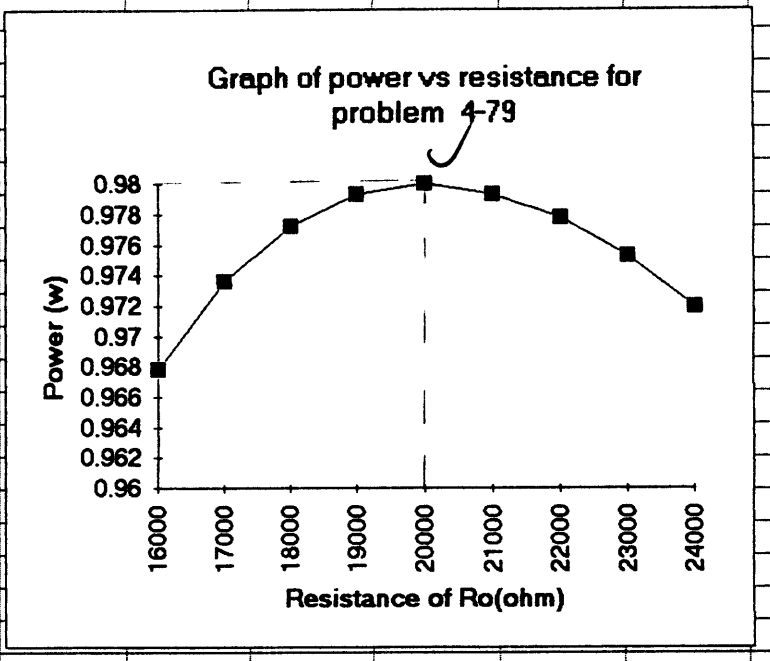
$R_x = R_2/R_1 \, R_3$

R_3 from graph I have at most 4 sig. figures

$\Rightarrow$ R_2/R_1 should have 4 sig figures so that R_x can be measured up to 4 sig. figures.

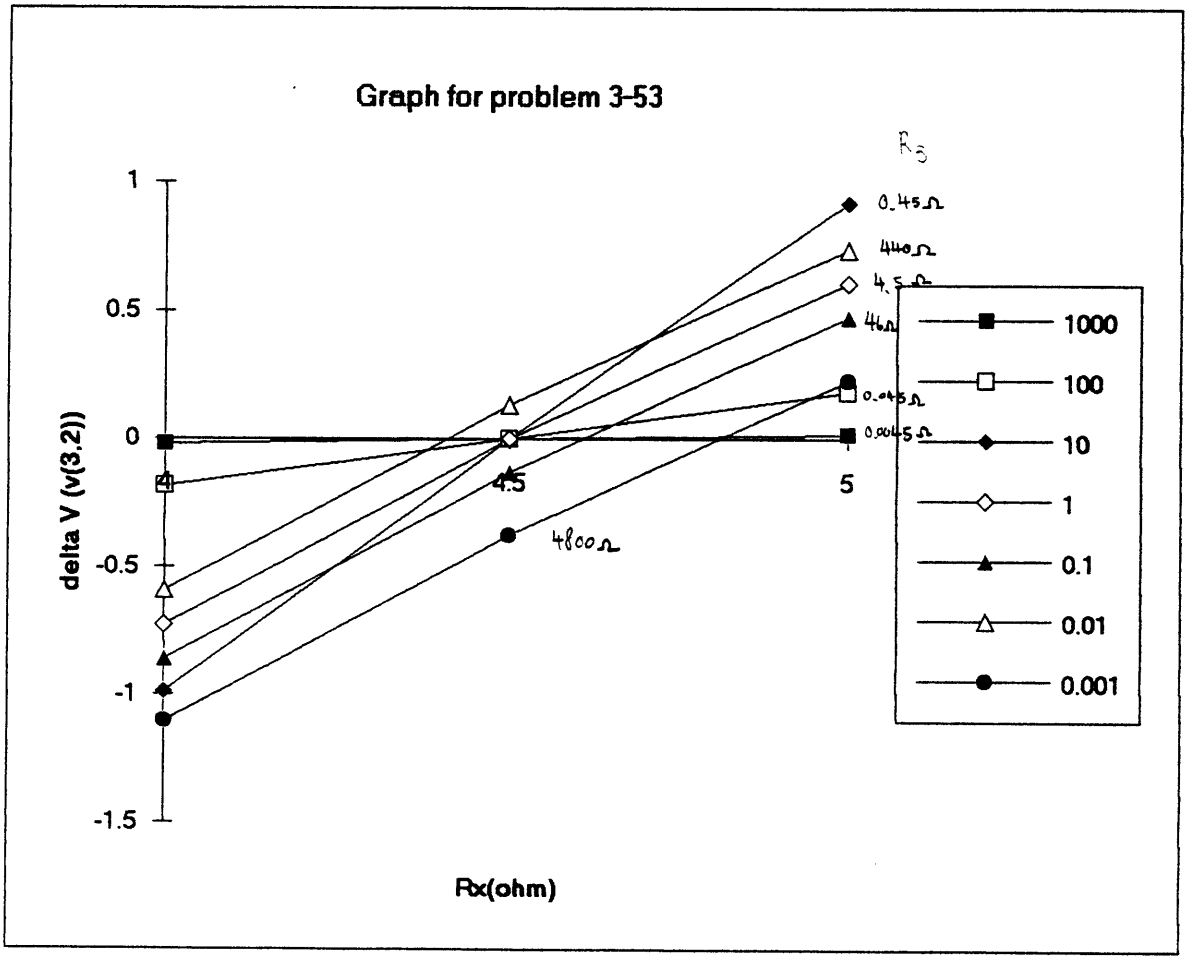
Graph for questions 4-79

Voltage	Ro	Power(w)
124.44	16000	0.967832
128.65	17000	0.973577
132.63	18000	0.97726
136.41	19000	0.97935
140.00	20000	0.98
143.41	21000	0.979353
146.67	22000	0.97782
149.77	23000	0.97526
152.73	24000	0.971936



Graph for problem 3-53

resistance	v(3,2) ratio	Rx 4	4.5	5
0.0045	1000	-0.0198	0	0.0198
0.045	100	-0.184	0	0.1823
0.45	10	-0.985	0	0.919
4.5	1	-0.727	0	0.606
4.6	0.1	-0.857	-0.13	0.476
440	0.01	-0.593	0.134	0.74
4800	0.001	-1.103	-0.376	0.23



Remark: R_s is adjusted to different values for different ratio.

Graph for problem 3-53

delta V ratio	Rx(ohm) 4	4.5	5
1000	39.8316	39.8118	39.792
100	38.4525	38.2685	38.0862
10	28.562	27.577	26.658
1	7.991	7.264	6.658
0.1	0.967	0.861	0.775
0.01	0.091	0.0808	0.071
0.001	0.001	0	-0.001

Method 2 :

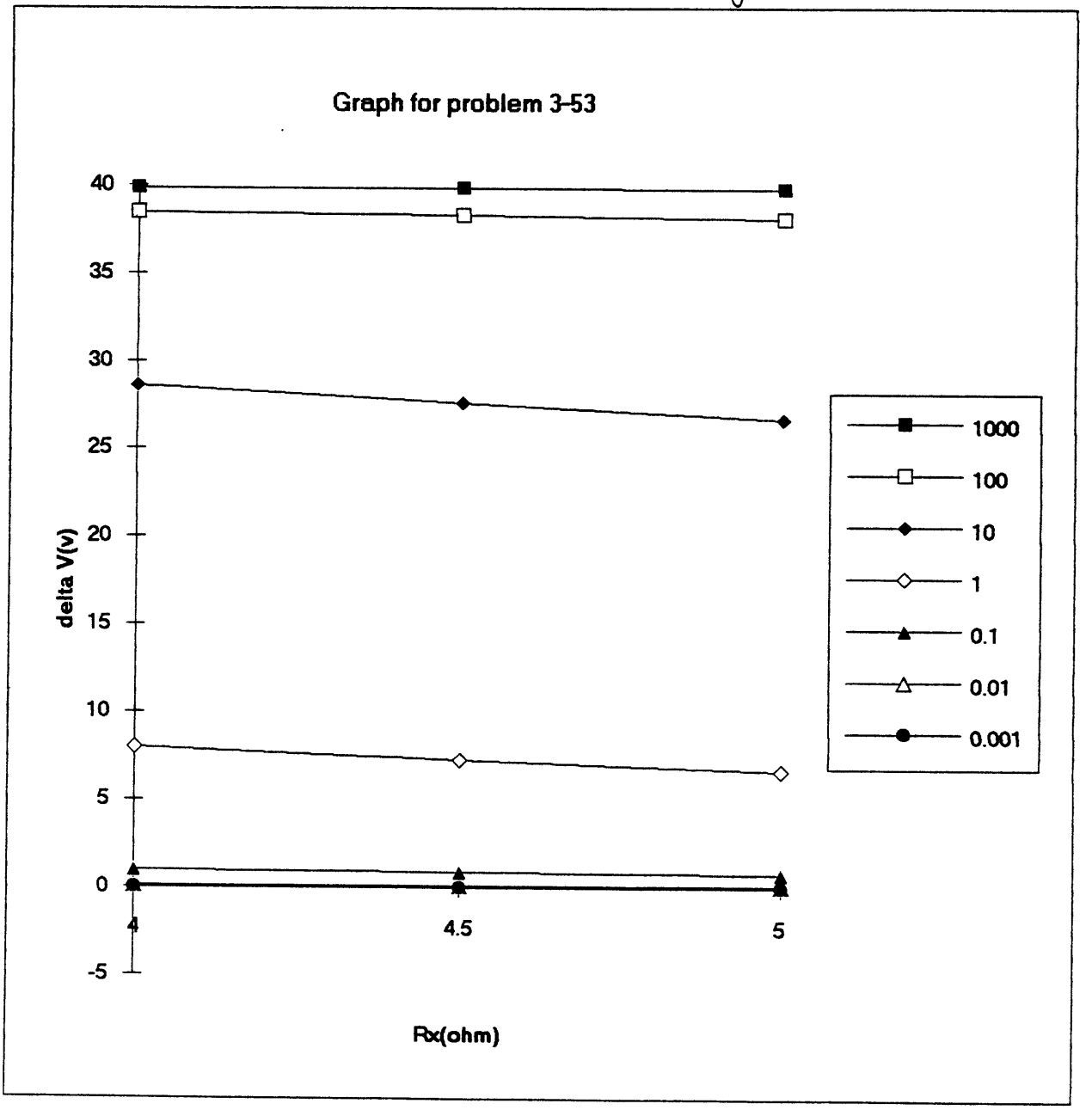
$4 \le R_3(0.001) \le 5$

$\Rightarrow 4000 \le R_3 \le 5000$

Choose $R_3 = 4500\ \Omega$

plot the graph

From the graph, equilibrium condition is attained when ratio is 0.001 only. $\Rightarrow R_2/R_1$ should be 0.001



100

Nice Work

Peter Kreymerman
EEAP 244
Pspice (WheatStone Bridge)
3.53

The enclosed data table and graph demonstrate the characteristics of a WheatStone Bridge simulated with Pspice. The WheatStone circuit is balanced when the voltage difference across the middle nodes is zero and therefore the equation R2/R1=Rx/R3 must hold true. The 8th program listing and following results demonstrate this perfectly.

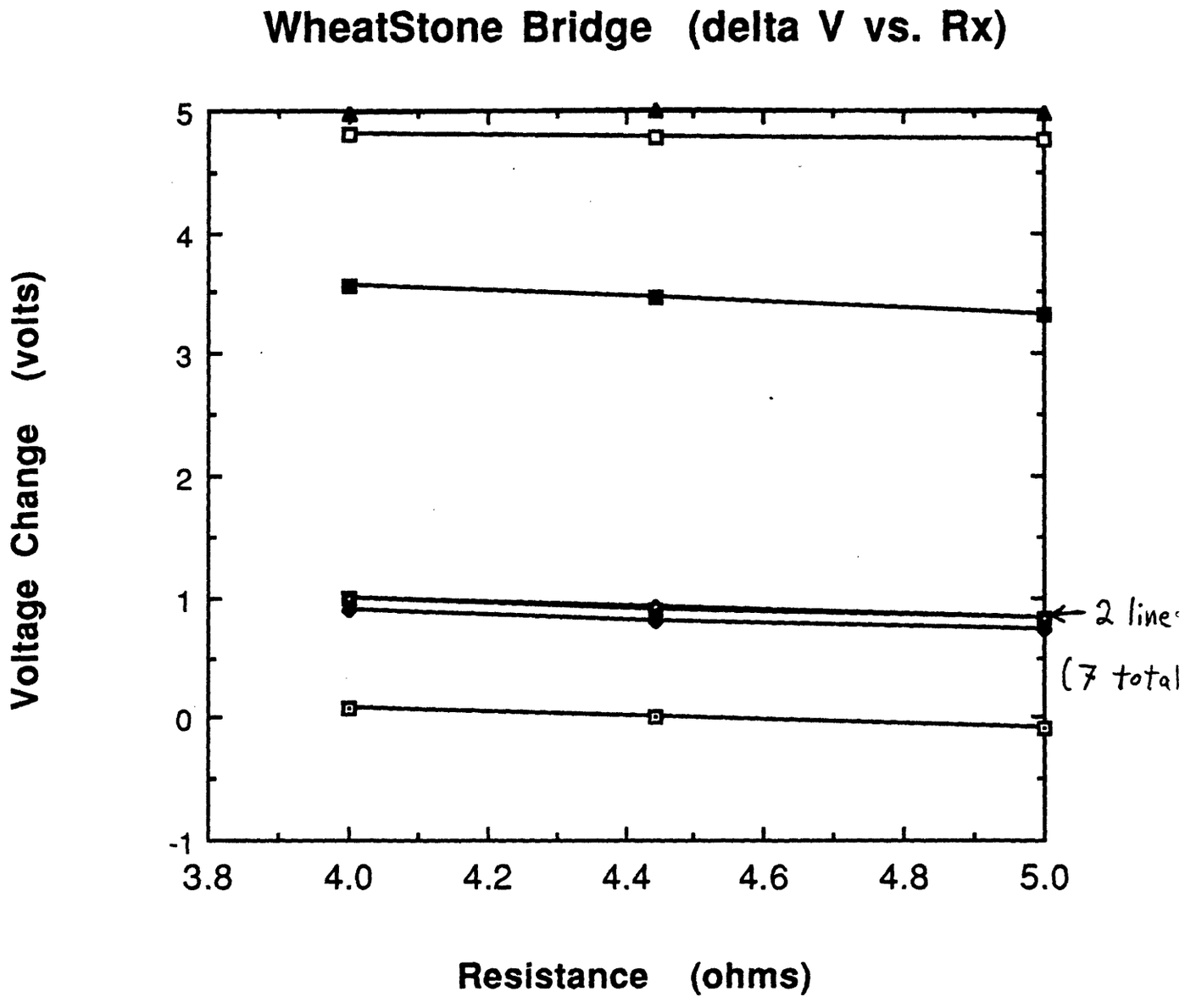
The problem required us to determine the value of the ratio R2/R1 (.001, .01, .1, 1, 10, 100, or 1000) so that Rx was between 4 and 5 ohms and was four significant digits. R3 is a dail-a-ohm which ranges from 1 to 11,110 ohms in incriments of 1. It was important to pick the proper R3 to satisfy the stated conditions. I chose R3 to be 4444 ohms, but anything between the 4000 to 5000 range (with 4 significant digits) is fine. By using this value for R3 and .001 for the R2/R1 ration I calculated Rx (Rx=4.444 ohms) to four significant digits and within the specified range. If any other R2/R1 ratio was used, Rx would have less then 4 significant digits.

In conclusion, the data table and graph demonstrate that the WheatStone Bridge is indeed balanced when R3=4444 ohms, Rx=4.444 ohms, and R2/R1=.001, because these values show that the change in voltage across the middle nodes is zero. ✓

50

Data_3.53 Thu, Mar 4, 1993 10:27 PM

	Rx (ohm)	Node 2 (V)	Node 3 (V)	Voltage Change
1	4.000	4.0816	4.0000	0.082
2	4.000	4.8900	4.0000	0.890
3	4.000	4.9888	4.0000	0.989
4	4.000	4.9989	4.0000	0.999
5	4.000	4.9989	1.4286	3.570
6	4.000	4.9989	0.1923	4.807
7	4.000	4.9989	0.0199	4.979
8	4.444	4.0816	4.0816	0.000
9	4.444	4.8900	4.0816	0.808
10	4.444	4.9888	4.0816	0.907
11	4.444	4.9989	4.0816	0.917
12	4.444	4.9989	1.5384	3.461
13	4.444	4.9989	0.2127	4.786
14	4.444	4.9989	0.0221	4.977
15	5.000	4.0816	4.1667	-0.085
16	5.000	4.8900	4.1667	0.723
17	5.000	4.9888	4.1667	0.822
18	5.000	4.9989	4.1667	0.832
19	5.000	4.9989	1.6667	3.332
20	5.000	4.9989	0.2381	4.761
21	5.000	4.9989	0.0249	4.974


WheatStone Bridge (delta V vs. Rx)
Voltage Change (volts)
5
4
3
2
1
0
-1
3.8
4.0
4.2
4.4
4.6
4.8
5.0
Resistance (ohms)
2 lines
(7 total

Peter Kreymerman
EEAP 244
Pspice (Power Transfer)
4.79

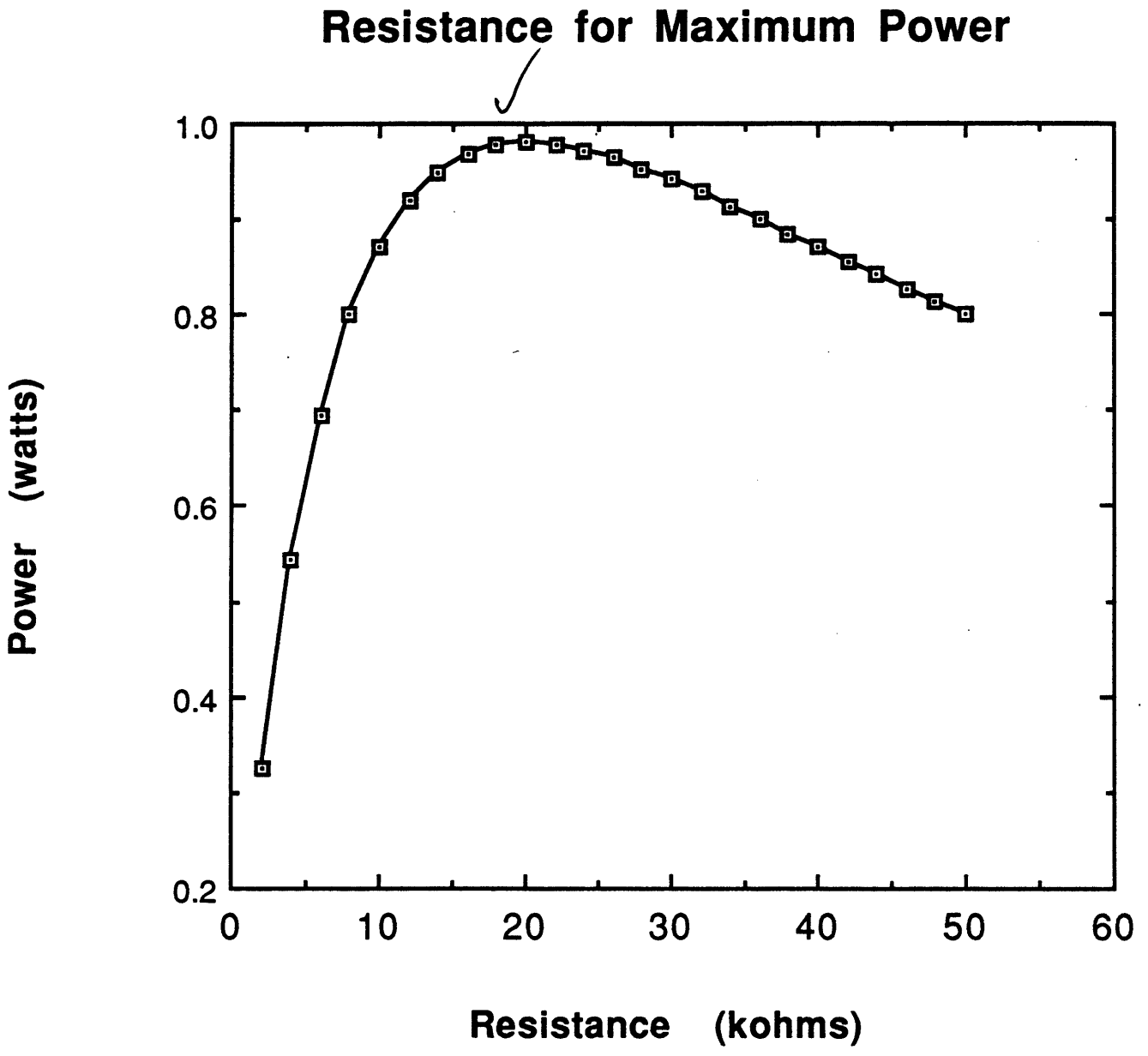
a) The maximum power transferred to the variable resistor (Ro) came when Ro=20 kohms. The data table and graphical representation proved that this value is true. Ro can also be determined by calculating the Thevenin Resistance of the Circuit.

b) The maximum power delivered to Ro was .980 watts and this value can be proven by examining the data table and graph.

c) The percentage of total power which is in Ro is about 19 percent. This value was determined by evaluating the sources (using KCL and KVL) and then finding the power delivered by each (P=VI). The power delivered to Ro was divided by the total power (from the sources) and multiplied by 100, getting the percentage which we desired.

Data_4.79 Thu, Mar 4, 1993 11:23 PM

	Resistance	Voltage (V)	Current (A)	Power (watts)
1	2.000	25.455	0.01273	0.324
2	4.000	46.667	0.01167	0.545
3	6.000	64.610	0.01077	0.696
4	8.000	80.000	0.01000	0.800
5	10.000	93.333	0.00933	0.871
6	12.000	105.000	0.00875	0.919
7	14.000	115.290	0.00823	0.949
8	16.000	124.440	0.00778	0.968
9	18.000	132.630	0.00737	0.977
10	20.000	140.000	0.00700	0.980
11	22.000	146.670	0.00667	0.978
12	24.000	152.730	0.00636	0.972
13	26.000	158.260	0.00609	0.963
14	28.000	163.330	0.00583	0.953
15	30.000	168.000	0.00560	0.941
16	32.000	172.310	0.00538	0.928
17	34.000	176.300	0.00519	0.914
18	36.000	180.000	0.00500	0.900
19	38.000	183.450	0.00483	0.886
20	40.000	186.670	0.00467	0.871
21	42.000	189.680	0.00452	0.857
22	44.000	192.500	0.00438	0.842
23	46.000	195.150	0.00424	0.828
24	48.000	197.650	0.00412	0.814
25	50.000	200.000	0.00400	0.800


Resistance for Maximum Power
1.0
0.8
0.6
0.4
0.2
Power (watts)
0
10
20
30
40
50
60
Resistance (kohms)

```
Power Transfer
*Sources
Vs 1 0 DC 40
F1 3 4 V2 30
*Dummy Sources
V2 2 5 DC 0
V3 4 6 DC 0
*Elements
R1 5 0 20000
R2 3 0 50000
R3 4 0 40000
R4 1 2 2000
R5 2 3 5000
R6 3 4 10000
R0 6 0 Rmod 1
.Model Rmod Res(R=1)
.Step Lin Res Rmod(R) 2000, 50000, 2000
*Output
.Print DC V(4), I(V3)
.END
```

```
****     CURRENT STEP                RMOD R =    2.0000E+03
**********************************************************************
*
(    1)   40.0000 (    2)   13.8180 (    3)  -48.1820 (    4)   25.4550

  VOLTAGE SOURCE CURRENT
    V3          1.273E-02

    TOTAL POWER DISSIPATION   5.24E-01  WATTS


****     CURRENT STEP                RMOD R =    4.0000E+03
**********************************************************************
*
'    1)   40.0000 (    2)   14.6670 (    3)  -45.0000 (    4)   46.6670
```

EEAP 244
PSPICE - ASSIGNMENT

NAME: Anand C. Patel
Signature: Anand C Patel
SS # : 216-06-5433

ASSIGNMENT #1: The objective of this assignment is to understand the construction and principle of the Wheatstone Bridge using the Circuit Simulation Software PSpice. The main objective of the assignment is to select a particular ratio R2/R1 from the given seven ratios so that the unknown resistor Rx that has a value between 4Ω and 5Ω can be measured upto four significant digits.

ASSIGNMENT #2: The objective of this assignment is to understand the concept of power development and power consumption in a circuit. The main objective is to analyze how the change in value of a load resistor affects the amount of power that resistor draws from the source circuit.

ASSIGNMENT #1

AIM: The objective of this assignment is to understand the construction and principle of the Wheatstone Bridge using the Circuit Simulation Software PSpice. The main objective of the assignment is to select a particular ratio R2/R1 from the given seven ratios so that the unknown resistor Rx that has a value between 4Ω and 5Ω can be measured upto four significant digits. Then finally plot the graphs ***Rx .vs. ΔV*** for each of the seven ratios.

GIVEN DATA:

1) The ratios R2/R1 can have the values 0.001, 0.01, 0.1, 1, 10, 100, 1000.
2) R3 can have a value between 1 to 11,110Ω in increments of 1Ω.
3) Rx has a value between 4Ω and 5Ω.

CIRCUIT DIAGRAM:

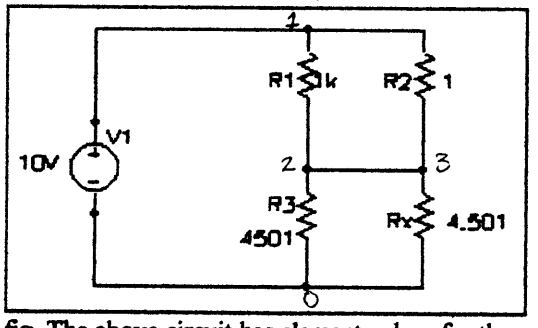


fig. The above circuit has element values for the ratio R2/R1=0.001

PRINCIPLE OF THE WHEATSTONE BRIDGE:

The principle of the Wheatstone Bridge is that the ratio (R2 / R1) = (Rx / R3) is true only when the voltage at nodes 2 and 3 is the same, ie, the bridge is balanced. Thus in such a case if R1, R2 and R3 are known the value of the unknown resistor Rx can be found easily using the ratio.

OBSERVATIONS:

R1 remains constant for all ratios = 1000Ω
R3 remains constant for all ratios = 4501Ω

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 0.001			
R2 = 1Ω			
8.1821	8.0048	0.1773	4.012
8.1821	8.1821	0	4.501
8.1821	8.3547	0.1726	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 0.01			
R2 = 10Ω			
8.1821	2.8633	5.3188	4.012
8.1821	3.1039	5.0782	4.501
8.1821	3.3678	4.8143	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 0.1			
R2 = 100Ω			
8.1821	0.3857	7.7964	4.012
8.1821	0.4307	7.7514	4.501
8.1821	0.4833	7.6988	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 1.0			
R2 = 1000Ω			
8.1821	0.04	8.1421	4.012
8.1821	0.0448	8.1373	4.501
8.1821	0.0505	8.1316	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 10.0			
R2 = 10000Ω			
8.1821	0.004	8.1781	4.012
8.1821	0.0045	8.1776	4.501
8.1821	0.0051	8.177	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 100.0			
R2 = 100000Ω			
8.1821	0.0004012	8.1816988	4.012
8.1821	0.0004501	8.1816499	4.501
8.1821	0.0005078	8.1815922	5.078

V(2) Volts	V(3) Volts	ΔV (Volts)	Rx (Ω)
R2 / R1 = 1000.0			
R2 = 1000000Ω			
8.1821	0.00004012	8.18205988	4.012
8.1821	0.00004501	8.18205499	4.501
8.1821	0.00005078	8.18204922	5.078

SOLUTION:

From the above observations we see that Rx is measured to four significant digits when the ratio R2 / R1 has the value 0.001. For this ratio Rx has the value 4.501Ω and therefore it also satisfies the principle of the wheatstone bridge, ie, the wheatstone bridge is balanced and ΔV is zero.

Now, I chose R3 to be equal to 4501Ω for the following reason :-

To get the value of Rx to be upto 4 significant digits and also to be between 4Ω and 5Ω, R3 can have any value between 4001Ω, 4101Ω, ..., 4551Ω, ..., 4667Ω, ..., 4999Ω. Another reason for this limit over R3 is that it's value can not exceed 11,110Ω and has to be a whole number since it can be varied in increments of 1Ω only.

```
PSpice Problem 3.53-FOR THE RATIO R2/R1=0.001
Vs       1 0      DC       10
R1       1 2      1000
R2       1 3      1
R3       2 0      4501
RX       3 0      4.012
.END
PSpice Problem 3.53-FOR THE RATIO R2/R1=0.001
Vs       1 0      DC       10
R1       1 2      1000
R2       1 3      1
R3       2 0      4501
RX       3 0      4.501
.END
PSpice Problem 3.53-FOR THE RATIO R2/R1=0.001
Vs       1 0      DC       10
R1       1 2      1000
R2       1 3      1
R3       2 0      4501
RX       3 0      5.078
.END
```

ASSIGNMENT #2

AIM: The objective of this assignment is to understand the concept of power development and power consumption in a circuit. The main objective is to analyze how the change in value of a load resistor affects the amount of power that resistor draws from the source circuit. Then plot a graph of ***Ro .vs. Power[Ro]***.

CIRCUIT DIAGRAM:

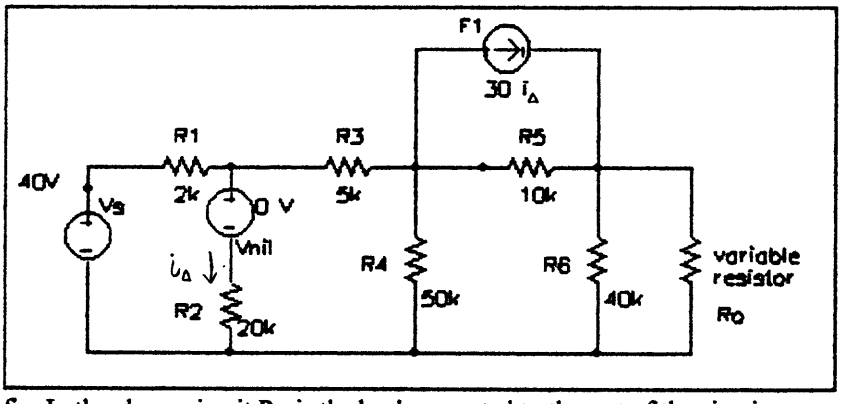


fig. In the above circuit Ro is the load connected to the rest of the circuit.

THEORY:

The following formula for Power is used in the calculations

Power = V*I = (V*V) / R = I*I*R

In the circuit on calculation it is found that the voltage source Vs and current source F1 produce power while all the resistors consume power. The resistance Ro acts like a load to the entire circuit. It is also true that the resistance Ro consumes the maximum power from the circuit, when Ro is equal to the Thevenin Equivalent of the circuit. Therefore if we know the current flowing through Ro or the voltage across its terminals we can calculate the power it will consume from the circuit using one of the above formulas.

OBSERVATIONS:

Ro (Ω)	I(Ro) amp.	Power(Ro) watts	% consumed
10000	0.00933	0.870489	8.090
10500	0.00918	0.8848602	8.224
11000	0.009032	0.897347264	8.340
11500	0.008889	0.908664692	8.445
12000	0.00875	0.91875	8.539
12500	0.008615	0.927727813	8.622
13000	0.008485	0.935937925	8.698
13500	0.008358	0.943058214	8.764
14000	0.008235	0.94941315	8.824
14500	0.008116	0.955107112	8.876
15000	0.008	0.96	8.922
15500	0.007887	0.96417392	8.961
16000	0.007778	0.967956544	8.996
16500	0.007671	0.970929977	9.024
17000	0.007568	0.973668608	9.049
17500	0.007467	0.975731558	9.068
18000	0.007368	0.977173632	9.082
18500	0.007273	0.978585787	9.095
19000	0.007179	0.979222779	9.101
19500	0.007089	0.97995146	9.107
20000	0.007	0.98	9.108
20500	0.006914	0.979969618	9.108
21000	0.006829	0.979340061	9.102
21500	0.006747	0.978723194	9.096
22000	0.006667	0.977875558	9.088
22500	0.006588	0.97653924	9.076
23000	0.006512	0.975341312	9.065
23500	0.006437	0.973721772	9.049
24000	0.006364	0.972011904	9.034
24500	0.006292	0.969936968	9.014
25000	0.006222	0.9678321	8.995

*(**** continued ****)*

25500	0.006154	0.965728758	8.975
26000	0.006087	0.963340794	8.953
26500	0.006022	0.961008826	8.931
27000	0.005957	0.958117923	8.904
27500	0.005895	0.955653188	8.882
28000	0.005833	0.952668892	8.854
28500	0.005773	0.949834577	8.827
29000	0.005714	0.946844084	8.800
29500	0.005657	0.944048646	8.774
30000	0.0056	0.9408	8.743

CALCULATIONS:

Total power developed in the circuit = P(Vs) + P(F1)
= 0.008 * 40 + 30 * 0.0012 * (280+10)
= 10.76 Watts

Sample Calculation:

Consider Ro = 20KΩ

Power delivered to Ro = 0.98 Watts

The percentage of the total power developed in the circuit
that is delivered to Ro = (0.98 * 100) / 10.76
= 9.108 %

TOTAL POWER X ?

RESULTS:

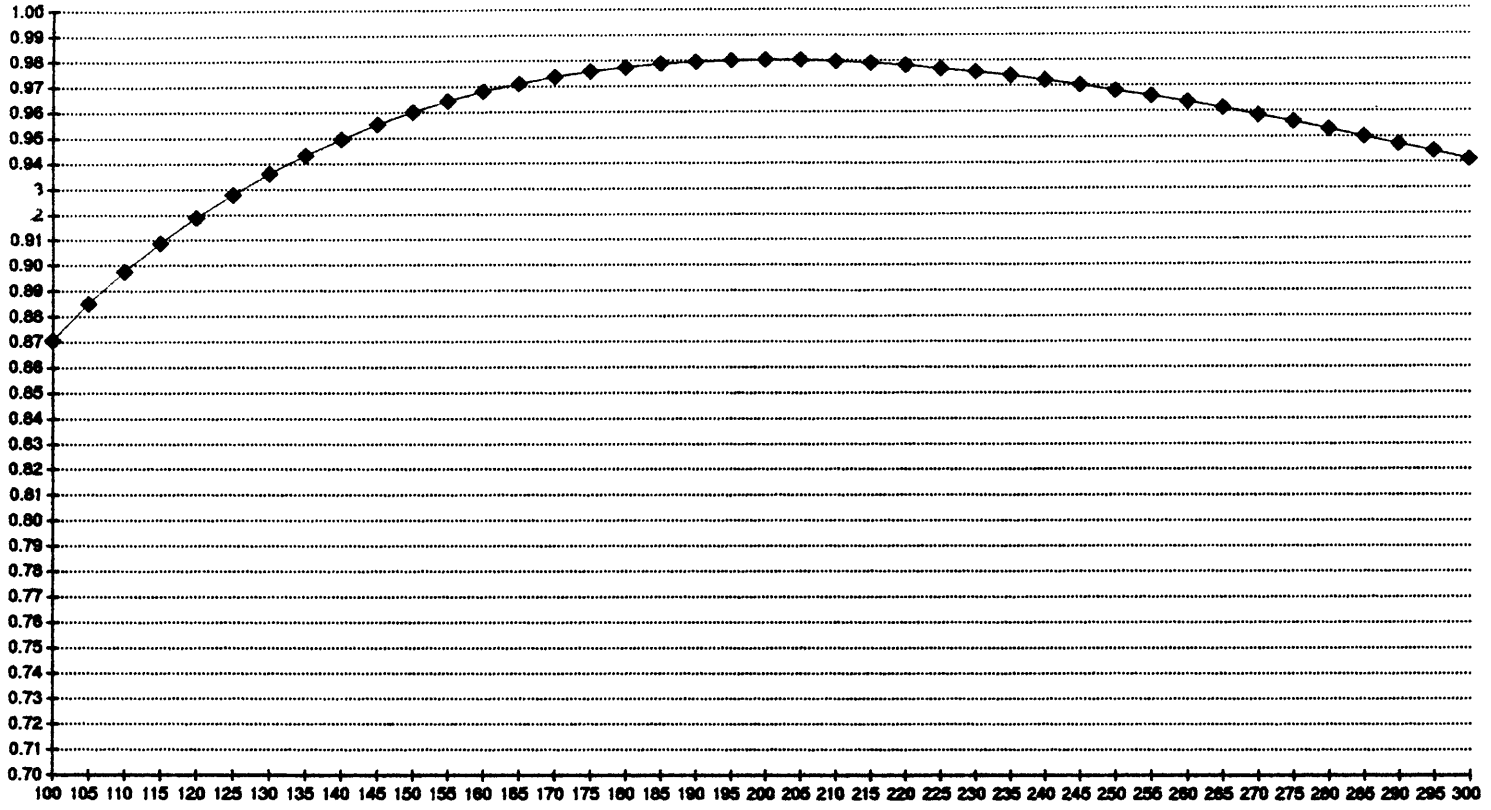
A). The value of Ro for which maximum power is transferred to it = **20KΩ**
This value of Ro is also the Thevenin Equivalent of the circuit.

B). The maximum power delivered to Ro by the circuit = **0.98 Watts**

C). The percentage of the total power developed in the circuit
that is delivered to Ro = **9.108 %**

On plotting *Ro .vs. Power[Ro]* we see from the curve that, the power being transferred from the circuit to Ro increases until Ro reaches the Thevenin Equivalent of the circuit. There after the power being transferred to Ro from the circuit begins to drop.

```
Problem No. 4.79; PSpice Homework-1, POWER RELATED
Vs 1 0 DC 40
Vnil 2 3 DC 0
R1 1 2 2K
R2 3 0 20K
R3 2 4 5K
R4 4 0 50K
R5 4 5 10K
R6 5 0 40K
Ro 5 0 RMOD 1
F1 4 5 Vnil 30
.MODEL RMOD RES(R=1)
.STEP LIN RES RMOD(R) 10000,30000,500
.DC Vs 0 40 40
.PRINT DC I(Ro), V(5)
.PROBE
.END
```


1.00
0.99
0.98
0.97
0.96
0.95
0.94
3
.2
0.91
0.90
0.89
0.88
0.87
0.86
0.85
0.84
0.83
0.82
0.81
0.80
0.79
0.78
0.77
0.76
0.75
0.74
0.73
0.72
0.71
0.70
100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300

EEAP 244

P-SPICE Homework #1

3-53, 4-79

David Sarafian

3-5-93

Problem 3-53

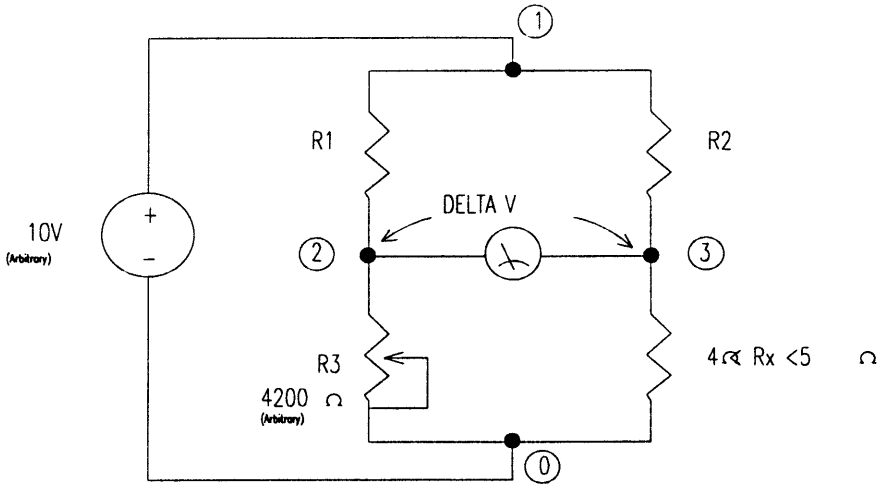


Figure 1 Wheatstone bridge with P-SPICE nodes indicated

The task for this Wheatstone bridge problem is to select the proper ratio of R2/R1, so that the unknown (Rx) can be measured to an accuracy of 4 decimal places with the digital variable resistor. The bridge (Fig. 1) is "balanced" when the voltage difference between nodes 2 and 3 (delta V) is zero. Since the bridge is actually two voltage dividers, the "balanced" condition is satisfied when:

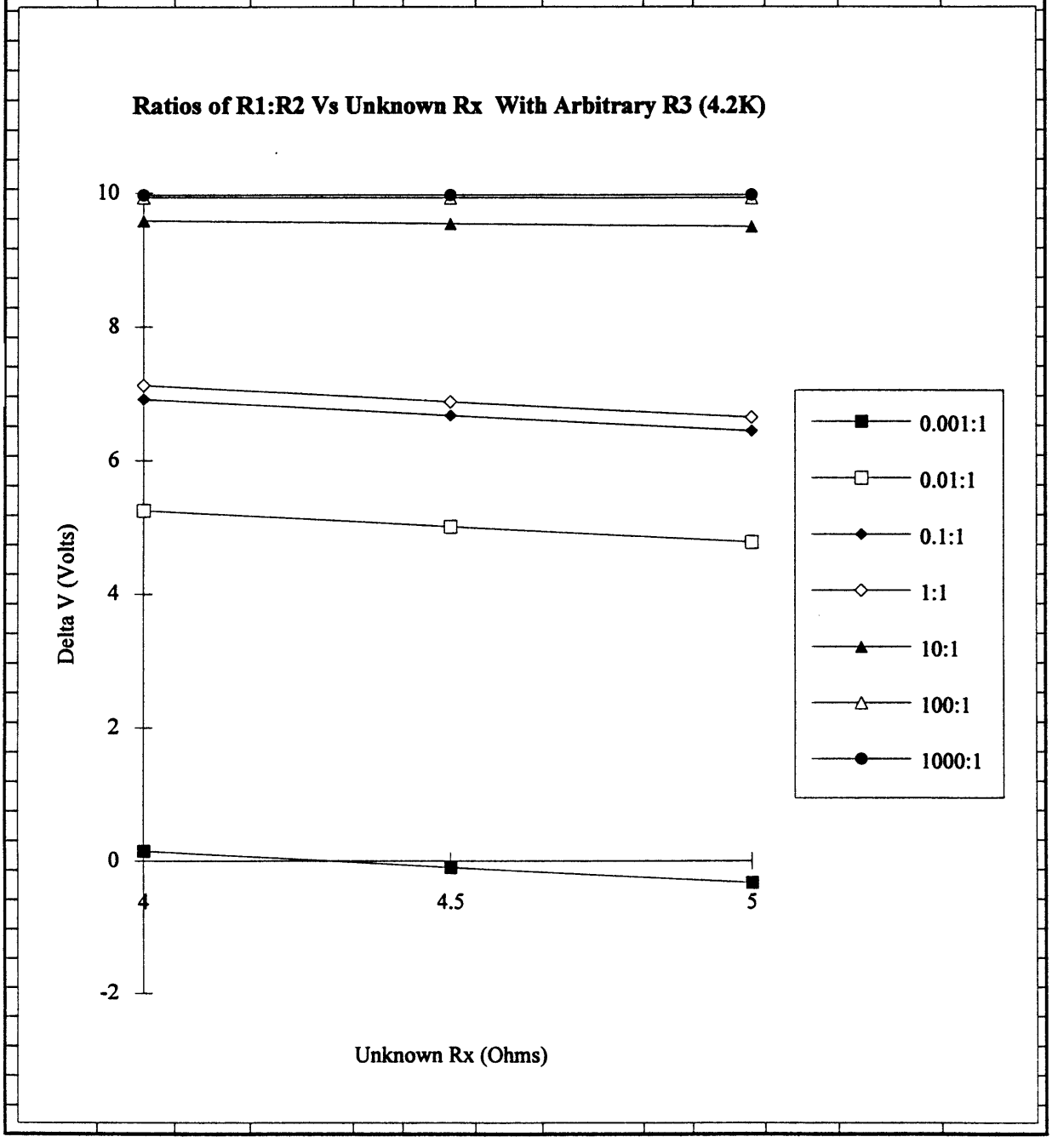
R1/R2=Rx/R3

The digital variable resistor (R3) has a maximum value of 11,110Ω. Changing the ratio R2/R1 has a multiplying effect on R3 (and also the range of measurable Rx for a given ratio). Since the desired accuracy is 4 significant figures, and the unknown is between 4Ω and 5Ω, R3 should have at least 1 integer and 3 fractional figures. This happens to be the maximum number of fractional figures, since the most significant digit of the resistor has a maximum value of 1 and cannot be set to 5.
When R2/R1 = 1, R3 is multiplied by 1, and indicates Rx directly in ohms (1Ω steps). As the ratio is decreased, the (imaginary) decimal point on R3 is moved to the left. When the ratio is 0.001, R3 will indicate a maximum value of 11.110Ω, which is satisfies the requirements. A graph on the next page shows how delta V varies with Rx, for an arbitrary value of R3 (4200Ω). The bottom curve shows the smallest values of delta V as Rx varies, and even crosses the zero axis indicating the balanced condition. This curve corresponds to the R2/R1 ratio of 0.001, which would be the correct ratio to use.

The following is a copy of the code used in the simulation. Runs were made for each of the given R2/R1 ratios

```
Problem 3-53 -- Wheatstone bridge
V1    1    0    DC    10
R2    1    3    10
R1    1    2    10000
Rx    0    3    Rmod  1                                    ;Define Rx as a variable
R3    0    2    4300
.MODEL          Rmod  RES (R=1)                            ;Define the model as a resistor
.STEP LIN       RES   Rmod (R)      4      5      0.5      ;Vary Rx from 4 to 5 (step=1/2)
.END
```

Rx=4 Ohms			Rx=4.5 Ohms			Rx=5 Ohms		
V(2)	V(3)	Delta V	V(2)	V(3)	Delta V	V(2)	V(3)	Delta V
3.007	2.857	0.1499	3.007	3.103	-0.0964	3.007	3.333	-0.3263
8.1132	2.857	5.2561	8.113	3.103	5.0098	8.113	3.333	4.7799
9.7727	2.857	6.9156	9.773	3.103	6.6693	9.773	3.333	6.4394
9.9768	2.857	7.1197	9.977	3.103	6.8734	9.977	3.333	6.6435
9.9768	0.385	9.5922	9.977	0.431	9.5462	9.977	0.476	9.5006
9.9768	0.04	9.937	9.977	0.045	9.932	9.977	0.05	9.927
9.9768	0.004	9.9728	9.977	0.005	9.9723	9.977	0.005	9.9718



Problem 4-79

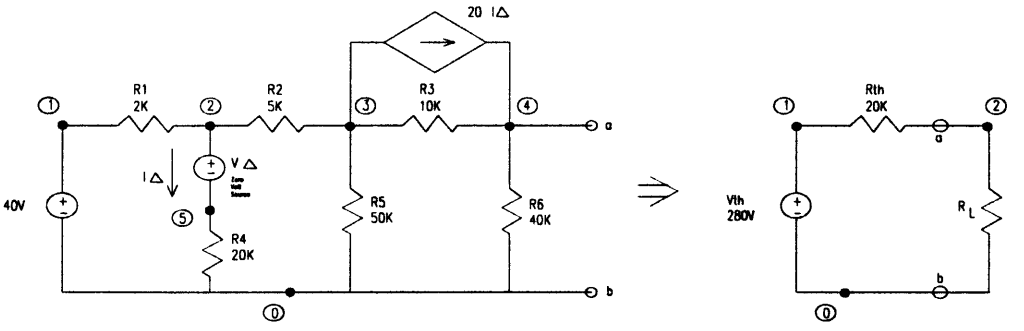


Figure 1 Circuit with P-SPICE nodes indicated and equivalent circuit

This problem requires the value of R_L and the maximum power transfered from the circuit to be found. The problem was solved in two steps. First, the original circuit was analyzed to find the Thevenin equivalent (Figure1) using the transfer function (.TF) analysis. The output file is shown below:

```
******* 03/02/93 ******* Evaluation PSpice (July 1989) ******* 00:31:33 *****************
Problem 4-79 -- Max. pwr. xfer. 4-79a.cir finds Thevenin equiv. 4-79b vaires Ro.
****     CIRCUIT DESCRIPTION
******************************************************************************
* Resistors
R1     1     2     2000
R2     2     3     5000
R3     3     4     10000
R4     5     0     20000
R5     3     0     50000
R6     4     0     40000
* Independent source
V1     1     0     DC     40
* Current control source
Videlta 2     5     DC     0
* Dependent source
F1     3     4     Videlta 30
* Analysis tools
.TF    V(4,0)  V1
.PROBE
.END

******* 03/02/93 ******* Evaluation PSpice (July 1989) ******* 00:31:33 *****************
Problem 4-79 -- Max. pwr. xfer. 4-79a.cir finds Thevenin equiv. 4-79b vaires Ro.
****     SMALL SIGNAL BIAS SOLUTION      TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
(   1)  40.0000 (   2)  24.0000 (   3) -10.0000 (   4) 280.0000
(   5)  24.0000
```

```
  VOLTAGE SOURCE CURRENTS
  NAME       CURRENT
  V1         -8.000E-03
  Videlta    1.200E-03
  TOTAL POWER DISSIPATION  3.20E-01  WATTS

****    SMALL-SIGNAL CHARACTERISTICS
   V(4,0)/V1 =  7.000E+00

   INPUT RESISTANCE AT V1 =  5.000E+03
   OUTPUT RESISTANCE AT V(4,0) =  2.000E+04

     JOB CONCLUDED
     TOTAL JOB TIME          1.65
```

It is known that maximum power is transferred (to the load) when the source resistance equals the load resistance. The power transferred to the load is therefore 1/2 the total power. The P-SPICE analysis gives the equivalent source resistance (Rth) as 20KΩ. It is expected that the load resistor should also equal 20KΩ, which would yield maximum power transfer. To prove this, a second analysis was run, varying the load around the theoretical 20KΩ value. Load power VS load resistance are shown graphically on the next page. The graph shows that maximum power is developed in the resistor when it's value equals the source resistance of 20KΩ.

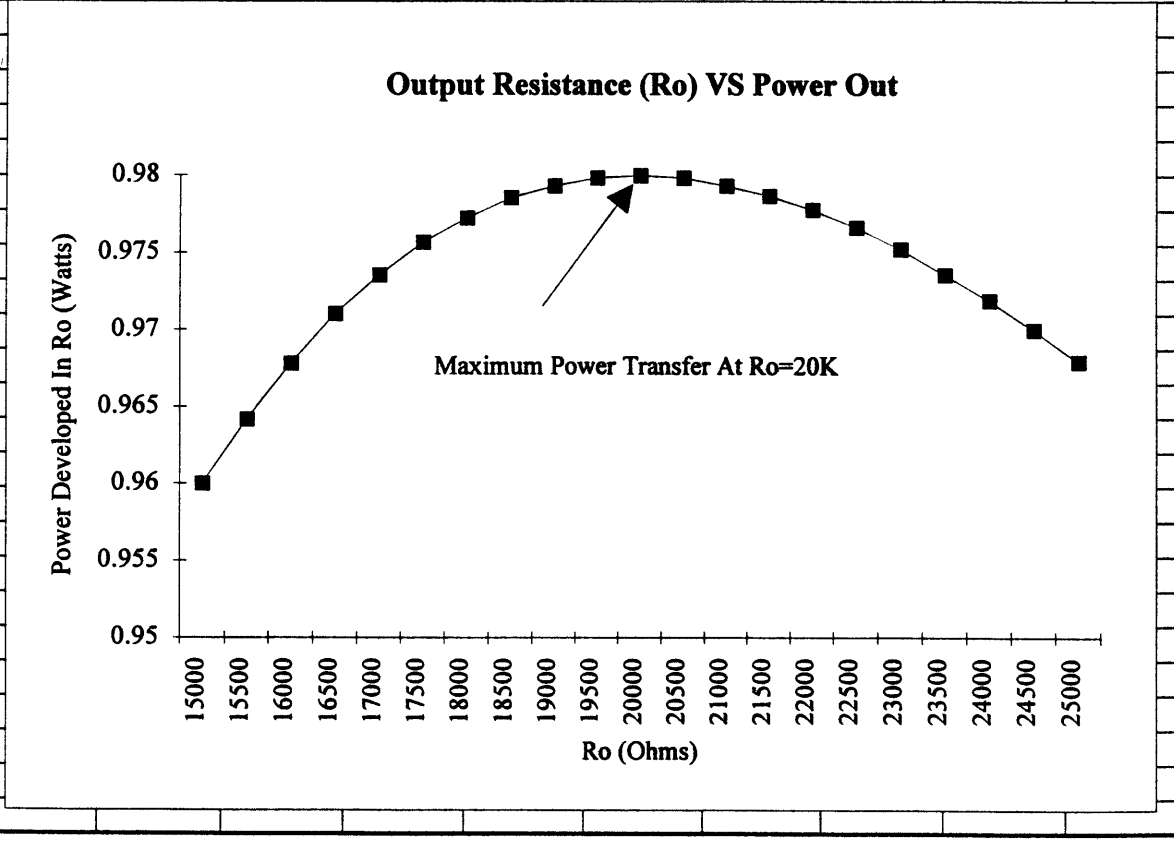
Final results: R_L=20KΩ Power R_L=0.98w
The power on R_L represents 50% of the total power developed in the circuit.

Shown below is a copy of the output file from the second analysis, with only the value of R_L=20KΩ shown:

```
******* 03/02/93 ******* Evaluation PSpice (July 1989) ******* 20:13:16 *******
Problem 4-79 -- Max. pwr. xfer. This pgm. varies Ro. 4-79a.cir is Thev. equiv.
****    CIRCUIT DESCRIPTION
******************************************************************************
* Resistors
R1    1     2     20000
* Output resistor defined as a variable model
Ro    2     0     Rmod   1
* Independent source
V1    1     0     DC     280
* Analysis tools
.MODEL  Rmod   RES(R=1)
*                        R-init  R-final  Increment
.STEP  LIN    RES    Rmod(R)     15000    25000   500
.PROBE
.END

****    Resistor MODEL PARAMETERS
        Rmod
   R    1

****    CURRENT STEP              RMOD R =  20.0000E+03

NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE   NODE  VOLTAGE
(  1) 280.0000 (  2) 140.0000


  TOTAL POWER DISSIPATION  1.96E+00  WATTS
```

Data and graphical analysis of load power VS load resistance.

V load	R load	P load
120	15000	0.96
122.25	15500	0.964198
124.44	16000	0.967832
126.58	16500	0.97106
128.65	17000	0.973578
130.67	17500	0.975694
132.63	18000	0.977262
134.55	18500	0.978579
136.41	19000	0.979352
138.23	19500	0.979873
140	20000	0.98
141.73	20500	0.979873
143.41	21000	0.979354
145.06	21500	0.978716
146.67	22000	0.977822
148.24	22500	0.976671
149.77	23000	0.975263
151.26	23500	0.973599
152.73	24000	0.971936
154.16	24500	0.970012
155.56	25000	0.967957



100

CIRCUITS, SIGNALS AND SYSTEMS
EEAP244

SPRING TERM 1993

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PSPICE ASSIGNMENT #1

PSPICE HOMEWORK

P3-53:

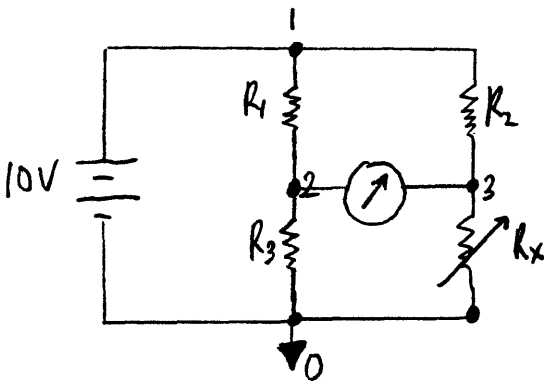


figure1

$$\frac{R_x}{R_3} = \frac{R_2}{R_1}$$ Equation 1

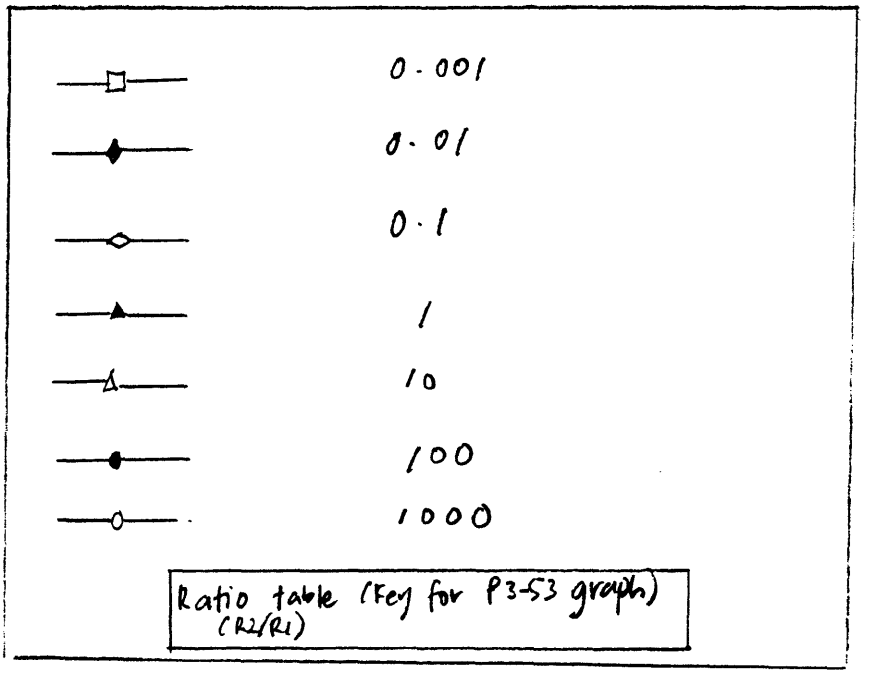
The main idea in solving this problem is to find the value of Rx, by adjusting the ratio of R2/R1 to certain value. However as suggested in the question, the value of R3 is lying between 1 to 11,110 ohm. In order to get the value of correct R3 we use the characteristis of a wheatstone bridge; when Ig =0.

Why I choose R3=4000ohm. It is obvious, because in order to get the unknown resistor in 4 significant figure, the value of R3 must lay between 4000 - 5000 ohm. From equation 1, Rx will only vary between 4 till 5 ohm. If Rx=4, R3=4000 then the ratio will produce a 4 sig. figure value of Rx.

From the graph, I conclude that the only ratio of R2/R1 by using the given value of Rx is 1/1000. This is because the wheatstone brigde will have a zero voltage different at node 2 and 3. Please refer to the given graph.

```
Problem 3.53 Wheatstone Bridge

V1  1  0 DC 10V
R1  1  2 1
R2  1  3 1000
R   ?  0 4000
Rx  3  0 Rmod 1
.MODEL Rmod RES(R=1)
.STEP LIN RES Rmod(R) 4,5,0.2
.PRINT DC V(2),V(3),V(3,2)
.END
```

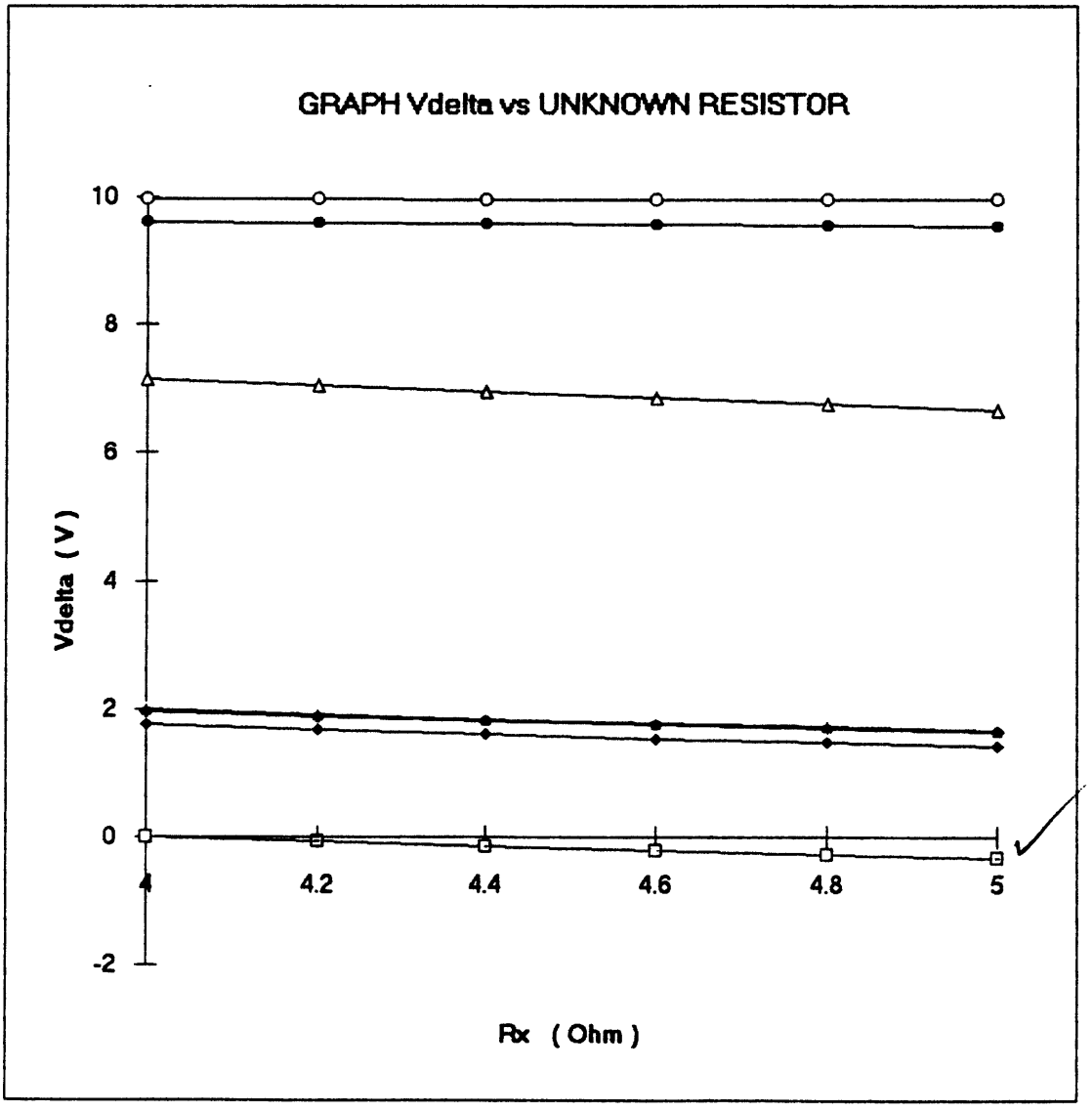
KEY FOR PROB 3-53



Ratio table (Key for P3-53 graph)
(R2/R1)

Data from output P3.53

Rx (Ohm)	Vdelta (V)						
4	0	1.7561	1.9751	1.9975	7.1404	9.6129	9.9577
4.2	-0.0769	1.6792	1.8941	1.9206	7.0398	9.5944	9.9557
4.4	-0.1481	1.608	1.827	1.8494	6.9419	9.576	9.9535
4.6	-0.2143	1.5418	1.7608	1.7832	6.8468	9.5577	9.9517
4.8	-0.2759	1.4802	1.6992	1.7216	6.7543	9.5395	9.9497
5	-0.3333	1.4228	1.6418	1.6642	6.6642	9.5213	9.9472



P4-79:

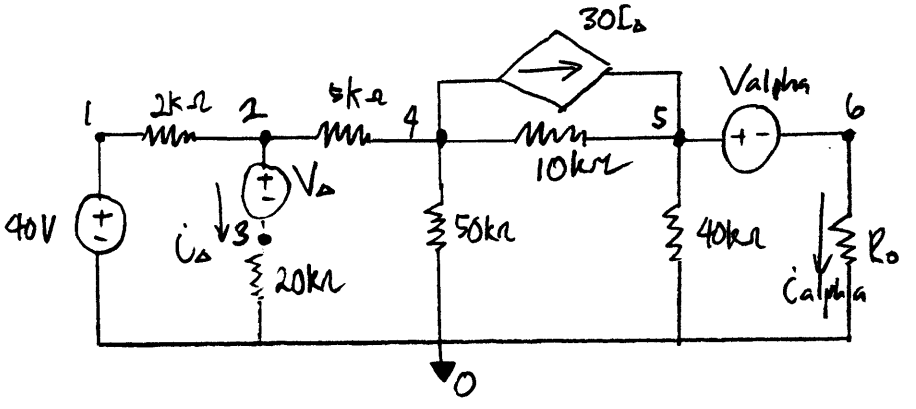


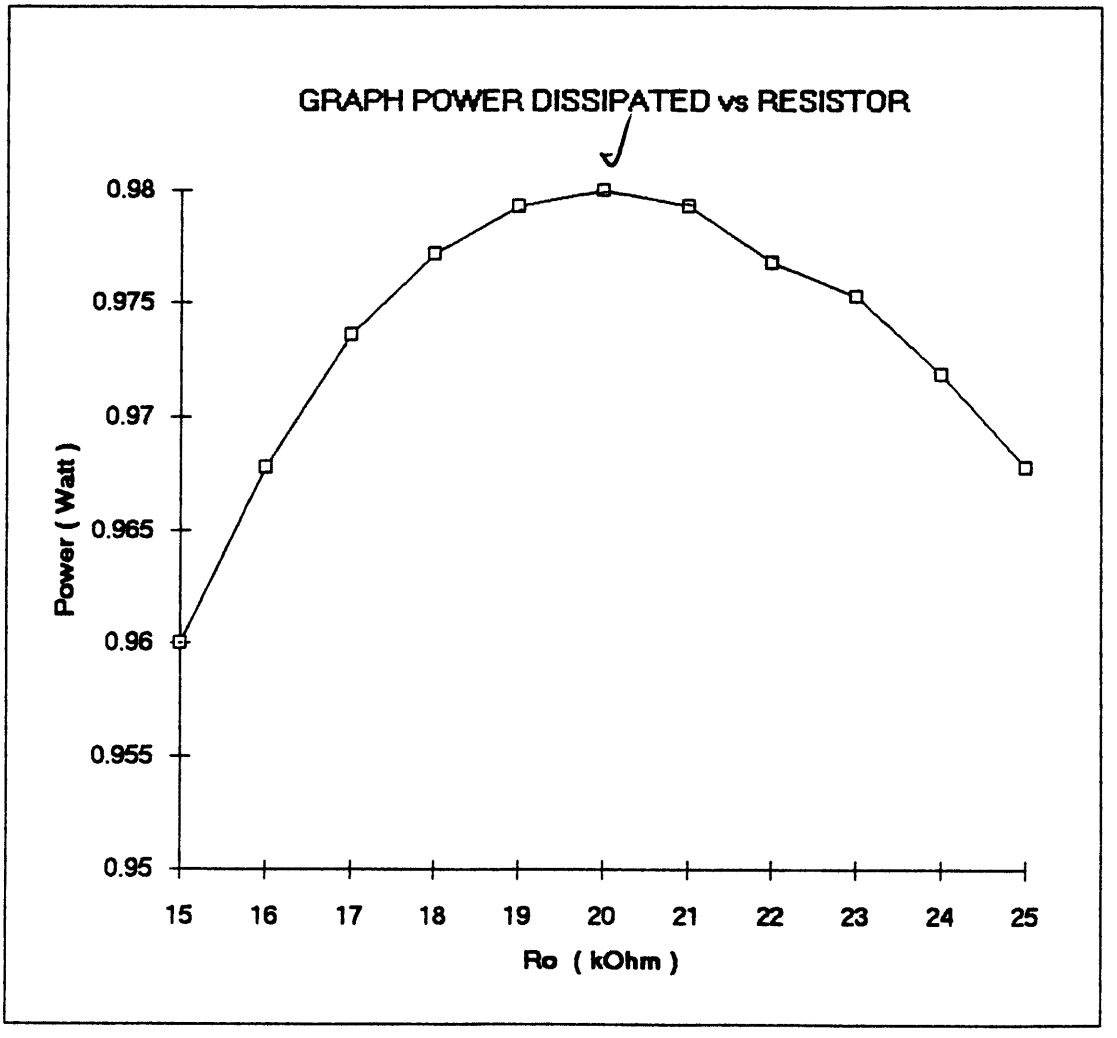
figure 2

a) by using pspice the Ro is 20k, which is the Rthev
b) the maximun power to Ro is 0.98 W
   P=vi v=140V, i=7.0e-3
c) % = (total power dissipated/power at Ro) x 100%
   = (0.432/0.98) x 100% = 44.08 %

```
*Problem 4.79 ; Find value of Ro

I   1 0 DC 40
R1 1 2 2k
R2 3 0 20k
R3 2 4 5k
R4 4 0 50k
R5 4 5 10k
F1 4 5 Vdelta 30
Vdelta 2 3 DC 0
Valpha 5 6 DC 0
R6 5 0 40k
R7 6 0 Rmod 1
.MODEL Rmod RES(R=1)
.STEP RES Rmod(R) 25k 45k 5k
.PROBE
.END
```

Data From output file Problem 4.79

Ro (kOhm)	Power (W)
15	0.96
16	0.9678
17	0.9736
18	0.9772
19	0.9793
20	0.98
21	0.9793
22	0.9768
23	0.9753
24	0.9719
25	0.9678



100

Dale Higginbotham
295 - 60 - 4803
3 - 5 - 93

Pspice problems:

3.53 Wheatstone Bridge:

For the Wheatstone bridge to work effectively their should be no current between the two branches. For this to happen (as proved in the textbook) the Ratio of R3 / R1 has to be equal to Rx / R2. I was given seven values for a ratio of R2 to R1 that varied between .001 to 1000. I was also given that Rx lied between 4 and 5 volts.

Therefore I implemented the program on the following page 21 times. Each time I implemented the program I changed Rx and R1. Rx was changed from the 4 to the exact ratio that gives the answer (4.567) and then changed again to 5. R1 was changed by a factor of ten to accommodate each ratio. I also changed Rx from 4-5 to 40-50 to 400-500, etc., because when I divided R1 by 10 I had to multiply Rx by 10 so as to keep the same ratio.

To get 4 significant digits I used the ratio of .001. This ratio therefore gives the value of Rx between 4 and 5 volts and not 400 and 500 volts. For the actual value of Rx one could pick any number between 4 and 5 volts as long as it had 4 significant digits. I then got R3 by dividing Rx by .001 to get 4567 ohms.

*Note: The program on the following page gives the correct ratio and values for Rx and R3. This program was used in all of the calculations.

4.79 Circuit to find Maximum Power through a load Resistance

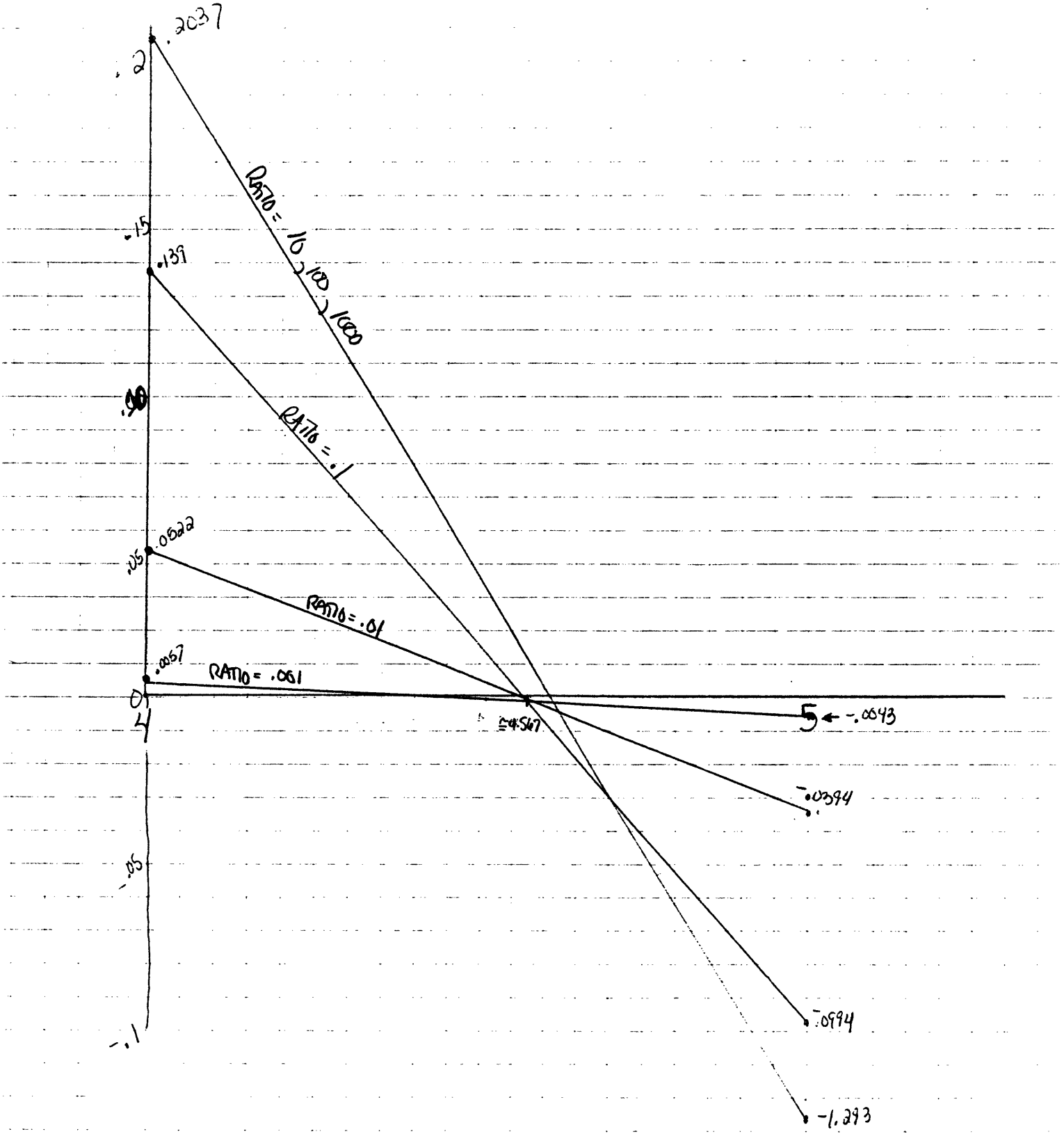
a:) To find the value of the load resistance at which the maximum power is delivered to it, I used the program on the following pages. This program generated an output file from which I took the values of the voltage at node a and the current through that branch and multiplied them to find the power at different resistances (values in table after program). The maximum power occurs when the load resistance is given a value of **20 kohms** as seen by the table and the graph.

b:) The maximum power at this resistance value is **.980 watts**.

c:) To find the total percentage of power delivered to Ro, I used KCL and KVL around the circuit to find the total power. Then I divided this value into the .98 watts (power dissipated by resistor) to get the percentage of total power developed in the circuit. This percentage is equal to **19.02 percent**.

```
Pspice problem 3.53 from text
Vin      1        0        DC       10
R1       1        2        1000k
R        1        3        1k
R        2        0        4567
Rx       3        0        4.567
.probe
.end
```

Graph for Problem 3.53

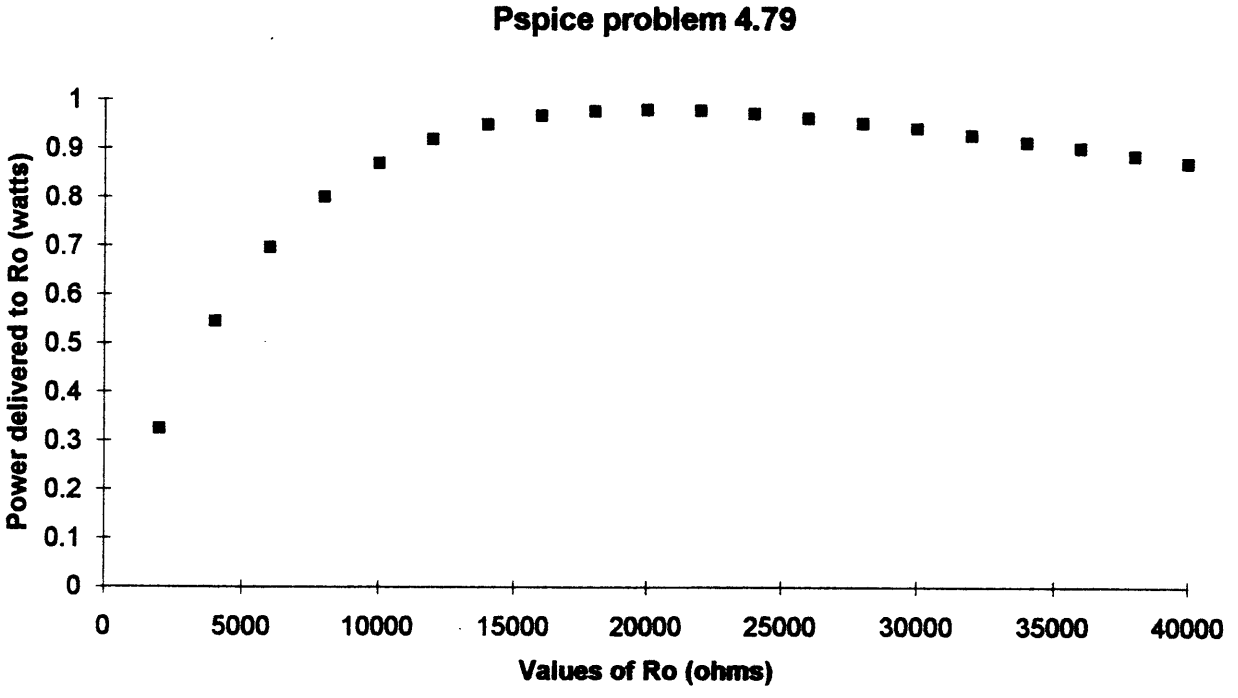


* the ratio of 1 was not drawn because of computer simulation errors (I did not use the same value for Vin)

* not drawn to scale

```
Pspice problem 4.79 from text
Vs      1       0       DC      40
Vdelta  2       3       DC      0
V ter   5       6       DC      0
H       4       5       Vdelta  30
R1      1       2       2k
R2      3       0       20k
R3      2       4       5k
R4      4       5       10k
R5      4       0       50k
R6      5       0       40k
R0      6       0       Rmod 1
.model Rmod Res(R=1)
.step lin Res Rmod(R) 2k,100k,2k
.probe
.end
```

Program Listing 4.79


Pspice problem 4.79
Power delivered to Ro (watts)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
5000
10000
15000
20000
25000
30000
35000
40000
Values of Ro (ohms)

R_o	Power
2000	0.324
4000	0.5446
6000	0.6959
8000	0.8
10000	0.8704
12000	0.91875
14000	0.9488
16000	0.967583
18000	0.9772
20000	0.98
22000	0.9778
24000	0.9719
26000	0.9622
28000	0.9522
30000	0.9408
32000	0.92707
34000	0.91256
36000	0.9
38000	0.884229
40000	0.86988

For part A: $R_G = 20K\Omega = R_{TH}$

part B: $P = .980$ WATTS

part C: % of total power delivered to R_o: 19.02%

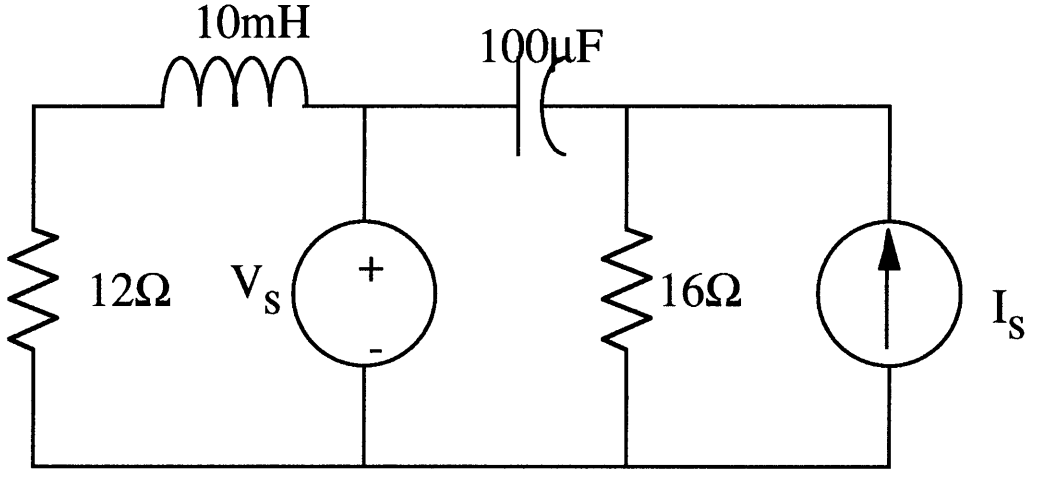
Print engine name:	PrintServer 20
Print engine version:	17
Printer firmware version:	32
Server Adobe PostScript version:	48.3
Server software version:	V2.0
Server network node:	crawford
Server name:	crawford
Server job number:	86
Client software version:	WRL-1.0
Client network node:	util
Client name:	flm
Client job name:	pspice_hw2.ps.735168793
Submitted at:	Sun Apr 18 17:53:57 19933X
Printed at:	Sun Apr 18 17:53:58 1993

flm@util
pspice_hw2.ps.735168793

PSpice HW #2: Due: March 12, 1993

Phasor analysis
Reference Conant, Chapter 5.

1. The voltage source in the circuit shown is 119cos(800t+0.7°) and the current source is 4.27cos(800t+41.9°). Find the current flowing downward through the 16 ohm resistor.



Solution:

The answer is 7.162 +j3.204 amps.

```
**** 03/17/93 11:16:44 *********** Evaluation PSpice (Jan 1993)
 Problem 5-1

 ****     CIRCUIT DESCRIPTION

******************************************************************************


R10 1 0 12
L12 1 2 10m
V20 2 0 ac 119 0.7
C23 2 3 100u
R30 3 0 16
I03 0 3 ac 4.27 41.9
.ac lin 1 127.3 127.3
.print ac IM(R30) IP(R30) IR(R30) II(R30)
.end

**** 03/17/93 11:16:44 *********** Evaluation PSpice (Jan 1993)
 Problem 5-1


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************
```

```
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(   1)    0.0000  (   2)    0.0000  (   3)    0.0000


    VOLTAGE SOURCE CURRENTS
    NAME          CURRENT

    V20           0.000E+00

    TOTAL POWER DISSIPATION   0.00E+00  WATTS

**** 03/17/93 11:16:44 *********** Evaluation PSpice (Jan 1993)
 Problem 5-1

 ****     AC ANALYSIS                        TEMPERATURE =   27.000 DEG C

*******************************************************************************

  FREQ         IM(R30)     IP(R30)     IR(R30)     II(R30)

   1.273E+02   7.846E+00   2.410E+01   7.162E+00   3.204E+00

          JOB CONCLUDED

          TOTAL JOB TIME             .87

**** 03/17/93 11:16:45 *********** Evaluation PSpice (Jan 1993)
 * 7.162 +j3.204


 ****     CIRCUIT DESCRIPTION

*******************************************************************************

WARNING -- There are no devices in this circuit, (this message will be
printed if there are blank lines after the last .END statement)
```

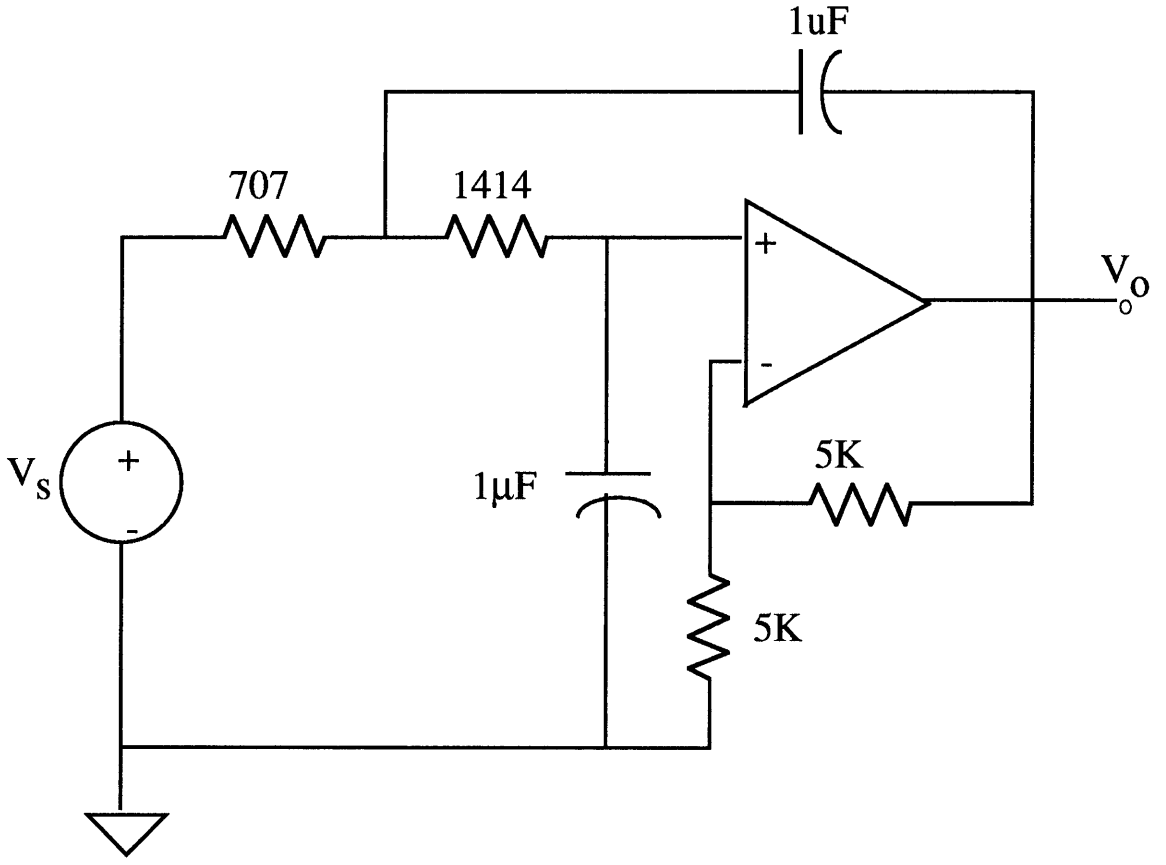
COMMENTS:

1. You lost 5 points if you did not label your answer. This will happen on all future PSpice homeworks.

2. You also lost 3 points for the wrong direction of a source, and 10 points for the wrong answer or no answer.

3. Labeled nodes are a big plus if your answer is wrong.

2. This op amp circuit is a low pass filter with a cutoff frequency of ω=1000/s. Find the output voltage when the input voltage is a unit sinusoid of that frequency.



Solution:

```
The answer is -j1.414


**** 03/17/93 11:21:12 ********** Evaluation PSpice (Jan 1993)
 Problem 5-5


 ****     CIRCUIT DESCRIPTION

******************************************************************************

V10 1 0 ac 1
R12 1 2 707
R23 2 3 1414
C30 3 0 1u
C24 2 4 1u
R45 4 5 5k
R50 5 0 5k
R35 3 5 1e7
E60 6 0 3 5 1e5
R64 6 4 100
.ac lin 1 .159k .159k
.print ac VM(4) VP(4)
.end
```

```
**** 03/17/93 11:21:12 ********** Evaluation PSpice (Jan 1993)
 Problem 5-5

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(    1)    0.0000  (    2)    0.0000  (    3)    0.0000  (    4)
0.0000

(    5)    0.0000  (    6)    0.0000



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V10          0.000E+00

    TOTAL POWER DISSIPATION   0.00E+00  WATTS

**** 03/17/93 11:21:12 ********** Evaluation PSpice (Jan 1993)
 Problem 5-5

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

*******************************************************************************

  FREQ        VM(4)       VP(4)

   1.590E+02   1.416E+00  -8.991E+01

          JOB CONCLUDED

          TOTAL JOB TIME             .90

**** 03/17/93 11:21:13 ********** Evaluation PSpice (Jan 1993)
 * -j sqrt(2)

 ****     CIRCUIT DESCRIPTION

*******************************************************************************
```

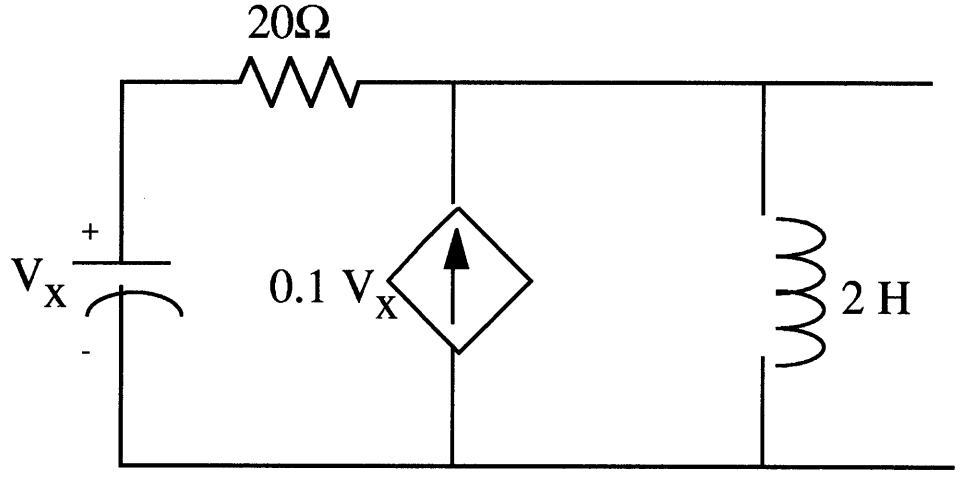
COMMENTS:

1. You could have also used a LM318 or uA741 from the PSpice library with a slight change in the numerical value of the answers.

2. PSpice works in linear frequency (Hz). Several of you used specified radians/second in the problem. You lost five points for the failure to convert your numbers.

3. Several of you used AC power supplies and/or reversed the polarity of the power supply. You lost 3 to 5 points depending upon the severity of the error.

3. Determine the Thevenin equivalent circuit at the terminals, at a frequency ω=10/s. Attach this Thevenin equivalent circuit, including an AC source, to the original circuit and show that the terminal voltage is the same for the original circuit and for its Thevenin equivalent.



Solutions:

```
**** 03/17/93 11:25:54 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt

 ****     CIRCUIT DESCRIPTION

******************************************************************************


C10 1 0 .01
R12 1 2 20
G02 0 2 1 0 .1
L20 2 0 2
I02 0 2 ac 1
.ac lin 1 1.5915 1.5915
.print ac VR(2) VI(2)
.end

**** 03/17/93 11:25:54 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt
```

```
 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

**********************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(    1)    0.0000  (    2)    0.0000


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    TOTAL POWER DISSIPATION   0.00E+00  WATTS

**** 03/17/93 11:25:54 *********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

**********************************************************************

  FREQ         VR(2)       VI(2)

   1.592E+00   4.000E+01  -2.000E+01

         JOB CONCLUDED

         TOTAL JOB TIME            .85

**** 03/17/93 11:25:55 *********** Evaluation PSpice (Jan 1993)
 Problem 5-6: TEC with new load ckt

 ****     CIRCUIT DESCRIPTION

**********************************************************************


R10 1 0 40
C12 1 2 .005
R20 2 0 1e10
L23 2 3 1
R34 3 4 5
V40 4 0 ac 4
.ac lin 1 1.5915 1.5915
```

```
.print ac VR(2) VI(2)
.end

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: TEC with new load ckt


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

**********************************************************************


 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(    1)    0.0000  (    2)    0.0000  (    3)    0.0000  (    4)
0.0000



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V40          0.000E+00

    TOTAL POWER DISSIPATION   0.00E+00  WATTS

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: TEC with new load ckt


 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

**********************************************************************


  FREQ        VR(2)       VI(2)

   1.592E+00   3.765E+00  -9.412E-01


          JOB CONCLUDED

          TOTAL JOB TIME            .42

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt with new load ckt


 ****     CIRCUIT DESCRIPTION

**********************************************************************
```

```
C10 1 0 .01
R12 1 2 20
G02 0 2 1 0 .1
L20 2 0 2
L23 2 3 1
R34 3 4 5
V40 4 0 ac 4
.ac lin 1 1.5915 1.5915
.print ac VR(2) VI(2)
.end

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt with new load ckt


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

(    1)    0.0000  (    2)    0.0000  (    3)    0.0000  (    4)
0.0000



    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V40          0.000E+00

    TOTAL POWER DISSIPATION   0.00E+00  WATTS

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt with new load ckt


 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

*******************************************************************************

  FREQ        VR(2)       VI(2)


   1.592E+00   3.765E+00  -9.411E-01


          JOB CONCLUDED

          TOTAL JOB TIME             .43

**** 03/17/93 11:25:55 ********** Evaluation PSpice (Jan 1993)
 * 40 ohms in series with 0.005 F capacitor
```

```
 ****     CIRCUIT DESCRIPTION

******************************************************************************


WARNING -- There are no devices in this circuit, (this message will be
printed if there are blank lines after the last .END statement)
```

COMMENTS:

1. The Thevenin resistance (impedance) is measured by applying a voltage or current source to the circuit under test. Several of you applied this test source from the left, i.e. across the capacitor. This was incorrect and caused you to lose 10 points. It was to be applied across the inductor. There is no Thevenin equivalent voltage source because the circuit has no independent voltage sources. When I used a test source of 1A I got $Z_{thevenin}$=40-j20 ohms which is a 40 ohm resistor in series with a 0.005μF capacitor.

2. This circuit is easier to analyze if you use a current source. That way the voltage at the test node is exactly the impedance because the voltage divided by the current is the impedance and anything divided by 1 (a good choice of test current) will be unchanged.

3. You cannot use a voltage test source unless you put it in series with a resistor. The value of the resistor is immaterial. The reason for this is that you will otherwise end up with two voltage sources in parallel which you know from the first quiz is not allowed.

4. This was a tough problem. If you did not indicate how you were calculating the Thevenin impedance I deducted 30 points. A PSpice printout is NOT the answer to this problem. You must typically do additional calculations which had to be presented.

5. Some people used the .TF command. This was a good idea but it only computes the DC Thevenin. This was an AC Thevenin problem and you lost 10 points.

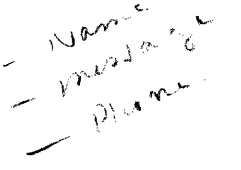
6. A lot of people used C=0.01μF since I gave this value in class. You did not lose any points for this and the corresponding results for C=0.01μF follow. Note that the equivalent impedance now becomes -8+j4 (8.944–153∞) ohms which is a negative 8 ohm resistance in series with a 0.4 henry inductor.

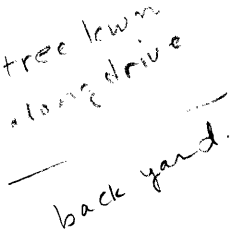
```
**** 03/26/93 21:39:20 ********** Evaluation PSpice (Jan 1993)
**************

 Problem 5-6: original ckt

 ****     CIRCUIT DESCRIPTION
******************************************************************************
C10 1 0 .01u
R12 1 2 20
G02 0 2 1 0 .1
L20 2 0 2
I02 0 2 ac 1
.ac lin 1 1.5915 1.5915
.print ac VR(2) VI(2)
```

```
.end

**** 03/26/93 21:39:20 ********** Evaluation PSpice (Jan 1993)
**************
 Problem 5-6: original ckt
 ****     AC ANALYSIS                          TEMPERATURE =   27.000 DEG C
******************************************************************************
  FREQ         VR(2)       VI(2)
   1.592E+00  -8.000E+00   4.000E+00



**** 03/26/93 21:39:21 ********** Evaluation PSpice (Jan 1993)
**************
 Problem 5-6: TEC with new source ckt
 ****     CIRCUIT DESCRIPTION
******************************************************************************
R10 1 0 -8
L12 1 2 .4
L23 2 3 1
R34 3 4 5
V40 4 0 ac 4
.ac lin 1 1.5915 1.5915
.print ac VR(2) VI(2)
.end

**** 03/26/93 21:39:21 ********** Evaluation PSpice (Jan 1993)
**************
 Problem 5-6: TEC with new source ckt
 ****     AC ANALYSIS                          TEMPERATURE =   27.000 DEG C
******************************************************************************
FREQ         VR(2)       VI(2)
   1.592E+00   1.561E+00   1.951E+00


          JOB CONCLUDED

          TOTAL JOB TIME             .70

**** 03/26/93 21:39:22 ********** Evaluation PSpice (Jan 1993)
**************
 Problem 5-6: original ckt with new source ckt
 ****     CIRCUIT DESCRIPTION
******************************************************************************
C10 1 0 .01u
R12 1 2 20
G02 0 2 1 0 .1
L20 2 0 2
L23 2 3 1
R34 3 4 5
V40 4 0 ac 4
.ac lin 1 1.5915 1.5915
.print ac VR(2) VI(2)
.end

**** 03/26/93 21:39:22 ********** Evaluation PSpice (Jan 1993)
 Problem 5-6: original ckt with new source ckt
 ****     AC ANALYSIS                          TEMPERATURE =   27.000 DEG C
******************************************************************************
FREQ         VR(2)       VI(2)
```

```
   1.592E+00    1.561E+00    1.951E+00


           JOB CONCLUDED

           TOTAL JOB TIME             .43

**** 03/26/93 21:39:22 ********** Evaluation PSpice (Jan 1993)
**************

 * -8 ohms in series with 0.4H inductor


 ****     CIRCUIT DESCRIPTION


********************************************************************************
WARNING -- There are no devices in this circuit, (this message will be
printed if there are blank lines after the last .END statement)
```

Print engine name:	PrintServer 20
Print engine version:	17
Printer firmware version:	32
Server Adobe PostScript version:	48.3
Server software version:	V2.0
Server network node:	crawford
Server name:	crawford
Server job number:	20
Client software version:	WRL-1.0
Client network node:	util
Client name:	flm
Client job name:	PSpice_HW3.ps.734099538
Submitted at:	Tue Apr 6 09:09:04 19933X
Printed at:	Tue Apr 6 09:09:04 1993



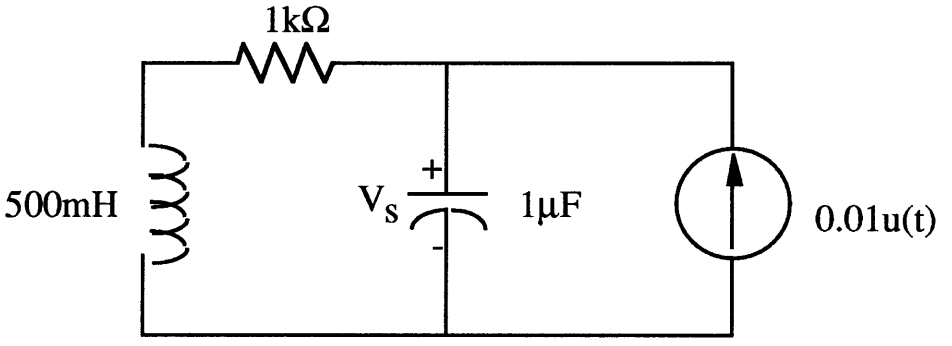


flm@util
PSpice_HW3.ps.734099538

PSpice HW #3: Due: April 2, 1993

Transient analysis
Reference: Conant, Chapter 4, 8.

4.7. At $t=0^-$, the capacitor voltage is 20 volts and the power dissipated by the resistor is 40 mW, and the current source is inactive. For $t>0$, the source injects 10 mA of current into the circuit. Demonstrate, using superposition with Probe, that the resistor current is the sum of current contributions arising from the current source and from the initial condition energy storage in the capacitor and inductor.

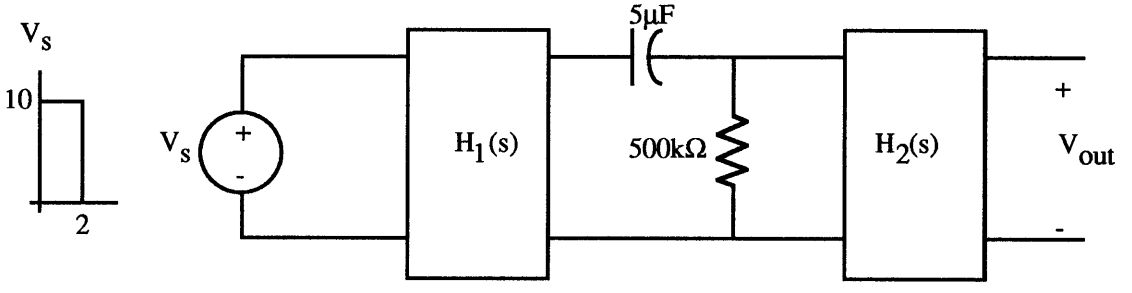


8.2. Calculate the inverse Laplace transform of

$$H(s) = \frac{s^2 + 8s + 13}{(s+1)(s+2)(s+3)},$$

by hand. Use PSpice and Probe to display your calculated f(t) and also to display the inverse transform directly, as the output of a Laplace-form E-source.

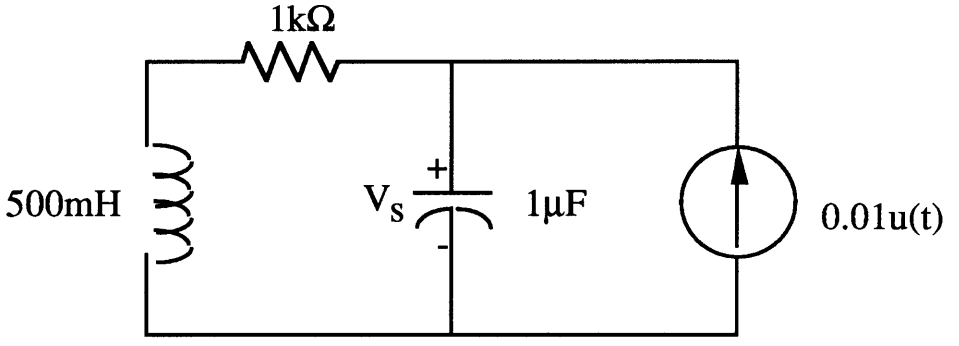
8.3. The pulse shown enters the system shown, with $H_1(s) = \frac{5}{s^2 + s + 5}$ and $H_2(s) = \frac{5}{s^2 + s + 10}$. Display the output of the system, $v_{out}(t)$.



PSpice HW #3: Due: April 2, 1993

Transient analysis
Reference: Conant, Chapter 4, 8.

4.7. At $t=0^-$, the capacitor voltage is 20 volts and the power dissipated by the resistor is 40 mW, and the current source is inactive. For $t>0$, the source injects 10 mA of current into the circuit. Demonstrate, using superposition with Probe, that the resistor current is the sum of current contributions arising from the current source and from the initial condition energy storage in the capacitor and inductor.



Solutions:

```
Problem 4-7: capacitor IC only
L20 2 0 500m
R23 2 3 1K
C30 3 0 .1u IC = 20
.tran 6m 6m 0 .06m UIC
.probe
.end
Problem 4-7: inductor IC only
L20 2 0 500m IC = 6.31m
R23 2 3 1K
C30 3 0 .1u
.tran 6m 6m 0 .06m UIC
.probe
.end
Problem 4-7: CS only
I03 0 3 pwl 0,0 1u,10m
L20 2 0 500m
R23 2 3 1K
C30 3 0 .1u
.tran 6m 6m 0 .06m
.probe
.end
Problem 4-7: all IC's and source
I03 0 3 pwl 0,0 1u,10m
L20 2 0 500m IC = 6.31m
R23 2 3 1K
C30 3 0 .1u IC = 20
.tran 6m 6m 0 .06m UIC
.probe
```

```
.end
```

8.2. Calculate the inverse Laplace transform of

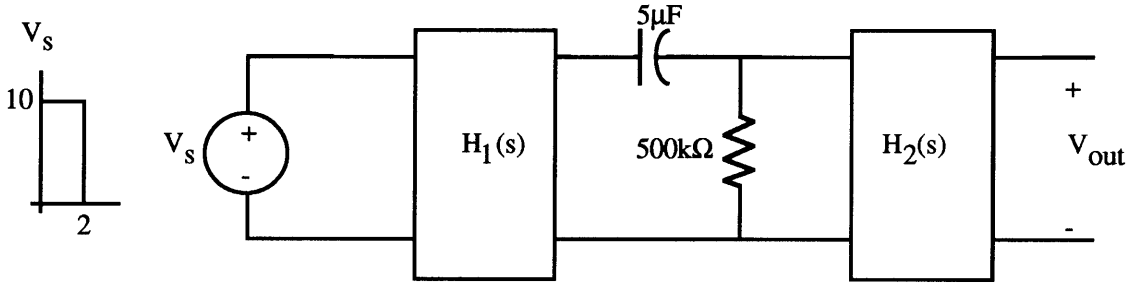
$H(s) = \dfrac{s^2 + 8s + 13}{(s+1)(s+2)(s+3)}$,

by hand. Use PSpice and Probe to display your calculated f(t) and also to display the inverse transform directly, as the output of a Laplace-form E-source.

Solution:

```
Problem 8-2
V10 1 0 pwl 0,0 1m,1K 2m,0  ;impulse
R10 1 0 1
E20 2 0 Laplace {V(1)} = {(s*s+8*s+13)/((s+1)*(s+2)*(s+3))}
R20 2 0 1
E30 3 0 value = {3*exp(-time) - exp(-2*time) - exp(-3*time)}
R30 3 0 1
.tran 5 5
.probe
.end
```

8.3. The pulse shown enters the system shown, with $H_1(s) = \dfrac{5}{s^2 + s + 5}$ and $H_2(s) = \dfrac{5}{s^2 + s + 10}$. Display the output of the system, $v_{out}(t)$.



Solution:

```
Problem 8-3
V10 1 0 pwl  0,0  1m,1  2,1  2.001,0
R10 1 0 1
E20 2 0 Laplace {V(1)} = {25/((s*s+s+10)*(s*s+s+5))}
R20 2 0 1
C23 2 3 5u
R30 3 0 100k
.tran 10 10
.probe
.end
```

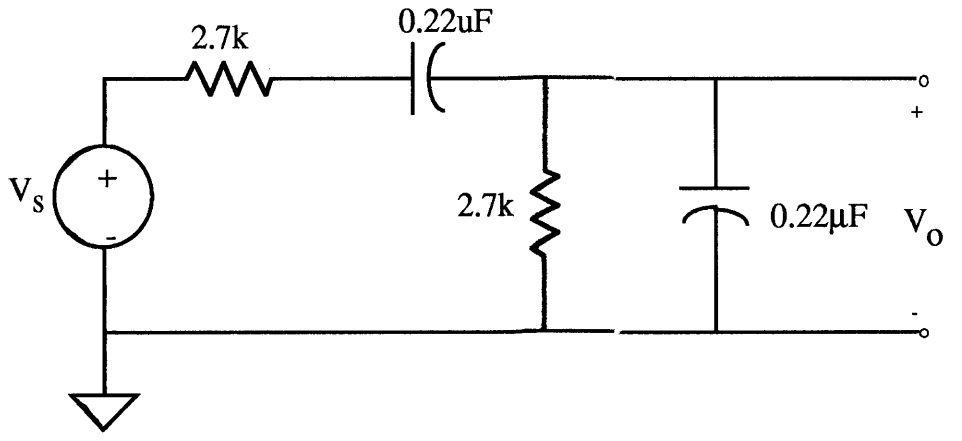
Print engine name:	PrintServer 20
Print engine version:	17
Printer firmware version:	32
Server Adobe PostScript version:	48.3
Server software version:	V2.0
Server network node:	crawford
Server name:	crawford
Server job number:	86
Client software version:	WRL-1.0
Client network node:	util
Client name:	flm
Client job name:	pspice_hw4.ps.735168779
Submitted at:	Sun Apr 18 17:55:50 19933X
Printed at:	Sun Apr 18 17:55:50 1993

flm@util
pspice_hw4.ps.735168779

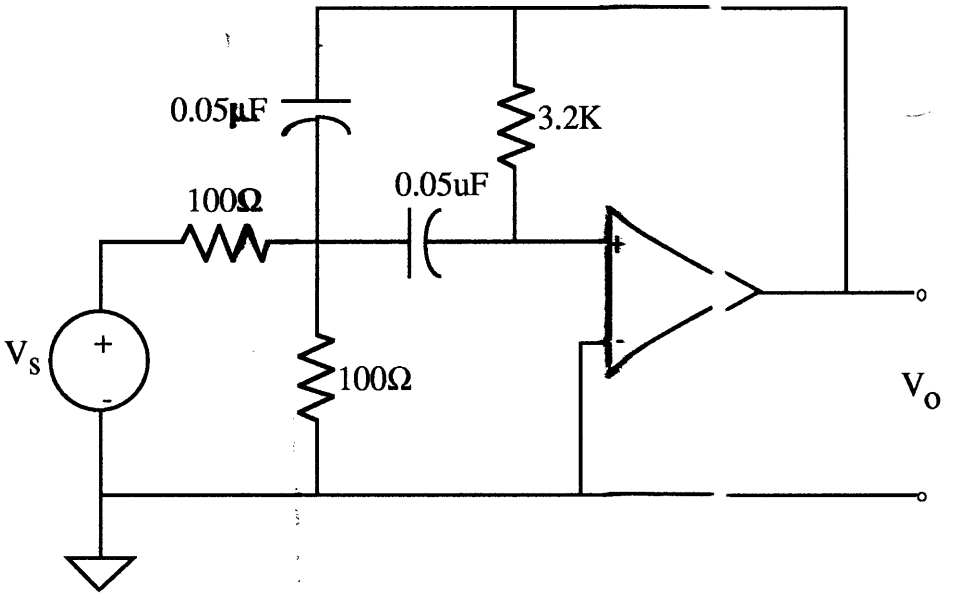
PSpice HW #4: Due: April 21, 1993

Frequency response
Reference: Conant, Chapter 6.

6.7. Display the magnitude and phase angle plots for $H(j\omega)=Vo(\omega)/Vs(\omega)$. Find the frequency at which the magnitude is a maximum. Find the frequency at which the phase angle is zero. This network is used in a common oscillator circuit.



6.8. Determine the center frequency and bandwidth of this bandpass filter, where the bandwidth is defined as the difference in frequency between the upper and lower half-power frequencies. At these frequencies, the magnitude of the output is $\frac{1}{\sqrt{2}}$ times the maximum, or 3dB lower than the maximum in dB units. Sharp second-order band pass filters like this one in the frequency domain correspond to underdamped resonant circuits in the time domain. Apply an impulse of voltage to this circuit and observe the transient response. How is the frequency of oscillation related to the center frequency of the filter? How is the damping related to the center frequency and bandwidth?



* Sample standard device library
*

* This is a reduced version of MicroSim's standard parts libraries. Some
* components from several types of component libraries have been included
* here. You are welcome to make as many copies of it as you find convenient.
*
* The Microsim library included with the production version of PSpice
* includes over 3,500 analog devices, and over 1,500 digital devices.
*
* Release date: January 1993
*
* It takes time for PSpice to scan a library file. To speed this up, PSpice
* creates an index file, called <filename>.IND. The index file is re-created
* whenever PSpice senses that the library file has changed.

* The following is a summary of parts in this library:
*
* Part name Part type
* --------- ---------
* Q2N2222A NPN bipolar transistor
* Q2N2907A PNP bipolar transistor
* Q2N3904 NPN bipolar transistor
* Q2N3906 PNP bipolar transistor
*
* D1N750 zener diode
* MV2201 voltage variable capacitance diode
* D1N4148 switching diode
* MBD101 switching diode
*
* J2N3819 N-channel Junction field effect transistor
* J2N4393 N-channel Junction field effect transistor
*
* LM324 linear operational amplifier
* LF411 linear operational amplifier
* UA741 linear operational amplifier
* LM111 voltage comparator
*
* K3019PL_3C8 ferroxcube pot magnetic core
* KRM8PL_3C8 ferroxcube pot magnetic core
* K502T300_3C8 ferroxcube pot magnetic core
*
* IRF150 N-type power MOS field effect transistor
* IRF9140 P-type power MOS field effect transistor
*
* 7402 TTL digital 2-input NOR gate
* 7404 TTL digital inverter
* 7405 TTL digital inverter, open collector
* 7414 TTL digital inverter, schmidt trigger
* 7474 TTL digital D-type flip-flop
* 74107 TTL digital JK-type flip-flop
* 74393 TTL digital 4-bit binary counter
*
* A4N25 optocoupler

```
*
*       2N1595          silicon controlled rectifier
*       2N5444          Triac
*
*       555D            555 timer subcircuit
*
*--------------------------------------------------------------------------------
* Library of bipolar transistor model parameters
*
* This is a reduced version of MicroSim's bipolar transistor model library.
*  You are welcome to make as many copies of it as you find convenient.
*
* The parameters in this model library were derived from the data sheets for
* each part. Each part was characterize using the Parts option.
* Devices can also be characterized without Parts as follows:
*
*       NE, NC                  Normally set to 4
*       BF, ISE, IKF    These are adjusted to give the nominal beta vs.
*                       collector current curve. BF controls the mid-
*                       range beta. ISE/IS controls the low-current
*                       roll-off. IKF controls the high-current rolloff.
*       ISC             Set to ISE.
*       IS, RB, RE, RC          These are adjusted to give the nominal VBE vs.
*                       IC and VCE vs. IC curves in saturation. IS
*                       controls the low-current value of VBE. RB+RE
*                       controls the rise of VBE with IC. RE+RC controls
*                       the rise of VCE with IC. RC is normally set to 0.
*       VAF             Using the voltages specified on the data sheet
*                       VAF is set to give the nominal output impedance
*                       (RO on the .OP printout) on the data sheet.
*       CJC, CJE        Using the voltages specified on the data sheet
*                       CJC and CJE are set to give the nominal input
*                       and output capacitances (CPI and CMU on the .OP
*                       printout; Cibo and Cobo on the data sheet).
*       TF              Using the voltages and currents specified on the
*                       data sheet for FT, TF is adjusted to produce the
*                       nominal value of FT on the .OP printout.
*       TR              Using the rise and fall time circuits on the
*                       data sheet, TR (and if necessary TF) are adjusted
*                       to give a transient analysis which shows the
*                       nominal values of the turn-on delay, rise time,
*                       storage time, and fall time.
*       KF, AF                  These parameters are only set if the data sheet has
*                       a spec for noise. Then, AF is set to 1 and KF
*                       is set to produce a total noise at the collector
*                       which is greater than the generator noise at the
*                       collector by the rated number of decibels.
*
*$
.model Q2N2222A NPN(Is=14.34f Xti=3 Eg=1.11 Vaf=74.03 Bf=255.9 Ne=1.307
+               Ise=14.34f Ikf=.2847 Xtb=1.5 Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.5 Cje=22.01p Mje=.377 Vje=.75
+               Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=10)
*               National        pid=19                  case=TO18
```

```
*               88-09-07 bam creation
*$
.model Q2N2907A PNP(Is=650.6E-18 Xti=3 Eg=1.11 Vaf=115.7 Bf=231.7 Ne=1.829
+               Ise=54.81f Ikf=1.079 Xtb=1.5 Br=3.563 Nc=2 Isc=0 Ikr=0 Rc=.715
+               Cjc=14.76p Mjc=.5383 Vjc=.75 Fc=.5 Cje=19.82p Mje=.3357 Vje=.75
+               Tr=111.3n Tf=603.7p Itf=.65 Vtf=5 Xtf=1.7 Rb=10)
*               National        pid=63                  case=TO18
*               88-09-09 bam creation
*$
.model Q2N3904      NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
*               National        pid=23                  case=TO92
*               88-09-08 bam creation
*$
.model Q2N3906      PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0
+               Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p
+               Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n
+               Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)
*               National        pid=66                  case=TO92
*               88-09-09 bam creation
*$
*--------------------------------------------------------------------------------
* Library of diode model parameters
*
* Copyright 1992 by MicroSim Corporation
* This is a reduced version of MicroSim's diode model library.
*   You are welcome to make as many copies of it as you find convenient.
*
* The parameters in this model library were derived from the data sheets for
* each part.  Most parts were characterize using the Parts option.
* Devices can also be characterized without Parts as follows:
*       IS              nominal leakage current
*       RS              for zener diodes: nominal small-signal impedance
*                       at specified operating current
*       IB              for zener diodes: set to nominal leakage current
*       IBV             for zener diodes: at specified operating current
*                       IBV is adjusted to give the rated zener voltage
*
*
*** Zener Diodes ***
*
* "A" suffix zeners have the same parameters (e.g., 1N750A has the same
* parameters as 1N750)
*
*$
.model D1N750       D(Is=880.5E-18 Rs=.25 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=175p
M=.5516
+               Vj=.75 Fc=.5 Isr=1.859n Nr=2 Bv=4.7 Ibv=20.245m Nbv=1.6989
+               Ibvl=1.9556m Nbvl=14.976 Tbv1=-21.277u)
*               Motorola        pid=1N750     case=DO-35
*               89-9-18 gjg
```

```
*               Vz = 4.7 @ 20mA, Zz = 300 @ 1mA, Zz = 12.5 @ 5mA, Zz =2.6  @
20mA

*$
.model D1N5229  D(Is=880.5E-18 Rs=.25 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=190p
M=.6124
+               Vj=.75 Fc=.5 Isr=1.743n Nr=2 Bv=4.3 Ibv=16.748m Nbv=1.7936
+               Ibvl=5.0382m Nbvl=12.554 Tbv1=-232.56u)
*               Motorola        pid=1N5229   case=DO-35
*               89-9-18 gjg
*               Vz = 4.3 @ 20mA, Zz = 325 @ 1mA, Zz = 24 @ 5mA, Zz = 3.2 @ 20mA



*$
*** Voltage-variable capacitance diodes

* The parameters in this model library were derived from the data sheets for
* each part.  Each part was characterize using the Parts option.
*$
.model MV2201   D(Is=1.365p Rs=1 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=14.93p M=.4261
+               Vj=.75 Fc=.5 Isr=16.02p Nr=2 Bv=25 Ibv=10u)
*               Motorola        pid=MV2201   case=182-03
*               88-09-22 bam creation

*** Switching Diodes ***
*$
.model D1N914       D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
*$
.model D1N914A      D(Is=0.1p Rs=4 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
*$
.model D1N4148      D(Is=0.1p Rs=16 CJO=2p Tt=12n Bv=100 Ibv=0.1p)
*$
.model MBD101   D(Is=192.1p Rs=.1 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=893.8f M=98.29m
+               Vj=.75 Fc=.5 Isr=16.91n Nr=2 Bv=5 Ibv=10u)
*               Motorola        pid=MBD101  case=182-03
*               88-09-22 bam creation


*** Power Diodes ***
*$
.model D1N4009      D(Is=0.1p Rs=4 CJO=2p Tt=3n Bv=60 Ibv=0.1p)
*               85-??-??        Original library
*$
*---------------------------------------------------------------------------
* Library of junction field-effect transistor (JFET) model parameters

* This is a reduced version of MicroSim's JFET model library.
*   You are welcome to make as many copies of it as you find convenient.

* The parameters in this model library were derived from the data sheets for
* each part.  Each part was characterize using the Parts option.
*$
.model J2N3819      NJF(Beta=1.304m Betatce=-.5 Rd=1 Rs=1 Lambda=2.25m Vto=-3
```

```
+               Vtotc=-2.5m Is=33.57f Isr=322.4f N=1 Nr=2 Xti=3 Alpha=311.7
+               Vk=243.6 Cgd=1.6p M=.3622 Pb=1 Fc=.5 Cgs=2.414p Kf=9.882E-18
+               Af=1)
*               National        pid=50                  case=TO92
*               88-08-01 rmn  BVmin=25
*$
.model J2N4393        NJF(Beta=9.109m Betatce=-.5 Rd=1 Rs=1 Lambda=6m Vto=-
1.422
+               Vtotc=-2.5m Is=205.2f Isr=1.988p N=1 Nr=2 Xti=3 Alpha=20.98u
+               Vk=123.7 Cgd=4.57p M=.4069 Pb=1 Fc=.5 Cgs=4.06p Kf=123E-18
+               Af=1)
*               National        pid=51                  case=TO18
*               88-07-13 bam  BVmin=40
*$
.model J2N5457        NJF(Beta=1.125m Betatce=-.5 Rd=1 Rs=1 Lambda=2.3m Vto=-
1.372
+               Vtotc=-2.5m Is=181.3f Isr=1.747p N=1 Nr=2 Xti=3 Alpha=2.543u
+               Vk=152.2 Cgd=4p M=.3114 Pb=.5 Fc=.5 Cgs=4.627p Kf=10.45E-18
+               Af=1)
*               National        pid=55                  case=TO92
*               88-08-03 rmn  BVmin=25

*$
*---------------------------------------------------------------------------
* Library of linear IC definitions

* This is a reduced version of MicroSim's linear subcircuit library.
*   You are welcome to make as many copies of it as you find convenient.
*
* The parameters in the opamp library were derived from the data sheets for
* each part.  The macromodel used is similar to the one described in:
*
*       Macromodeling of Integrated Circuit Operational Amplifiers
*         by Graeme Boyle, Barry Cohn, Donald Pederson, and James Solomon
*       IEEE Journal of SoliE-State Circuits, Vol. SC-9, no. 6,       Dec. 1974
*
* Differences from the reference (above) occur in the output limiting stage
* which was modified to reduce internally generated currents associated with
* output voltage limiting, as well as short-circuit current limiting.
*
* The opamps are modelled at room temperature and do not track changes with
* temperature.  This library file contains models for nominal, not worst case,
* devices.
*
*$
*---------------------------------------------------------------------------
* connections:  non-inverting input
*               | inverting input
*               | | positive power supply
*               | | | negative power supply
*               | | | | output
*               | | | | |
.subckt LM318   1 2 3 4 5
*
```

```
 c1   11 12 2.887E-12
 c2    6  7 20.00E-12
 dc    5 53 dx
 de   54  5 dx
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 636.5E3 -600E3 600E3 600E3 -600E3
 ga    6  0 11 12 12.57E-3
 gcm   0  6 10 99 125.7E-9
 iee  10  4 dc 1.400E-3
 hlim 90  0 vlim 1K
 q1   11  2 13 qx
 q2   12  1 14 qx
 r2    6  9 100.0E3
 rc1   3 11 79.57
 rc2   3 12 79.57
 re1  13 10 42.61
 re2  14 10 42.61
 ree  10 99 142.8E3
 ro1   8  5 50
 ro2   7 99 25
 rp    3  4 9.678E3
 vb    9  0 dc 0
 vc    3 53 dc 2
 ve   54  4 dc 2
 vlim  7  8 dc 0
 vlp  91  0 dc 22
 vln   0 92 dc 22
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=4.667E3)
.ends
*$
*--------------------------------------------------------------------------------
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt LM324    1 2 3 4 5
*
 c1   11 12 2.887E-12
 c2    6  7 30.00E-12
 dc    5 53 dx
 de   54  5 dx
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 21.22E6 -20E6 20E6 20E6 -20E6
 ga    6  0 11 12 188.5E-6
 gcm   0  6 10 99 59.61E-9
```

```
 iee   3 10 dc 15.09E-6
 hlim 90  0 vlim 1K
 q1   11  2 13 qx
 q2   12  1 14 qx
 r2    6  9 100.0E3
 rc1   4 11 5.305E3
 rc2   4 12 5.305E3
 re1  13 10 1.845E3
 re2  14 10 1.845E3
 ree  10 99 13.25E6
 ro1   8  5 50
 ro2   7 99 25
 rp    3  4 9.082E3
 vb    9  0 dc 0
 vc    3 53 dc 1.500
 ve   54  4 dc 0.65
 vlim  7  8 dc 0
 vlp  91  0 dc 40
 vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx PNP(Is=800.0E-18 Bf=166.7)
.ends
*$
*-------------------------------------------------------------------------------
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt uA741    1 2 3 4 5
*
 c1   11 12 8.661E-12
 c2    6  7 30.00E-12
 dc    5 53 dx
 de   54  5 dx
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -10E6 10E6 10E6 -10E6
 ga    6  0 11 12 188.5E-6
 gcm   0  6 10 99 5.961E-9
 iee  10  4 dc 15.16E-6
 hlim 90  0 vlim 1K
 q1   11  2 13 qx
 q2   12  1 14 qx
 r2    6  9 100.0E3
 rc1   3 11 5.305E3
 rc2   3 12 5.305E3
 re1  13 10 1.836E3
 re2  14 10 1.836E3
 ree  10 99 13.19E6
 ro1   8  5 50
```

```
 ro2   7 99 100
 rp    3  4 18.16E3
 vb    9  0 dc 0
 vc    3 53 dc 1
 ve   54  4 dc 1
 vlim  7  8 dc 0
 vlp  91  0 dc 40
 vln   0 92 dc 40
.model dx D(Is=800.0E-18 Rs=1)
.model qx NPN(Is=800.0E-18 Bf=93.75)
.ends
*$
*-------------------------------------------------------------------------------
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt LF411    1 2 3 4 5
*
 c1   11 12 4.196E-12
 c2    6  7 10.00E-12
 css  10 99 1.333E-12
 dc    5 53 dx
 de   54  5 dx
 dlp  90 91 dx
 dln  92 90 dx
 dp    4  3 dx
 egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
 fb    7 99 poly(5) vb vc ve vlp vln 0 31.83E6 -30E6 30E6 30E6 -30E6
 ga    6  0 11 12 251.4E-6
 gcm   0  6 10 99 2.514E-9
 iss  10  4 dc 170.0E-6
 hlim 90  0 vlim 1K
 j1   11  2 10 jx
 j2   12  1 10 jx
 r2    6  9 100.0E3
 rd1   3 11 3.978E3
 rd2   3 12 3.978E3
 ro1   8  5 50
 ro2   7 99 25
 rp    3  4 15.00E3
 rss  10 99 1.176E6
 vb    9  0 dc 0
 vc    3 53 dc 1.500
 ve   54  4 dc 1.500
 vlim  7  8 dc 0
 vlp  91  0 dc 25
 vln   0 92 dc 25
.model dx D(Is=800.0E-18 Rs=1m)
.model jx NJF(Is=12.50E-12 Beta=743.3E-6 Vto=-1)
.ends
*$
```

```
*--------------------------------------------------------------------------

*** Voltage comparators

* The parameters in this comparator library were derived from data sheets for
* each parts. The macromodel used was developed by MicroSim Corporation, and
* is produced by the "Parts" option to PSpice.
*
* Although we do not use it, another comparator macro model is described in:
*
*       An Integrated-Circuit Comparator Macromodel
*         by Ian Getreu, Andreas Hadiwidjaja, and Johan Brinch
*       IEEE Journal of Solid-State Circuits, Vol. SC-11, no. 6, Dec. 1976
*
* This reference covers the considerations that go into duplicating the
* behavior of voltage comparators.
*
* The comparators are modelled at room temperature. The macro model does not
* track changes with temperature. This library file contains models for
* nominal, not worst case, devices.
*
*$
*--------------------------------------------------------------------------
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | open collector output
*                | | | | | output ground
*                | | | | | |
.subckt LM111    1 2 3 4 5 6
*
 f1   9  3 v1 1
 iee  3  7 dc 100.0E-6
 vi1  21  1 dc .45
 vi2  22  2 dc .45
 q1   9 21  7 qin
 q2   8 22  7 qin
 q3   9  8  4 qmo
 q4   8  8  4 qmi
.model qin PNP(Is=800.0E-18 Bf=833.3)
.model qmi NPN(Is=800.0E-18 Bf=1002)
.model qmo NPN(Is=800.0E-18 Bf=1000 Cjc=1E-15 Tr=118.8E-9)
 e1   10  6  9  4  1
 v1   10 11 dc 0
 q5   5 11  6 qoc
.model qoc NPN(Is=800.0E-18 Bf=34.49E3 Cjc=1E-15 Tf=364.6E-12 Tr=79.34E-9)
 dp   4  3 dx
 rp   3  4 6.122E3
.model dx  D(Is=800.0E-18 Rs=1)
*
.ends
*$
*--------------------------------------------------------------------------
```

```
* Library of magnetic core model parameters

* This is a reduced version of MicroSim's magnetic core library.
*   You are welcome to make as many copies of it as you find convenient.

* The parameters in this model library were derived from the data sheets for
* each core. The Jiles-Atherton magnetics model is described in:
*
*   Theory of Ferromagnetic Hysteresis, by D C Jiles and D L Atherton,
*   Journal of Magnetism and Magnetic Materials, vol 61 (1986) pp 48-60
*
* Model parameters for ferrite material (Ferroxcube 3C8) were obtained by
* trial simulations, using the B-H curves from the manufacturer's catalog.
* Then, the library was compiled from the data sheets for each core geometry.
* Notice that only the geometric values change once a material is
* characterized.

* Example use:  K2 L2 .99 K1409PL_3C8

* Notes:
*   1) Using a K device (formerly only for mutual coupling) with a model
*   reference changes the meaning of the L device: the inductance value
*   becomes the number of turns for the winding.
*   2) K devices can "get away" with specifying only one inductor, as in the
*   example above, to simulate power inductors.

* Example circuit file:

*+-------------------------------------------------------------------------
*|Demonstration of power inductor B-H curve
*|
*|* To view results with Probe (B-H curve):
*|* 1) Add Trace for B(K1)
*|* 2) set X-axis variable to H(K1)
*|*
*|* Probe x-axis unit is Oersted
*|* Probe y-axis unit is Gauss
*|*
*|.tran .1 4
*|igen0 0 1 sin(0 .1amp 1Hz 0)        ; Generator: starts with 0.1 amp sinewave, then
*|igen1 0 1 sin(0 .1amp 1Hz 1)        ;  +0.1 amps, starting at 1 second
*|igen2 0 1 sin(0 .2amp 1Hz 2)        ;  +0.2 amps, starting at 2 seconds
*|igen3 0 1 sin(0 .8amp 1Hz 3)        ;  +0.4 amps, starting at 3 seconds
*|RL 1 0 1ohm                         ; generator source resistance
*|L1 1 0 20                    ; inductor with 20 turns
*|K1 L1 .9999 K528T500_3C8        ; Ferroxcube torroid core
*|.model K528T500_3C8  Core(LEVEL=2 ALPHA=0 MS=415.2K A=44.82 C=.4112
K=25.74
*|+                                AREA=1.17 PATH=8.49)
*|.options itl5=0
*|.probe
*|.end
*+-------------------------------------------------------------------------
```

```
*** Ferroxcube pot cores: 3C8 material
*$
.model K3019PL_3C8          Core(Level=2 Alpha=0 MS=415.2K A=44.82 C=.4112
K=25.74
+                       Area=1.38 Path=4.52)

*** Ferroxcube square cores: 3C8 material
*$
.model KRM8PL_3C8    Core(Level=2 Alpha=0 MS=415.2K A=44.82 C=.4112
K=25.74
+                       Area=.630 Path=3.84)

*** Ferroxcube toroid cores: 3C8 material
*$
.model K502T300_3C8         Core(Level=2 Alpha=0 MS=415.2K A=44.82 C=.4112
K=25.74
+                       Area=.371 Path=7.32)
.model K528T500_3C8         Core(Level=2 Alpha=0 MS=415.2K A=44.82 C=.4112
K=25.74
+                  Area=1.17 Path=8.49)
*$
*---------------------------------------------------------------------------
* Library of MOSFET model parameters (for "power" MOSFET devices)
*
* This is a reduced version of MicroSim's power MOSFET model library.
*   You are welcome to make as many copies of it as you find convenient.
*
* The parameters in this model library were derived from the data sheets for
* each part.  Each part was characterize using the Parts option.
* Device can also be characterized without Parts as follows:
*       LEVEL                   Set to 3 (short-channel device).
*       TOX             Determined from gate ratings.
*       L, LD, W, WD            Assume L=2u.  Calculate from input capacitance.
*       XJ, NSUB        Assume usual technology.
*       IS, RD, RB      Determined from "source-drain diode forward voltage"
*                       specification or curve (Idr vs. Vsd).
*       RS              Determine from Rds(on) specification.
*       RDS             Calculated from Idss specification or curves.
*       VTO, UO, THETA      Determined from "output characteristics" curve family
*                       (Ids vs. Vds, stepped Vgs).
*       ETA, VMAX, CBS      Set for null effect.
*       CBD, PB, MJ             Determined from "capacitance vs. Vds" curves.
*       RG              Calculate from rise/fall time specification or curves.
*       CGSO, CGDO              Determined from gate-charge, turn-on/off delay and
*                       rise time specifications.
*
* NOTE:         when specifying the instance of a device in your circuit file:
*
*       BE SURE to have the source and bulk nodes connected together, as this
*       is the way the real device is constructed.
*
*       DO NOT include values for L, W, AD, AS, PD, PS, NRD, or NDS.
*       The PSpice default values for these parameters are taken into account
*       in the library model statements.  Of course, you should NOT reset
```

```
*       the default values using the .OPTIONS statement, either.
*
* Example use:          M17    15 23 7 7       IRF150
*
* - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
*
* The "power" MOSFET device models benefit from relatively complete specifi-
* cation of static and dynamic characteristics by their manufacturers.  The
* following effects are modeled:
*       - DC transfer curves in forward operation,
*       - gate drive characteristics and switching delay,
*       - "on" resistance,
*       - reverse-mode "body-diode" operation.
*
* The factors not modeled include:
*       - maximum ratings (eg. high-voltage breakdown),
*       - safe operating area (eg. power dissipation),
*       - latch-up,
*       - noise.
*
* For high-current switching applications, we advise that you include
* series inductance elements, for the source and drain, in your circuit file.
* In doing so, voltage spikes due to di/dt will be modeled.  According to the
* 1985 International Rectifier databook, the following case styles have lead
* inductance values of:
*       TO-204 (modified TO-3)      source = 12.5nH             drain = 5.0nH
*       TO-220                      source =  7.5nH             drain = 3.5-4.5nH
* - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
*$
.model IRF150          NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+               Tox=100n Uo=600 Phi=.6 Rs=1.624m Kp=20.53u W=.3 L=2u
Vto=2.831
+             Rd=1.031m Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5 Cgso=9.027n
+               Cgdo=1.679n Rg=13.89 Is=194E-18 N=1 Tt=288n)
*               Int'l Rectifier  pid=IRFC150 case=TO3
*               88-08-25 bam creation
*$
.model IRF9140         PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
Vmax=0 Xj=0
+               Tox=100n Uo=300 Phi=.6 Rs=70.6m Kp=10.15u W=1.9 L=2u Vto=-
3.67
+               Rd=60.66m Rds=444.4K Cbd=2.141n Pb=.8 Mj=.5 Fc=.5 Cgso=877.2p
+               Cgdo=369.3p Rg=.811 Is=52.23E-18 N=2 Tt=140n)
*               Int'l Rectifier  pid=IRFC9140          case=TO3
*               88-08-25 bam creation
*$
*-------------------------------------------------------------------------
* Library of digital logic

* Copyright 1992 by MicroSim Corporation
* This is a reduced version of MicroSim's Digital components library.
*   You are welcome to make as many copies of it as you find convenient.
*
```

```
* The parameters in this model library were derived from:
*
*  The TTL Data Book, Texas Instruments, 1985
*    vol. 2
*
* Each device is modeled by a subcircuit. The interface pins of the
* subcircuit have the same name as the pin labels in the data book. The
* general order is inputs followed by outputs, but on the more complex
* devices you will have to look at the subcircuit definition.
* The word "BAR" is appended to inverted inputs or outputs.
*
* There are two optional power supply pins for each digital subcircuit.
* You do not need to specify these if you are using a 5v supply with
* analog and digital ground connected. If you use another power supply
* configuration, then the pins should be connected to that supply.
*
* The timing charactistics from the data book are included in the models,
* with all data sheet effects modeled, unless noted in this file.
*
* If a device contains multiple, independant, identical functions, only
* one is contained in the subcircuit. (e.g. the 7400 contains four two-
* input NAND gates, but there is only one in the 7400 subckt.)
*
* The subcircuit name is the part name.  Only the 74 series (not the 54
* series) is included in the library, except for a few parts which
* are only made in the 54 series. (e.g. 54L00)
*---------------------------------------------------------------------
*$
* 7402  Quadruple 2-input Positive-Nor Gates
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/23/89        Update interface and model names

.subckt 7402  A B Y
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
U1 nor(2) DPWR DGND
+       A B  Y
+       D_02 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_02 ugate (
+       tplhty=12ns     tplhmx=22ns
+       tphlty=8ns      tphlmx=15ns
+       )
*---------------------------------------------------------------------
*$
* 7404  Hex Inverters
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/23/89        Update interface and model names

.subckt 7404  A Y
+       optional: DPWR=$G_DPWR DGND=$G_DGND
```

```
+       params: MNTYMXDLY=0 IO_LEVEL=0
U1 inv DPWR DGND
+       A  Y
+       D_04 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_04 ugate (
+       tplhty=12ns     tplhmx=22ns
+       tphlty=8ns      tphlmx=15ns
+       )
*---------------------------------------------------------------------
*$
* 7405  Hex Inverters with Open-Collector Outputs
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/23/89        Update interface and model names

.subckt 7405  A Y
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
U1 inv DPWR DGND
+       A  Y
+       D_05 IO_STD_OC MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_05 ugate (
+       tplhty=40ns     tplhmx=55ns
+       tphlty=8ns      tphlmx=15ns
+       )
*---------------------------------------------------------------------
*$
* 7414  Hex Schmitt-Trigger Inverters
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/23/89        Update interface and model names

.subckt 7414  A Y
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
* Note: These devices are modeled as simple inverters
*       Hysteresis is modeled in the AtoD interface

U1 inv DPWR DGND
+       A  Y
+       D_14 IO_STD_ST MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_14 ugate (
+       tplhty=15ns     tplhmx=22ns
+       tphlty=15ns     tphlmx=22ns
+       )
*---------------------------------------------------------------------
*$
* 7474  Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear
```

```
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/28/89        Update interface and model names

.subckt 7474  1CLRBAR 1D 1CLK 1PREBAR 1Q 1QBAR
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
UFF1 dff(1) DPWR DGND
+       1PREBAR 1CLRBAR 1CLK   1D   1Q 1QBAR
+       D_74 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_74 ueff (
+       twpclmn=30ns          twclklmn=37ns
+       twclkhmn=30ns         tsudclkmn=20ns
+       thdclkmn=5ns          tppcqlhmx=25ns
+       tppcqhlmx=40ns        tpclkqlhty=14ns
+       tpclkqlhmx=25ns       tpclkqhlty=20ns
+       tpclkqhlmx=40ns
+       )
*---------------------------------------------------------------------
*$
* 74107  Dual J-K Flip-Flops with Clear
*
* The TTL Data Book, Vol 2, 1985, TI
* tdn   06/29/89        Update interface and model names

.subckt 74107  CLK CLRBAR J K Q QBAR
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
UIBUF bufa(3) DPWR DGND
+       CLRBAR J K   CLRBAR_BUF J_BUF K_BUF
+       D0_GATE IO_STD IO_LEVEL={IO_LEVEL}
U2BUF buf DPWR DGND
+       CLK   CLK_BUF
+       D_107_4 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
U1 srff(1) DPWR DGND
+       $D_HI CLRBAR_BUF CLK_BUF   W1 W2   Y YB
+       D_107_1 IO_STD MNTYMXDLY={MNTYMXDLY}
U2 srff(1) DPWR DGND
+       $D_HI CLRBAR_BUF CLKBAR   Y YB   QBUF QBAR_BUF
+       D_107_2 IO_STD MNTYMXDLY={MNTYMXDLY}
U3 inva(3) DPWR DGND
+       CLK_BUF J_BUF K_BUF   CLKBAR JB KB
+       D0_GATE IO_STD
U4 ao(3,2) DPWR DGND
+       J_BUF K_BUF QBAR_BUFD J_BUF KB $D_HI   W1
+       D_107_3 IO_STD MNTYMXDLY={MNTYMXDLY}
U5 ao(3,2) DPWR DGND
+       J_BUF K_BUF QBUFD JB K_BUF $D_HI   W2
+       D_107_3 IO_STD MNTYMXDLY={MNTYMXDLY}
UBUF bufa(4) DPWR DGND
+       QBUF QBAR_BUF QBUF QBAR_BUF   Q QBAR QBUFD QBAR_BUFD
+       D_107_3 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
```

```
.ends

.model D_107_1 ugff (
+       twghmx=19ns         twghty=19ns
+       twpclmx=47ns        twpclty=47ns
+       )
.model D_107_2 ugff (
+       tppcqlhty=10ns      tppcqlhmx=19ns
+       tppcqhlty=19ns      tppcqhlmx=34ns
+       tpgqlhty=10ns       tpgqlhmx=19ns
+       tpgqhlty=19ns       tpgqhlmx=34ns
+       twghmx=20ns         twghty=20ns
+       twpclmx=47ns        twpclty=47ns
+       )
.model D_107_3 ugate (
+       tplhty=6ns    tplhmx=6ns
+       tphlty=6ns    tphlmx=6ns
+       )
.model D_107_4 ugate (
+       tplhmn=6ns    tplhmx=6ns
+       )
*---------------------------------------------------------------------
*$
* 74393  Dual 4-bit Binary Counter with Individual Clocks
*
* The TTL Data Book, Vol 2, 1985, TI
* atl   7/18/89   Update interface and model names

.subckt 74393  A CLR QA QB QC QD
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params: MNTYMXDLY=0 IO_LEVEL=0
UINV inv DPWR DGND
+       CLR  CLRBAR
+       D0_GATE IO_STD IO_LEVEL={IO_LEVEL}
U1 jkff(1) DPWR DGND
+       $D_HI CLRBAR A  $D_HI $D_HI  QA_BUF $D_NC
+       D_393_1 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
U2 jkff(1) DPWR DGND
+       $D_HI CLRBAR QA_BUF  $D_HI $D_HI  QB_BUF $D_NC
+       D_393_2 IO_STD MNTYMXDLY={MNTYMXDLY}
U3 jkff(1) DPWR DGND
+       $D_HI CLRBAR QB_BUF  $D_HI $D_HI  QC_BUF $D_NC
+       D_393_2 IO_STD MNTYMXDLY={MNTYMXDLY}
U4 jkff(1) DPWR DGND
+       $D_HI CLRBAR QC_BUF  $D_HI $D_HI  QD_BUF $D_NC
+       D_393_3 IO_STD MNTYMXDLY={MNTYMXDLY}
UBUFF bufa(4) DPWR DGND
+       QA_BUF QB_BUF QC_BUF QD_BUF  QA QB QC QD
+       D_393_4 IO_STD MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends

.model D_393_1 ueff (
+       tppcqhlty=18ns      tppcqhlmx=33ns
+       tpclkqlhty=6ns      tpclkqlhmx=14ns
```

```
+       tpclkqhlty=7ns          tpclkqhlmx=14ns
+       twclkhmn=20ns           twclklmn=20ns
+       twpclmn=20ns            tsudclkmn=25ns
+       )
.model D_393_2 ueff ()
.model D_393_3 ueff (
+       tpclkqlhty=27ns         tpclkqlhmx=40ns
+       tpclkqhlty=27ns         tpclkqhlmx=40ns
+       )
.model D_393_4 ugate (
+       tphlty=6ns      tphlmx=6ns
+       tplhty=6ns      tplhmx=6ns
+       )
*$
* AtoD and DtoA Subcircuits
* -------------------------
* The subcircuits in this library are used to convert analog signals
* into digital signals (AtoD) and digital signals into analog signals
* (DtoA). The PSpice Digital Simulation Option creates "X" devices which
* reference these subcircuits whenever it needs to convert a digital or
* analog signal. The user usually will not need to use these subcircuits
* directly. However, if you need to add new AtoD or DtoA subcircuits, the
* interface nodes must be in the following order, and have the following
* parameters:
*
*   AtoD: .subckt <name> <analog-node> <dig-node> <dig-pwr> <dig-gnd>
*         +         params: CAPACITANCE=0
*
*   DtoA: .subckt <name> <dig-node> <analog-node> <dig-pwr> <dig-gnd>
*         +         params: DRVL=0  DRVH=0  CAPACITANCE=0
*
* I/O Models
* ----------
* I/O models specify the names of the AtoD and DtoA subcircuits PSpice must
* use to convert analog signals to digital signals or vice versa. (I/O models
* also describe driving and loading characteristics.) Up to four of each
* AtoD and DtoA subcircuit names may be specified in an I/O model, using
* parameters AtoD1 through AtoD4, and DtoA1 through DtoA4. The subcircuit
* which PSpice actually uses depends on the value of the IO_LEVEL parameter
* in a subcircuit reference.
*
* As implemented in this library, the levels have the following definitions:
*
*   IO_LEVEL  Definition
*   --------  ----------------------------------------------------------
*      1      Basic (simple) model with X, R, and F between VIL max and VIH min (AtoD)
*      2      Basic (simple) model without intermediate X value
*      3      Elaborate model with X between VIL max and VIH min (AtoD)
*      4      Elaborate model without intermediate X, R, and F value
*
* The Elaborate model has a more accurate I-V curve, including clamping
* diodes, but since it has more devices, it can take longer to simulate
* when it is used.
*
```

```
* For example, to specify the basic interface without an intermediate
* X value, you would use:
*
* X1 in out 74LS04 PARAMS: IO_LEVEL=2
*
* If the IO_LEVEL is not specified for a device, the default IO_LEVEL is used.
* The default level is controled by the .OPTION parameter DIGIOLVL, which
* defaults to 1.
*

*$
*-------------------------------------------------------------------------
* Digital Power Supply
*-------------------------------------------------------------------------

*  PSpice automatically creates one instance of this subcircuit if any
*  AtoD or DtoA interfaces are created.  PSpice always uses node 0 as the
*  required analog reference node "GND".  The digital power and ground
*  nodes default to global nodes named $G_DPWR and $G_DGND, which are
*  used throughout the digital libraries.  The default output is 5.0v.
*
*  To create your own power supply, simply create an instance of this
*  subcircuit, using your own digital power and ground node names, and
*  the desired voltage.  For example:
*
*  XMYPOWER 0 MY_PWR MY_GND DIGIFPWR params: VOLTAGE=3.5V
*

.subckt DIGIFPWR  AGND
+       optional: DPWR=$G_DPWR DGND=$G_DGND
+       params:   VOLTAGE=5.0v REFERENCE=0v
*
VDPWR  DPWR DGND  {VOLTAGE}
R1     DPWR AGND  1MEG
VDGND  DGND REF   {REFERENCE}
R2     REF  AGND  1E-6
R3     DGND AGND  1MEG
.ends

*$
*-------------------------------------------------------------------------
* Stimulus Device Models and Subcircuits
*-------------------------------------------------------------------------

*-----------------------------------------------
* Stimulus I/O Models

.model IO_STM uio (
+       drvh=0          drvl=0
+       DtoA1="DtoA_STM" DtoA2="DtoA_STM"
+       DtoA3="DtoA_STM" DtoA4="DtoA_STM"
+       )
.model IO_STM_OC uio (
+       drvh=1MEG    drvl=0
```

```
+       DtoA1="DtoA_STM_OC"     DtoA2="DtoA_STM_OC"
+       DtoA3="DtoA_STM_OC"     DtoA4="DtoA_STM_OC"
+       )

*-----------------------------------------------
* Stimulus DtoA Subcircuit

.subckt DtoA_STM  D A  DPWR DGND
+       params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1  A DGND DPWR DINSTM DGTLNET=D IO_STM
C1  A 0 {CAPACITANCE+0.1pF}
.ends

*-----------------------------------------------
* Stimulus Open Collector DtoA Subcircuit

.subckt DtoA_STM_OC  D A  DPWR DGND
+       params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1  A DGND DPWR DINSTM_OC DGTLNET=D IO_STM_OC
C1  A 0 {CAPACITANCE+0.1pF}
.ends

*-----------------------------------------------
* Stimulus Digital Input/Output Models
*
* We use 1/2 ohm and a 500ps transition time, on the assumption that
* this will be a "strong" signal source with a "fast" switching time
* in most systems which use this library. Change the tsw's and/or the
* rlow and rhi values if these don't work for your system.
*
.model DINSTM dinput (
+       s0name="0"   s0tsw=0.5ns  s0rlo=.5       s0rhi=1k
+       s1name="1"   s1tsw=0.5ns  s1rlo=1k       s1rhi=.5
+       s2name="X"   s2tsw=0.5ns  s2rlo=0.429    s2rhi=1.16 ; .313ohm, 1.35v
+       s3name="R"   s3tsw=0.5ns  s3rlo=0.429    s3rhi=1.16 ; .313ohm, 1.35v
+       s4name="F"   s4tsw=0.5ns  s4rlo=0.429    s4rhi=1.16 ; .313ohm, 1.35v
+       s5name="Z"   s5tsw=0.5ns  s5rlo=1MEG     s5rhi=1MEG
+       )
.model DINSTM_OC dinput (
+       s0name="0"   s0tsw=0.5ns  s0rlo=.5       s0rhi=1k
+       s1name="1"   s1tsw=0.5ns  s1rlo=1MEG     s1rhi=1MEG
+       s2name="X"   s2tsw=0.5ns  s2rlo=0.429    s2rhi=1.16 ; .313ohm, 1.35v
+       s3name="R"   s3tsw=0.5ns  s3rlo=0.429    s3rhi=1.16 ; .313ohm, 1.35v
+       s4name="F"   s4tsw=0.5ns  s4rlo=0.429    s4rhi=1.16 ; .313ohm, 1.35v
+       s5name="Z"   s5tsw=0.5ns  s5rlo=1MEG     s5rhi=1MEG
+       )


*-------------------------------------------------------------------------
* Zero-Delay Models
*-------------------------------------------------------------------------
```

```
*---------------------------------------------
* Zero-Delay Gate Model

.model D0_GATE ugate ()

*---------------------------------------------
* Zero-Delay Tristate Gate Model

.model D0_TGATE utgate ()

*---------------------------------------------
* Zero-Delay Edge-Triggered Flip-Flop Model

.model D0_EFF ueff ()

*---------------------------------------------
* Zero-Delay Gated Flip-Flop Model

.model D0_GFF ugff ()


*********************************************************************************
******
* 74/54 Family (standard TTL)
*********************************************************************************
******

*---------------------------------------------
* 7400 I/O Models

.model IO_STD uio (
+       drvh=96.4     drvl=104
+       AtoD1="AtoD_STD"  AtoD2="AtoD_STD_NX"
+       AtoD3="AtoD_STD_E"       AtoD4="AtoD_STD_NXE"
+       DtoA1="DtoA_STD"  DtoA2="DtoA_STD"
+       DtoA3="DtoA_STD"  DtoA4="DtoA_STD"
+       )
.model IO_STD_ST uio (
+       drvh=96.4     drvl=104
+       AtoD1="AtoD_STD_ST"      AtoD2="AtoD_STD_ST"
+       AtoD3="AtoD_STD_ST_E"   AtoD4="AtoD_STD_ST_E"
+       DtoA1="DtoA_STD"  DtoA2="DtoA_STD"
+       DtoA3="DtoA_STD"  DtoA4="DtoA_STD"
+       )
.model IO_STD_OC uio (
+       drvh=1MEG   drvl=104
+       AtoD1="AtoD_STD"  AtoD2="AtoD_STD_NX"
+       AtoD3="AtoD_STD_E"       AtoD4="AtoD_STD_NXE"
+       DtoA1="DtoA_STD_OC"      DtoA2="DtoA_STD_OC"
+       DtoA3="DtoA_STD_OC"      DtoA4="DtoA_STD_OC"
+       )

*---------------------------------------------
* 7400 Standard AtoD Subcircuits
```

```
* Simple Models:

.subckt AtoD_STD  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74 DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
.ends

.subckt AtoD_STD_NX  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74_NX DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
.ends

* Elaborate Models:

.subckt AtoD_STD_E  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74 DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
D0      DGND            a       D74CLMP
D1      1       2       D74
D2      2       DGND    D74
R1      DPWR            3       4k
Q1      1       3       A       0       Q74 ; substrait should be DGND
.ends

.subckt AtoD_STD_NXE  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74_NX DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
D0      DGND            a       D74CLMP
D1      1       2       D74
D2      2       DGND    D74
R1      DPWR            3       4k
Q1      1       3       A       0       Q74 ; substrait should be DGND
.ends

*--------------------------------------------------
* 7400 Schmidt trigger AtoD Subcircuits

* Simple Model:

.subckt AtoD_STD_ST  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74_ST DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
.ends
```

```
* Elaborate Model:

.subckt AtoD_STD_ST_E  A D  DPWR DGND
+       params: CAPACITANCE=0
*
O0  A DGND DO74_ST DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
D0      DGND        a       D74CLMP
D1      1       2       D74
D2      2       DGND    D74
R1      DPWR        3       4k
Q1      1       3       A       0       Q74
.ends

*-------------------------------------------------
* 7400 standard DtoA Subcircuit

.subckt DtoA_STD  D A  DPWR DGND
+       params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1  A DGND DPWR DIN74 DGTLNET=D IO_STD
C1  A 0 {CAPACITANCE+0.1pF}
.ends

*-------------------------------------------------
* 7400 open collector DtoA Subcircuit

.subckt DtoA_STD_OC  D A  DPWR DGND
+       params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1  A DGND DPWR DIN74_OC DGTLNET=D IO_STD_OC
C1  A 0 {CAPACITANCE+0.1pF}
.ends

*-------------------------------------------------
* 7400 Digital Input/Output Models

.model DIN74 dinput (
+       s0name="0"   s0tsw=3.5ns  s0rlo=7.13    s0rhi=389 ; 7ohm,   0.09v
+       s1name="1"   s1tsw=5.5ns  s1rlo=467     s1rhi=200 ; 140ohm,  3.5v
+       s2name="X"   s2tsw=3.5ns  s2rlo=42.9    s2rhi=116 ; 31.3ohm, 1.35v
+       s3name="R"   s3tsw=3.5ns  s3rlo=42.9    s3rhi=116 ; 31.3ohm, 1.35v
+       s4name="F"   s4tsw=3.5ns  s4rlo=42.9    s4rhi=116 ; 31.3ohm, 1.35v
+       s5name="Z"   s5tsw=3.5ns  s5rlo=200K    s5rhi=200K
+       )
.model DIN74_OC dinput (
+       s0name="0"   s0tsw=3.5ns  s0rlo=7.13    s0rhi=389 ; 7ohm,   0.09v
+       s1name="1"   s1tsw=5.5ns  s1rlo=200K    s1rhi=200K
+       s2name="X"   s2tsw=3.5ns  s2rlo=42.9    s2rhi=116 ; 31.3ohm, 1.35v
+       s3name="R"   s3tsw=3.5ns  s3rlo=42.9    s3rhi=116 ; 31.3ohm, 1.35v
+       s4name="F"   s4tsw=3.5ns  s4rlo=42.9    s4rhi=116 ; 31.3ohm, 1.35v
+       s5name="Z"   s5tsw=5.5ns  s5rlo=200K    s5rhi=200K
+       )
```

```
.model DO74 doutput (
+       s0name="X"   s0vlo=0.8      s0vhi=2.0
+       s1name="0"   s1vlo=-1.5     s1vhi=0.8
+       s2name="R"   s2vlo=0.8      s2vhi=1.4
+       s3name="R"   s3vlo=1.3      s3vhi=2.0
+       s4name="X"   s4vlo=0.8      s4vhi=2.0
+       s5name="1"   s5vlo=2.0      s5vhi=7.0
+       s6name="F"   s6vlo=1.3      s6vhi=2.0
+       s7name="F"   s7vlo=0.8      s7vhi=1.4
+       )
.model DO74_NX doutput (
+       s0name="0"   s0vlo=-1.5     s0vhi=1.35
+       s2name="1"   s2vlo=1.35     s2vhi=7.0
+       )
.model DO74_ST doutput (
+       s0name="0"   s0vlo=-1.5     s0vhi=1.7
+       s1name="1"   s1vlo=0.9      s1vhi=7.0
+       )

.model D74 d (
+       is=1e-16        rs=25   cjo=2pf
+       )
.model D74CLMP d (
+       is=1e-15        rs=2    cjo=2pf
+       )
.model Q74 npn (
+       ise=1e-16       isc=4e-16
+       bf=49  br=.03
+       cje=1pf         cjc=.5pf
+       cjs=3pf         vje=0.9v
+       vjc=0.8v        vjs=0.7v
+       mje=0.5         mjc=0.33
+       mjs=0.33        tf=0.2ns
+       tr=10ns         rb=50
+       rc=20
+       )
*$
*---------------------------------------------------------------------------
* Library of optocoupler models

* Copyright 1992 by MicroSim Corporation
* This is a reduced version of MicroSim's Opto-coupler components library.
*   You are welcome to make as many copies of it as you find convenient.

* The parameters in this model library were derived from the data sheets for
* each part.
*$
*.model 4N25
* 6-pin DIP: pin #1   #2   #4   #5   #6
*            |    |    |    |    |
.subckt A4N25           pin1 pin2 pin4 pin5 pin6        params: rel_CTR=1
*               Motorola        pid=4N25
*               88-01-04 pwt
*               88-01-18 pwt  rework Cje approximation
```

```
* The data sheet used for this model is from Motorola: it was the most
* complete for DC and switching parameters, and is was easy to find the
* component IR-LED and phototransistor as separate devices for further
* specifications.

 d_MainLED  pin1 pin2      MainLED
 d_PhotoLED        pin1 1        PhotoLED .001
 v_PhotoLED        1 pin2        0

 f_TempComp        0 2           v_PhotoLED 1
 r_TempComp        2 0           TempComp {rel_CTR}

 g_BaseSrc   5 6 2 0             .9
 q_PhotoBJT  5 6 4         PhotoBJT
 r_C         5 pin5        .1
 r_B         6 pin6        .1
 r_E         4 pin4        .1

* Since active devices dominate pin-to-pin capacitance on each "side" of the
* optocoupler, isolation is modeled by identical capacitances and resistances
* linked to a common point; this gives isolation of .5pF and 1E+11 ohms
 c_1         pin1 7        .4p
 r_1         pin1 7        .12T
 c_2         pin2 7        .4p
 r_2         pin2 7        .12T
 c_4         pin4 7        .4p
 r_4         pin4 7        .12T
 c_5         pin5 7        .4p
 r_5         pin5 7        .12T
 c_6         pin6 7        .4p
 r_6         pin6 7        .12T

* Similar to Motorola MLED15.
.model MainLED  D(Is=1.1p Rs=.66 Ikf=30m N=1.9 Xti=3 Cjo=40p M=.34 Vj=.75
+               Isr=30n Nr=3.8 Bv=6 Ibv=100u Tt=.5u)

* Models photon generation: same as MainLED except no AC effects, no breakdown.
.model PhotoLED D(Is=1.1p Rs=.66 Ikf=30m N=1.9 Xti=3 Cjo=0   M=.34 Vj=.75
+               Isr=30n Nr=3.8 Bv=0 Tt=0)

* Temperature compensation for system: 1.38x @ -55'C, .54x @ +100'C, all @ 10mA
* Note: the photo BJT has its own temperature corrections, which must be kept
* as the transistor is electrically available.
.model TempComp     RES(R=1 Tc1=-11.27m Tc2=43.46u)

* Similar to Motorola MDR3050; Hfe=325 @ Ic=500uA, Vce=5V
* Use beta variation (w/Parts) to model change in current-transfer ratio (CTR).
* Hand adjust reverse beta (Br) to match saturation characteristics.
* Set Isc to model dark current.
* Hand adjust Cjc to match fall time @ Ic=10mA (which yields rise time, too).
* Hand adjust reverse transit-time (Tr) to match storage time @ Ic=10mA.
* Delay time set by LED I-V and C-V characteristics; set Cje to 25% of Cjc,
* inspection of phototransistor chip layouts show the emitter area is 20%-25%
```

```
* that of the collector area. The same layouts show that base resistance is
* made negligible by design; also, the operating currents are small.
* Hand adjust forward transit-time (Tf) to match MDR3050 pulse data. Check
* against 4N25 frequency response (Fig 11, 12).
.model PhotoBJT NPN(Is=10f Xti=3 Vaf=60
+                  Bf=400 Ne=3.75 Ise=580p Ikf=.26 Xtb=1.5
+                  Br=.04 Nc=2    Isc=3.5n
+                  Cjc=10p  Mjc=.3333 Vjc=.75 Tr=88u
+                  Cje=2.5p Mje=.3333 Vje=.75 Tf=1.5n)
.ends
*$
*.model 4N25A
* 6-pin DIP: pin #1   #2   #4   #5   #6
*            |   |   |   |   |
.subckt A4N25A        pin1 pin2 pin4 pin5 pin6
*                  88-01-05 pwt
* Same as 4N25 (UL recognized).
 x1 pin1 pin2 pin4 pin5 pin6 A4N25
.ends
*$
*-------------------------------------------------------------------------------
* Library of Thyristor (SCR and Triac) models

* Copyright 1992 by MicroSim Corporation
* This is a reduced version of MicroSim's Thyristor components library.
*   You are welcome to make as many copies of it as you find convenient.

* Library of SCR models

* NOTE:  This library requires the "Analog Behavioral Modeling"
*        option available with PSpice.  A model developed without
*        Behavioral Modeling was found to be very slow and not
*        very robust.

* This macromodel uses a controlled switch as the basic SCR
* structure.  In all cases, the designer should use
* the manufacturer's data book for actual part selection.

* The required parameters were derived from data sheet (Motorola)
* information on each part.  When available, only "typical"
* parameters are used (except for Idrm which is always
* a "max" value).  If a "typical" parameter is not available,
* a "min" or "max" value may be used in which case a comment is
* made in the library.

* The SCRs are modeled at room temperature and do not track
* changes with temperature.  Note that Vdrm is specified by the
* manufacturer as valid over a temperature range.  Also, in
* nearly all cases, dVdt and Toff are specified by the
* manufacturer at approximately 100 degrees C.  This results in a
* model which is somewhat "conservative" for a room temperature
* model.

* The parameter dVdt (when available from the date sheet) is used
```

```
* to model the Critical Rate of Rise of Off-State Voltage. If
* not specified, dVdt is defaulted to 1000 V/microsecond.
* A side effect of this model is that the turn-on current, Ion,
* is determined by Vtm/(Ih*Vdrm). Vtm is also used as the
* holding voltage.
*$
.SUBCKT Scr anode gate cathode PARAMS:
+ Vdrm=400v    Vrrm=400v    Idrm=10u
+ Ih=6ma       dVdt=5e7
+ Igt=5ma      Vgt=0.7v
+ Vtm=1.7v     Itm=24
+ Ton=1u       Toff=15u

* Where:
* Vdrm => Forward breakover voltage
* Vrrm => Reverse breakdown voltage
* Idrm => Peak blocking current
* Ih   => Holding current
* dVdt => Critical value for dV/dt triggering
* Igt  => Gate trigger current
* Vgt  => Gate trigger voltage
* Vtm  => On-state voltage
* Itm  => On-state current
* Ton  => Turn-on time
* Toff => Turn-off time

* Main conduction path
Scr     anode   anode0  control 0      Vswitch ; controlled switch
Dak1    anode0  anode2  Dakfwd  OFF           ; SCR is initially off
Dka     cathode anode0  Dkarev  OFF
VIak    anode2  cathode                  ; current sensor

* dVdt Turn-on
Emon    dvdt0   0       TABLE {v(anode,cathode)} (0 0) (2000 2000)
CdVdt   dvdt0   dvdt1   100pfd                ; displacement current
Rdlay   dvdt1   dvdt2   1k
VdVdt   dvdt2   cathode DC 0.0
EdVdt   condvdt 0       TABLE {i(vdVdt)-100p*dVdt}  (0 0 ) (.1m 10)
RdVdt   condvdt 0       1meg

* Gate
Rseries gate    gate1   {(Vgt-0.65)/Igt}
Rshunt  gate1   gate2   {0.65/Igt}
Dgkf    gate1   gate2   Dgk
VIgf    gate2   cathode                  ; current sensor

* Gate Turn-on
Egate1  gate4   0       TABLE {i(Vigf)-0.95*Igt} (0 0) (1m 10)
Rgate1  gate4   0       1meg
Egon1   congate 0       TABLE {v(gate4)*v(anode,cathode)} (0 0) (10 10)
Rgon1   congate 0       1meg

* Main Turn-on
EItot   Itot    0       TABLE {i(VIak)+5E-5*i(VIgf)/Igt} (0 0) (2000 2000)
```

```
RItot   Itot   0      1meg
Eprod   prod   0      TABLE {v(anode,cathode)*v(Itot)} (0 0) (1 1)
Rprod   prod   0      1meg
Elin    conmain 0      TABLE
+       {10*(v(prod) - (Vtm*Ih))/(Vtm*Ih)} (0 0) (2 10)
Rlin    conmain 0      1meg

* Turn-on/Turn-off control
Eonoff  contot 0      TABLE
+       {v(congate)+v(conmain)+v(condvdt)} (0 0) (10 10)

* Turn-on/Turn-off delays
Rton    contot  dlay1   825
Dton    dlay1   control Delay
Rtoff   contot  dlay2   {290*Toff/Ton}
Dtoff   control dlay2   Delay
Cton    control 0       {Ton/454}

* Reverse breakdown
Dbreak  anode   break1  Dbreak
Dbreak2 cathode break1  Dseries

* Controlled switch model
.MODEL Vswitch vswitch
+ (Ron = {(Vtm-0.7)/Itm}, Roff = {Vdrm*Vdrm/(Vtm*Ih)},
+  Von = 5.0,            Voff = 1.5)

* Diodes
.MODEL  Dgk     D       (Is=1E-16 Cjo=50pf Rs=5)
.MODEL  Dseries D       (Is=1E-14)
.MODEL  Delay   D       (Is=1E-12 Cjo=5pf  Rs=0.01)
.MODEL  Dkarev  D       (Is=1E-10 Cjo=5pf  Rs=0.01)
.MODEL  Dakfwd  D       (Is=4E-11 Cjo=5pf)
.MODEL  Dbreak  D       (Ibv=1E-7 Bv={1.1*Vrrm} Cjo=5pf Rs=0.5)

* Allow the gate to float if required
Rfloat  gate    cathode 1e10

.ENDS
*$
.SUBCKT 2N1595          anode gate cathode
* "Typical" parameters
X1 anode gate cathode Scr PARAMS:
+ Vdrm=50v   Vrrm=50v    Ih=5ma      Vtm=1.1v    Itm=1
+ dVdt=1e9   Igt=2ma     Vgt=.7v     Ton=0.8u    Toff=10u
+ Idrm=10u
* 90-5-18    Morotola    DL137, Rev 2, 3/89
.ENDS
*$
* Library of Triac models

* NOTE:  This library requires the "Analog Behavioral Modeling"
*        option available with PSpice.
```

```
* This macromodel uses two controlled switches as the basic triac
* structure. The model was developed to provide firing in all
* four quadrants. It should be noted, however, that the library
* contains parts which the manufacturer has guaranteed will fire
* in 4 quadrants, 3 quadrants or 2 quadrants. Therefore, the
* designer should always use the manufacturer's data book for
* part selection.

* The required parameters were derived from data sheet (Motorola)
* information on each part. When available, only "typical"
* parameters are used (except for Idrm which is always
* a "max" value). If a "typical" parameter is not available,
* a "min" or "max" value may be used in which case a comment is
* made in the library.

* The triacs are modeled at room temperature and do not track
* changes with temperature. Note that Vdrm is specified by the
* manufacturer as valid over a temperature range. Also, in
* nearly all cases, dVdt is specified by the manufacturer at
* approximately 100 degrees C. This results in a model which
* is somewhat "conservative" for a room temperature model.

* The parameter dVdt (when available from the date sheet) is used
* to model the Critical Rate of Rise of Off-State Voltage. If
* not specified, dVdt is defaulted to 1000 V/microsecond. The
* Critical Rate of Rise of Commutation Voltage is not modeled.
* It is generally good practice to use an RC snubber network
* across the triac to limit the commutating dvdt to a value below
* the maximum allowable rating (see manufacturer's data sheet and
* application notes). Also, note that the turn-off time is
* assumed to be zero.
*$
.SUBCKT Triac MT2 gate MT1 PARAMS:
+ Vdrm=400v    Idrm=10u
+ Ih=6ma       dVdt=50e6
+ Igt=20ma     Vgt=0.9v
+ Vtm=1.3v     Itm=17
+ Ton=1.5u

* Where:
* Vdrm => Forward breakover voltage
* Idrm => Peak blocking current
* Ih   => Holding current [MT2(+)]
* dVdt => Critical value for dV/dt triggering
* Igt  => Gate trigger current [MT2(+),G(-)]
* Vgt  => Gate trigger voltage [MT2(+),G(-)]
* Vtm  => On-state voltage
* Itm  => On-state current
* Ton  => Turn-on time

* Main conduction path
Striac  MT2    MT20   cntrol  0      Vswitch ; controlled switch
Dak1    MT20   MT22   Dak     OFF             ; triac is initially off
VIak    MT22   MT1                            ; current sensor
```

```
Striacr MT2    MT23   cntrolr 0      Vswitch ; controlled switch
Dka1   MT21    MT23   Dak     OFF           ; triac is initially off
VIka   MT1     MT21                         ; reverse current sense

* dVdt Turn-on
Emon   dvdt0  0      TABLE {ABS(V(MT2,MT1))} (0 0) (2000 2000)
CdVdt  dvdt0  dvdt1  100pfd                 ; displacement current
Rdlay  dvdt1  dvdt2  1k
VdVdt  dvdt2  MT1    DC 0.0
EdVdt  condvdt 0     TABLE {i(vdVdt)-100p*dVdt}  (0 0 ) (.1m 10)
RdVdt  condvdt 0     1meg

* Gate
Rseries  gate   gate1  {(Vgt-0.65)/Igt}
Rshunt   gate1  gate2  {0.65/Igt}
Dgkf   gate1  gate2  Dgk
Dgkr   gate2  gate1  Dgk
VIgf   gate2  MT1    DC 0.0               ; current sensor

* Gate Turn-on
Egate  congate 0     TABLE {(ABS(i(VIgf))-0.95*Igt)} (0 0) (1m 10)
Rgate  congate 0     1meg

* Holding current, holding voltage (Quadrant I)
Emain1  main1  0     TABLE {i(VIak)-Ih+5e-3*i(VIgf)/Igt} (0 0) (.1m 1)
Rmain1  main1  0     1meg
Emain2  main2  0     TABLE {v(MT2,MT1)-(Ih*Vtm/Itm)} (0 0) (.1m 1)
Rmain2  main2  0     1meg
Emain3  cnhold 0     TABLE {v(main1,0)*v(main2,0)} (0 0 (1 10)
Rmain3  cnhold 0     1meg

* Holding current, holding voltage (Quadrant III)
Emain1r main1r  0    TABLE {i(VIka)-Ih-5e-3*i(VIgf)/Igt} (0 0) (.1m 1)
Rmain1r main1r  0    1meg
Emain2r main2r  0    TABLE {v(MT1,MT2)-(Ih*Vtm/Itm)} (0 0) (.1m 1)
Rmain2r main2r  0    1meg
Emain3r cnholdr 0    TABLE {v(main1r,0)*v(main2r,0)} (0 0 (1 10)
Rmain3r cnholdr 0    1meg

* Main
Emain4  main4   0    table {(1.0-ABS(i(VIgf))/Igt)} (0 0) (1 1)
Rmain4  main4   0    1meg
Emain5  cnmain  0    table {v(mt2,mt1)-1.05*Vdrm*v(main4)} (0 0) (1 10)
Rmain5  cnmain  0    1meg

Emain5r cnmainr 0    table {v(mt1,mt2)-1.05*Vdrm*v(main4)} (0 0) (1 10)
Rmain5r cnmainr 0    1meg

* Turn-on/Turn-off control (Quadrant I )
Eonoff  contot 0     TABLE
+      {v(cnmain)+v(congate)+v(cnhold)+v(condvdt)} (0 0) (10 10)

* Turn-on/Turn-off delays (Quadrant I)
Rton    contot dlay1  825
```

```
Dton    dlay1  cntrol  Delay
Rtoff   contot  dlay2  {2.9E-3/Ton}
Dtoff   cntrol  dlay2  Delay
Cton    cntrol  0      {Ton/454}

* Turn-on/Turn-off control (Quadrant III)
Eonoffr  contotr 0      TABLE
+       {v(cnmainr)+v(congate)+v(cnholdr)+v(condvdt)} (0 0) (10 10)

* Turn-on/Turn-off delays (Quadrant III)
Rtonr   contotr dlayr1   825
Dtonr   dlayr1  cntrolr  Delay
Rtoffr  contotr dlayr2  {2.9E-3/Ton}
Dtoffr  cntrolr dlayr2  Delay
Ctonr   cntrolr 0       {Ton/454}

* Controlled switch model
.MODEL Vswitch vswitch
+ (Ron = {(Vtm-0.7)/Itm}, Roff = {1.75E-3*Vdrm/Idrm},
+  Von = 5.0,            Voff = 1.5)

* Diodes
.MODEL  Dgk    D       (Is=1E-16 Cjo=50pf Rs=5)
.MODEL  Delay  D       (Is=1E-12 Cjo=5pf  Rs=0.01)
.MODEL  Dak    D       (Is=4E-11 Cjo=5pf)

* Allow the gate to float if required
Rfloat  gate   MT1 1e10

.ENDS

*$
.SUBCKT 2N5444        MT2 gate MT1
* Min and Max parameters
X1 MT2 gate MT1 Triac PARAMS:
+ Vdrm=200v  Idrm=10u    Ih=70ma     dVdt=50e6   Ton=1u
+ Igt=70ma   Vgt=2.0v    Vtm=1.65v   Itm=56
* 90-5-18   Morotola    DL137, Rev 2, 3/89
.ENDS

*$
* Mixed a/d model for Cmos version of 555.
*
.subckt 555d 1 2 3 4 5 6 7 8
+ params:maxfreq=3e6
 r1 8    5   13k
 r2 5    botm 13k
 r3 botm  0   13k
 m1 7 qb 0 0 nchan l=2u w=1000u
 otop 6    5  cmp dgtlnet=r io_std
 obot botm  2  cmp dgtlnet=s io_std
 ud1 dlyline 8 1 s sd dlymod io_std
 ud2 dlyline 8 1 r rd dlymod io_std
 u1 srff(1) 8 1 strt 4 hi sd rd 3 qb t_srff io_555
```

```
 uhigh stim(1,1) 8 1  hi io_stm 0s 1
 ustrt stim(1,1) 8 1  strt io_stm 0s 0 1ns 1
.model nchan nmos cgbo=1p cgdo=1p cgso=1p
.model dlymod udly(dlymn={.5/maxfreq}
+ dlyty={.5/maxfreq}
+ dlymx={0.5/maxfreq})
.model cmp doutput(
+ s0name=0 s0vlo=-500 s0vhi=0
+ s1name=1 s1vlo=  0 s1vhi=500)
.model io_555 uio (
+       drvh=96.4     drvl=104
+       atod1="atod_555"     atod2="atod_555"
+       atod3="atod_555"     atod4="atod_555"
+       dtoa1="dtoa_555"     dtoa2="dtoa_555"
+       dtoa3="dtoa_555"     dtoa4="dtoa_555")
.model t_srff ugff (tppcqlhty=120ns)
.ends
.subckt atod_555  a d  dpwr dgnd
+       params: capacitance=0
*
 o0  a dgnd do555 dgtlnet=d io_std
 c1  a 0 {capacitance+0.1pf}
.ends
.subckt dtoa_555  d a  dpwr dgnd
+       params: drvl=0 drvh=0 capacitance=0
*
 n1  a dgnd dpwr din555 dgtlnet=d io_std
 c1  a 0 {capacitance+.1pf}
.ends
.model din555 dinput (
+       s0name="0"   s0tsw=0.7ns  s0rlo=100     s0rhi=1meg
+       s1name="1"   s1tsw=0.7ns  s1rlo=1meg    s1rhi=300
+       s2name="x"   s2tsw=0.7ns  s2rlo=200     s2rhi=200
+       s3name="r"   s3tsw=0.7ns  s3rlo=200     s3rhi=200
+       s4name="f"   s4tsw=0.7ns  s4rlo=200     s4rhi=200
+       s5name="z"   s5tsw=0.7ns  s5rlo=200k    s5rhi=200k
+       )
.model DO555 doutput (
+       s0name="X"   s0vlo=0.8    s0vhi=2.0
+       s1name="0"   s1vlo=-1.5   s1vhi=0.8
+       s2name="R"   s2vlo=0.8    s2vhi=1.4
+       s3name="R"   s3vlo=1.3    s3vhi=2.0
+       s4name="X"   s4vlo=0.8    s4vhi=2.0
+       s5name="1"   s5vlo=2.0    s5vhi=50.0
+       s6name="F"   s6vlo=1.3    s6vhi=2.0
+       s7name="F"   s7vlo=0.8    s7vhi=1.4
+       )


*|* DIGITAL 555 CONNECTED AS AN ASTABLE
*|.LIB EVAL.LIB
*|.OPTIONS ITL5=0 ITL1=500
*|.PARAM CVAL=20000P
*|VRESET 4 0 PULSE(0 5 1NS .1U .1U 1 2)
```

```
*|C2 OUT 0 10P
*|VCC 8 0 5
*|RA 8 7 4700
*|RB 7 6 2200
*|C1 6 0 {CVAL}
*|X1 0 6 OUT 4 5 6 7 8 555D
*|.TRAN 1N 800U
*|.PROBE
*|.END
*$
* End of library file
```