in our transmission circuit design. Specifically, a communication distance of 1 meter corresponds to a coupling factor of about 10^{-6}, although there is some doubt about this measurement and a goal of this thesis is to measure coupling factor for distances up to 1 meter.

1.4.2 Applicable Semiconductor Technologies

Among many aspects to implement high-temperature electronics, the high-temperature semiconductor technology is the most challenging, although IC packaging, wiring and solder must also be considered. The applicable semiconductor materials are silicon (Si), gallium arsenide (GaAs) and other III-V compound semiconductors, silicon carbide (SiC), diamonds, etc [6].

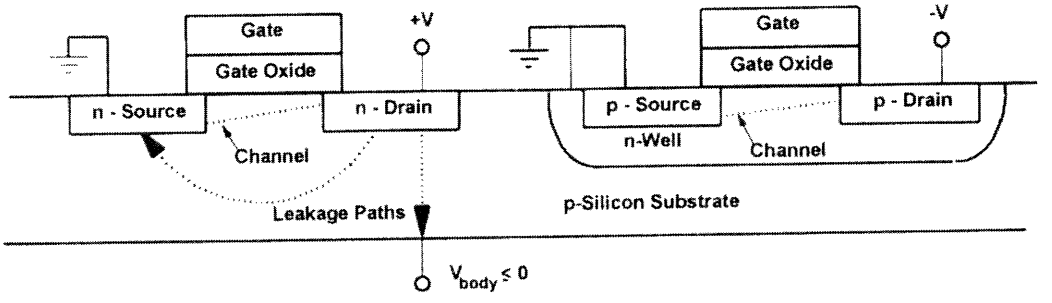

Figure 1-2 Simplified sketch on n-channel and p-channel MOSFETs on a p-type silicon wafer (from [4])

Currently, Si complementary metal oxide semiconductor (CMOS) is the most widely used technology (Figure 1-2). When temperature is increased, channel mobility and threshold voltage decrease, and the two leakage current paths, shown by the dashed arrows in Figure 1-2, significantly degrade the characteristics of a MOSFETs [4]. Well designed bulk Si CMOS circuits can operate at temperature approaching 200°C, but the desired high-temperature applications require operation above 200°C, as high as 300°C.

Instead of isolation using the reversed-biased junctions, Silicon-On-Insulator (SOI) technology isolates the devices using dielectric materials. The leakage current can

be reduced by two to four orders of magnitude, and integrated circuits on SOI can be operated at temperatures up to 300°C.

The Ultra Thin Silicon (UTSi) process, a mature SOI process invented by Peregrine Semiconductor, was chosen for our SOI circuits. The insulating layer in the technology is sapphire, and the technology is also called SOS. This technique allows Peregrine to use common silicon fabrication equipment and processing techniques to integrate CMOS transistors and nearly ideal passive components on the same wafer.

As stated above, wells in a regular CMOS process isolate each MOSFET from the substrate. At high temperature, a large reverse-biased current will flow through the parasitic PNP and NPN structure to cause circuit malfunction. On the other hand, SOI technology provides devices on insulator. Inherently, there are no parasitic bulk diodes or BJTs. Therefore, the IC can be operated at higher temperature. The comparison between a bulk Si process and a SOS process is illustrated in Figure 1-3.

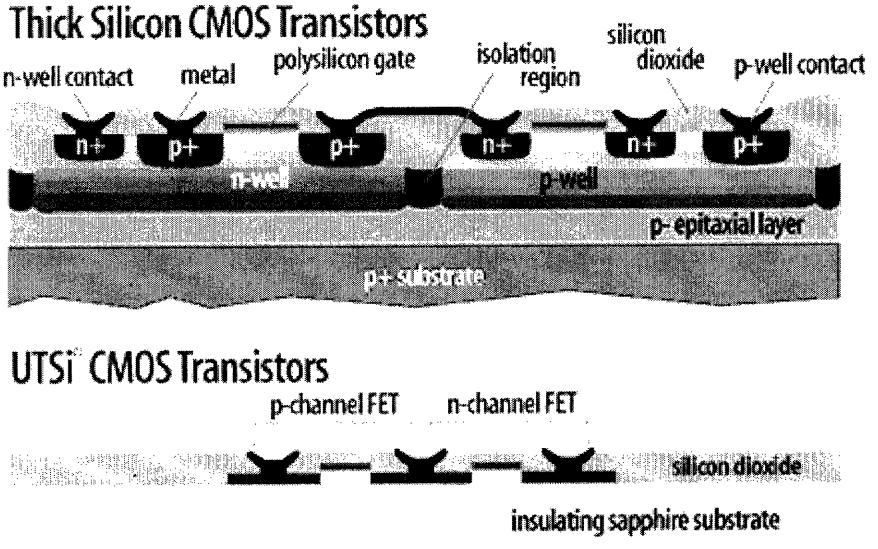

Figure 1-3 The comparison between bulk CMOS technology and Peregrine SOI technology (from [17]).