WIRELESS INTERFACE CIRCUIT FOR HIGH-TEMPERATURE APPLICATIONS USING SOI MOS VARACTOR

by

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Submitted in partial fulfillment of the requirements

For the degree of Master of Science

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To my family

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Wireless Interface Circuits for High-Temperature Sensor Applications Using SOI MOS Varactor

Abstract

by

YUNLI HE

A wireless interface circuit has been designed for low-power operation, compact size, and reliable performance in a harsh environment, i.e. at high-temperature. The work includes both transmitter and receiver pre-amplifier, which are designed to operate at an ISM frequency, 27 MHz, which is suitable for short-range communication requiring relatively low bandwidth. The modulation scheme is BFSK, and the bandwidth of the communication link is designed for a maximum bit rate of 125 kbps.

The transmitter uses a 2-turn 2-cm square planar loop antenna, which also serves as the inductance required for oscillation. A Germanium tunnel diode is used to provide negative resistance required for oscillation. Frequency is modulated using a voltage-controlled capacitor which has been implemented using a PN varactor diode or SOI MOS varactor, the latter which has potential for achieving the ultimate goal 250 ℃ operation.

The receiver employs a low-cost, commercial antenna. A two-stage receiver pre-amplifier was designed based on a discrete BJT to optimize SNR and amplify the received signal to the mV range for display or demodulation. Simulations show that SNR is greater than 10 dB when antenna coupling factor is 10^{-6}, corresponding to a maximum distance of about 1 meter.

Room-temperature test results are presented for all circuits, and suggestions for future work towards the ultimate goal of high-temperature wireless sensing are presented.

1 Introduction

1.1 Background

In the past two decades, CMOS technology has embraced the field of analog integrated circuits, providing low-cost, high-performance solutions and rising to dominate the market for analog ICs. Analog circuit design has evolved with the technology. High-voltage, high-power analog circuits containing a few tens of transistors and processing small, continuous-time signals have gradually been replaced by low-voltage, low-power systems comprising thousands of devices and processing large, mostly discrete-time signals [1]. At the same time, MEMS technology has emerged and recently there has been a noticeable trend towards integrated microsystems that merge microsensors, microactuators and microelectronics on a common substrate [2].

Most microsystems are developed for commercial and industrial applications operating at 70°C and 85°C maximum, respectively, and for military applications at 125°C. There is growing demand for high-temperature microsystems (≥200°C) for applications in sensor instrumentation, down-hole petroleum and geothermal production, distributed turbine engine controls, and distributed heavy duty engine controls [29].

Conventional microelectronics, based upon bulk CMOS technology, suffer from severe performance degradation and failure due to excessive junction leakage currents for temperatures above 150°C. Silicon-On-Insulator (SOI) and Silicon-Carbide (SiC) technologies are promising for increased operating temperatures up to 300°C and 600°C, respectively [3]. While researchers continue to develop SiC technology, SOI technology is presently available.

In the Glennan Microsystem Initiative (GMI), researchers at CWRU and NASA Glenn Research Center (GRC) explore the feasibility of high-temperature sensing using capacitive or resistive sensors, converting data from analog to digital format, decimating, and transmitting the processed digital data by wireless transmission from the high-temperature environment (up to 500°C) to an ambient temperature environment (Figure 1-1). Circuits were first designed for SiC technology, but the current work is focused on SOI technology, which can operate at temperatures up to 300°C. This thesis provides a brief overview of the entire project, but is focused on the implementation of the wireless communication.

1.2 Motivation

The project has been motivated by the need for high-temperature electronics that are critical to implementing harsh-environment systems. The primary demands come from the current and future applications in automotive electronic systems, aircraft and space devices, military applications, well logging industries and geothermal measurements [4] [5].

1.2.1 Automotive Electronic Systems

Application temperature ranges from 137°C to 700°C in the automotive industry [4], where the exhaust gas sensor requires the most extreme temperature. Because of the difficulty in keeping effective air flow throughout the engine compartment over the wide operating speed and load ranges, the typical temperature in the engine compartment ranges from 137°C to 300°C [4] [5]. To be located on the engine, the electronics are required to work in a high-temperature environment. The automobile manufactures are

investing more money to develop high-temperature electronics for reliable operation [4] [5].

1.2.2 Aircraft Industry and Space Programs

In the aircraft industry, it is desirable that electronic sensors and controlling devices be located on or near the jet engine. The typical temperature is 300°C and the leading edge temperature can be up to 650°C. Without high-temperature electronics, complex cooling systems and wiring are required. In military applications, electronics are actively cooled or remotely located to reduce temperature. In commercial applications, these electronics are cooled by air. The availability of high-temperature electronics simplifies the system, and has dramatic effects on power generation and distribution onboard aircraft [4] [5] [6].

In addition, the reactor space power program, nuclear power plants and scientific space missions will benefit from the availability of high-temperature electronics [5].

1.2.3 Geothermal and Well Logging

Well logging is another important application for high-temperature electronics. The temperature for enhanced oil recovery, which is done by steam injection, ranges from 200°C to 300°C [5] [6] while geothermal well logging system requires electronics operating even higher, up to 500°C [6].

1.3 Objective

The **overall** GMI project being conducted by S. Garverick *et al* includes the following components:

1. A high-temperature SOI oscillator circuit, which provides the clock for the data conversion circuits.
2. A high-temperature SOI sigma-delta analog-to-digital converter, which oversamples the sensor data and converts to digital format at1 Mbps.
3. A high-temperature SOI decimation filter, which filters and down-samples the sigma-delta output to a lower data rate and converts parallel data to serial data for convenience in transmission.
4. A high-temperature wireless interface circuit using SOI technology and a tunnel diode, which modulates serial digital data by frequency-shift-keying (FSK) and transmits the data using a planar loop antenna.
5. A room-temperature receiver, which detects the very weak signal, pre-amplifies, demodulates the FSK format and retrieves the sensor data in digital format.

In this thesis, the wireless communication link is studied, including the antenna system, FSK oscillator and modulator, and receiver pre-amplifier. The simplified system architecture for the proposed wireless sensor is shown in Figure 1-1. The transmitter is designed using SOI IC technology, a tunnel diode, and planar loop antenna. A pre-amplifier for the receiver has been designed to detect the transmitted signal for distance up to about 1meter. The selected carrier is the ISM frequency at 27 MHz [8] and FSK is employed to modulate the data. A commercial 27-MHz antenna is used in the receiver design.

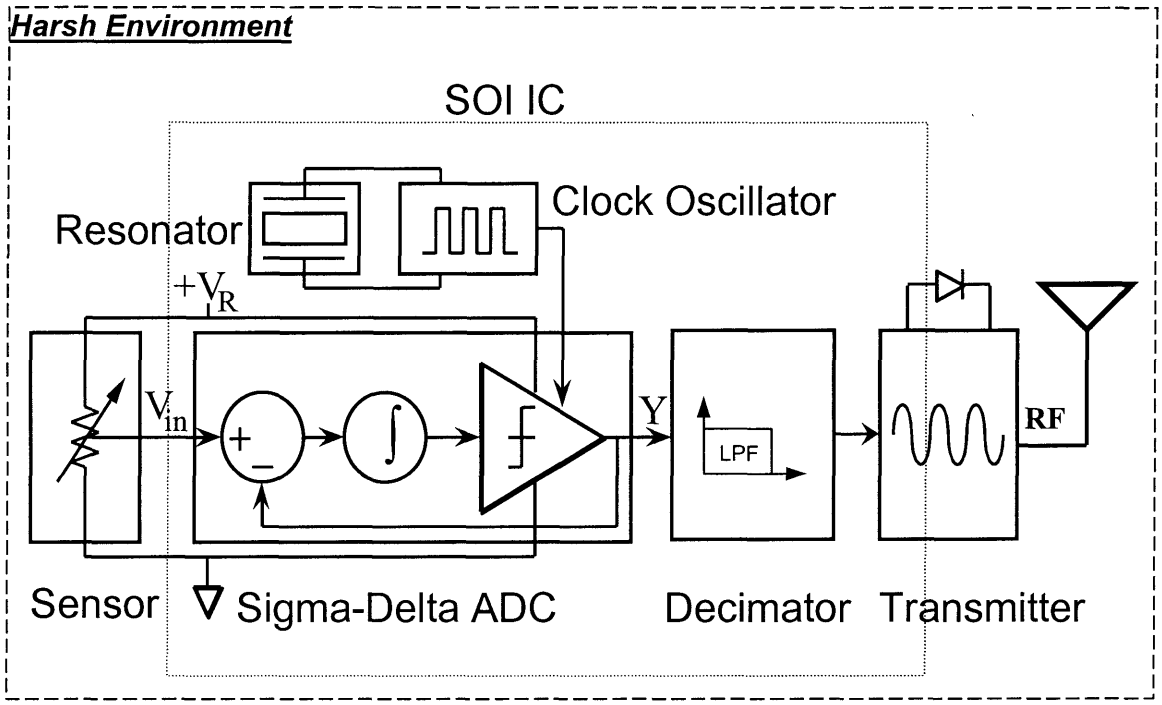


Figure 1-1 Simplified transmitter architecture in harsh environment [7].

1.4 Project History and Approaches

Several students have contributed to the overall group effort to develop a low-power, high-temperature wireless communications circuit.

1.4.1 Project History

In the thesis by Daniel Baker, an RF link using ASK was successful designed and measured. Within 2-inch (5.08-cm) distance, the ratio of transmitting voltage to receiving voltage is degrading to 0.05 [27].

Eric Kimball also explored inductively coupled RF transmission using Amplitude Shift Keying [28]. Theory regarding the power efficiency and the signal fidelity has been developed and verified by new circuitry design.

Premal Shal explored the coupling factor in his project. Though the measured coupling factor is far larger than the theoretical value [11], it provides helpful information

in our transmission circuit design. Specifically, a communication distance of 1 meter corresponds to a coupling factor of about 10^{-6}, although there is some doubt about this measurement and a goal of this thesis is to measure coupling factor for distances up to 1 meter.

1.4.2 Applicable Semiconductor Technologies

Among many aspects to implement high-temperature electronics, the high-temperature semiconductor technology is the most challenging, although IC packaging, wiring and solder must also be considered. The applicable semiconductor materials are silicon (Si), gallium arsenide (GaAs) and other III-V compound semiconductors, silicon carbide (SiC), diamonds, etc [6].

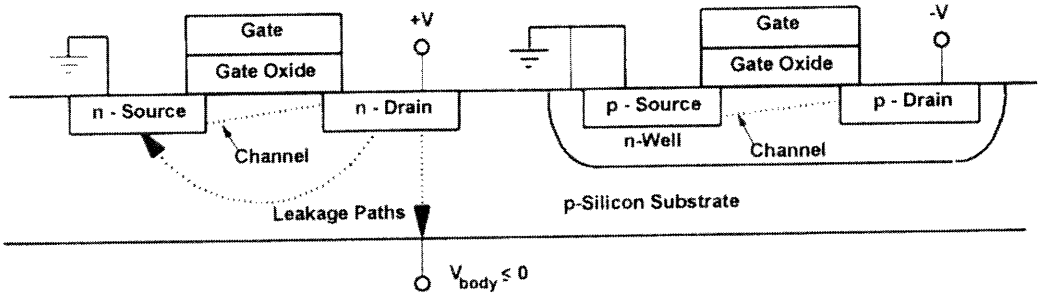


Figure 1-2 Simplified sketch on n-channel and p-channel MOSFETs on a p-type silicon wafer (from [4])

Currently, Si complementary metal oxide semiconductor (CMOS) is the most widely used technology (Figure 1-2). When temperature is increased, channel mobility and threshold voltage decrease, and the two leakage current paths, shown by the dashed arrows in Figure 1-2, significantly degrade the characteristics of a MOSFETs [4]. Well designed bulk Si CMOS circuits can operate at temperature approaching 200°C, but the desired high-temperature applications require operation above 200°C, as high as 300°C.

Instead of isolation using the reversed-biased junctions, Silicon-On-Insulator (SOI) technology isolates the devices using dielectric materials. The leakage current can

be reduced by two to four orders of magnitude, and integrated circuits on SOI can be operated at temperatures up to 300°C.

The Ultra Thin Silicon (UTSi) process, a mature SOI process invented by Peregrine Semiconductor, was chosen for our SOI circuits. The insulating layer in the technology is sapphire, and the technology is also called SOS. This technique allows Peregrine to use common silicon fabrication equipment and processing techniques to integrate CMOS transistors and nearly ideal passive components on the same wafer.

As stated above, wells in a regular CMOS process isolate each MOSFET from the substrate. At high temperature, a large reverse-biased current will flow through the parasitic PNP and NPN structure to cause circuit malfunction. On the other hand, SOI technology provides devices on insulator. Inherently, there are no parasitic bulk diodes or BJTs. Therefore, the IC can be operated at higher temperature. The comparison between a bulk Si process and a SOS process is illustrated in Figure 1-3.

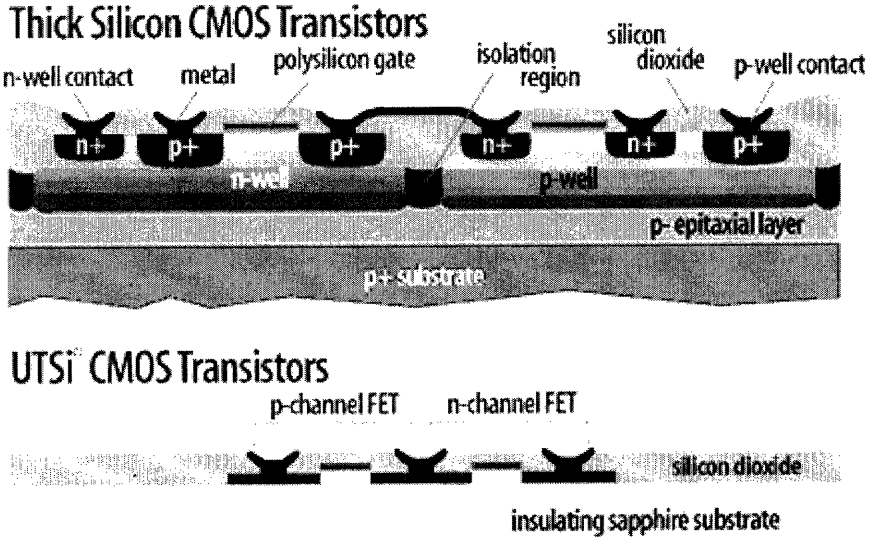


Figure 1-3 The comparison between bulk CMOS technology and Peregrine SOI technology (from [17]).

1.5 Thesis outline

Chapter 2 explains the basic approach to digital telemetry. The selection of carrier frequency and antenna design is discussed. The available digital modulation techniques are explained, as well as the reason for using Binary Frequency Shift Keying (BFSK).

Chapter 3 presents the transmitter design and measurements. The oscillator design based on a tunnel-diode is described. The PN varactor and SOI MOSFET capacitors used to implement FSK are also explained. The n-turn planar loop antenna is described and the inductance is calculated. The condition for start-up and oscillation frequency is presented. Finally, the complete transmitter design, measurement procedures, and test results are presented.

Chapter 4 presents the receiver pre-amplifier design and measurement. Here, the coupling theory is analyzed in detail and the antenna model is developed. Before presenting the final first-stage design, the limitations of the simple common-emitter design are explained. The design of the second-stage and biasing circuit are also discussed.

Chapter 5 presents the integrated measurement of transmitter and pre-amplifier, including procedure and measurement results.

Chapter 6 summarizes the thesis work and suggests future work.

2 Digital Telemetry

The earliest telemetry systems used analog techniques. Digital wireless transmission is now common, offers improved efficiency and facilitates digital signal processing. The cost of these benefits is the need for analog-to-digital conversion in the transmitter.

In this project, the sensed signal must be transmitted from a harsh environment. An important consideration in the design of this harsh-environment transmitter is low-power and tiny space. In such a situation, digital telemetry is a good choice for our application. The most significant parameters of the transmission link are carrier frequency and modulation technique.

2.1 Carrier Frequency

Engineers must deal with a broad range of frequencies of circuit operation. Frequency resource is limited; and the abuse of frequency not only interferes with others and wastes resources, but can be harmful. The Federal Communications Commission (FCC) regulates the use of radio frequencies. Commercial frequency channels must be purchased. There are channels that are free for amateurs and other purposes.

Among others, the FCC regulates "industrial, scientific, and medical equipment (ISM) that emits electromagnetic energy on frequencies within the radio frequency spectrum in order to prevent harmful interference to authorized radio communication services" [13]. ISM equipment operating on a frequency specified in Table 2-1 is permitted unlimited radiated energy in the band specified for that frequency [13]. In this research project, we have adhered to the ISM frequencies bands, even though our transmission power is too low to be of concern to others. The ISM bands are located

mainly at low frequencies (less than 50 MHz) or very high frequencies (above 1 GHz) as shown in Table 2-1. In many oscillators, power consumption increases with frequency. A higher frequency requires a device with higher-transconductance, and a higher-transconductance device means higher DC current that consumes more power. In our low-power, short-range telemetry system (about 1-m distance), we have chosen to operate at the lowest ISM frequency that is consistent with our data rate (125 kbps), 27.12 MHz.

Table 2-1 Frequency Bands Allocated for Use by ISM Equipment

ISM frequency	Tolerance
6.78 MHz.....	±15.0 kHz
13.56 MHz.....	±7.0 kHz
27.12 MHz.....	±163.0 kHz
40.68 MHz.....	±20.0 kHz
915 MHz.....	±13.0 MHz
2,450 MHz.....	±50.0 MHz
5,800 MHz.....	±75.0 MHz
24,125 MHz.....	±125.0 MHz
61.25 GHz.....	±250.0 MHz
122.50 GHz.....	±500.0 MHz
245.00 GHz.....	±1.0 GHz

2.2 Antenna Design

This relatively low frequency and short distance means that our system is operating in the near field. The antennae can be capacitively coupled or inductively coupled. Capacitive coupling requires high voltage, but the current can be low. Inductive coupling requires high current, but the voltage can be low. Neither has a clear power advantage, but coupled inductors can be operated directly from a 1.5-V battery.

The best candidate for the transmitter antenna in this project is the simple, easy-implemented, and versatile loop antenna. It is useful that the loop antenna is an inductor, and can be used as the basis of the oscillator. The antenna can be easily implemented on a PCB whose material can be selected for high-temperature applications. Since the transmission distance is moderate, about 1 meter, the antenna interaction is dominated by the inductive coupling. The detailed antenna design is presented in Chapter 3.

The small loop antenna is equivalent to an infinitesimal magnetic dipole whose axis is perpendicular to the plane of the loop. That is, the fields radiated by an electrically small loop antenna are of the same mathematical form as those radiated by an infinitesimal magnetic dipole. The antenna size for this project should be small, no more than 2 centimeters in diameter. Such an antenna is much smaller than the wavelength (λ=c/v) at 27 MHz (11 meter).

Though loop antennas are widely used in HF (3 –30 MHz), VHF (30 – 300 MHz), and UHF (300 – 3000 MHz) bands, electrically small loop antennas are poor radiators because their radiation resistances are generally smaller than their loss resistances.

2.3 Modulation Technique

In wireless systems, the transmitted signal is a high-frequency carrier modulated by the message signal, which is a 125-kbps bit stream in this project. Digital modulation can be performed using Amplitude Shift Keying (ASK), Phase Shift Keying (PSK), or Frequency Shift Keying (FSK). In RF applications, PSK and FSK are much more widely used than ASK because of their lower sensitivity to amplitude noise. The comparison between PSK and FSK is much more involved [14].

Two types of digital modulation are widely used: binary modulation and M-ary modulation. The latter technique employs multiple levels to modulate multiple bits of data, known as a "symbol". In this project, binary modulation was selected because multilevel modulation requires higher amplitude resolution in the demodulator [14].

The quality of transmission involves three parameters: signal quality, spectral efficiency, and power efficiency.

Signal quality is expressed in terms of bit error rate (BER), which is the probability of error in the presence of noise and other interferers [14]. As shown in Table 2-2, bit error rate is a function of energy per bit E_b, noise N_0, and the Q(x) function. The analysis assumes that the received signal is corrupted by additive white noise. The equations for E_b and Q(x) are

$$E_b = A_C^2 T_b / 2 \text{ and} \tag{2-1}$$

$$\begin{aligned} Q(x) &= \frac{1}{\sqrt{2\pi}} \int_x^\infty \exp(\frac{-u^2}{2}) du \\ &= \frac{1}{\sqrt{\pi}} \int_x^\infty \exp\left(-\left(\frac{\mu}{\sqrt{2}}\right)^2\right) d\left(\frac{\mu}{\sqrt{2}}\right), \\ &= \frac{1}{2} erfc\left(\frac{x}{\sqrt{2}}\right) \end{aligned} \tag{2-2}$$

where T_b is the bit duration, $1/T_b$ is the bit rate f_b, A_c is the amplitude of the two modulated signals in BPSK or BFSK. Figure 2-1 (a) and Figure 2-2 (a) show the modulators in which the baseband data is modulated. $p_1(t) = -p_2(t)$ in BPSK modulator, which can be seen from its constellation diagram in Figure 2-1 (b) and the two signals

have 180 phase difference. The two BFSK signals must be orthogonal, illustrated by its constellation diagram in Figure 2-2 (b).

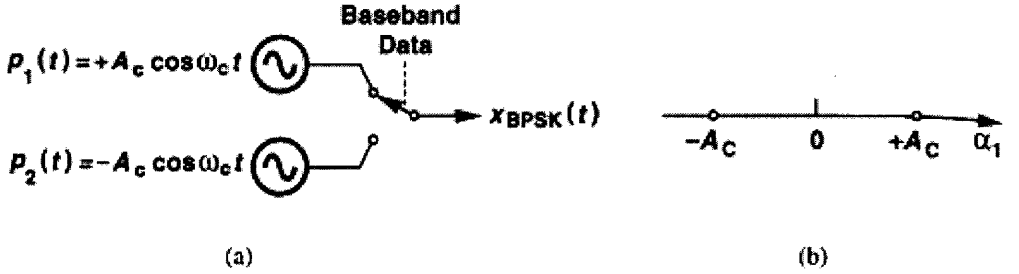


Figure 2-1 BPSK (a) modulator (b) constellation [14]

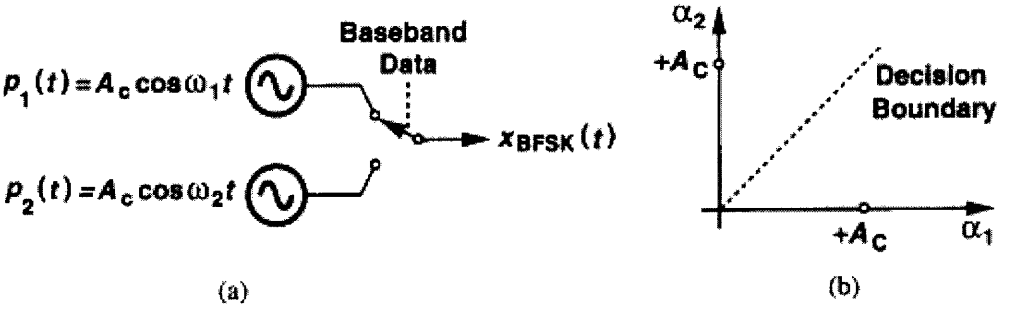


Figure 2-2 BFSK (a) modulator (b) constellation [14]

The BER can be lowered by increasing the signal power or decreasing the data rate. One can say that "BPSK has a 3-dB advantage over BFSK" [14], i.e. transmit power can be 3 dB lower in BPSK, for the same BER.

As regards spectrum occupancy, BPSK occupies $2f_b$ while BFSK depends on the bit rate f_b and the frequency spacing Δf that separates a logic 0 from a logic 1, illustrated by Figure 2-3. The frequency spacing Δf can be as low as $0.5f_b$ [20], but $2f_b$ provides robust communication [21]. If Δf is $2f_b$, the total spectrum occupied by BFSK spreading is $4f_b$, twice that required by BPSK. Nevertheless, BFSK is widely used in low data rate applications where E_b can be maximized by a long bit period.

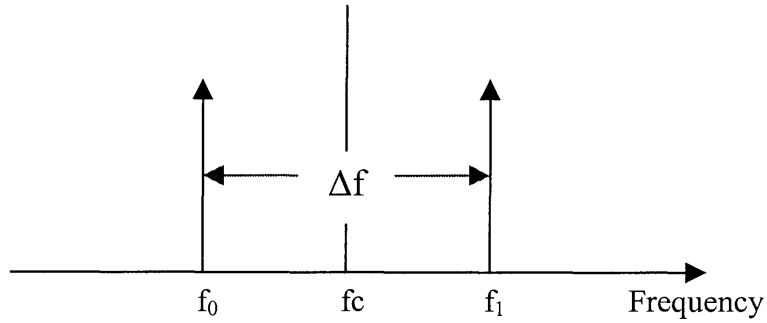


Figure 2-3 Illustration of f1, f0, Δf and fc for BFSK

The FSK technique has better power efficiency performance than PSK since the FSK signal has no abrupt phase change and does not require "spectral regrowth" to smooth the waveform [14]. In other words, FSK has a better adjacent channel power ratio, while PSK requires a complicated circuit to achieve similar performance. The popularity of BFSK stems from the simplicity of its implementation in transmitter and receiver.

In conclusion, BFSK has been chosen for this project.

Table 2-2 Comparison of BFSK and BPSK

	BFSK	BPSK
BER	$P_{e,BFSK} = Q\left(\sqrt{\frac{E_b}{N_0}}\right)$	$P_{e,BPSK} = Q\left(\sqrt{\frac{2E_b}{N_0}}\right)$
Spectral Efficiency	$BW=2f_b + \Delta f$	$BW=2f_b$
Power Efficiency	Good	Poor

3 High-Temperature Transmitter with SOI MOS Varactor

3.1 Introduction

A simple transmitter is shown in Figure 3-1. Considering that the goal of the project is low power and tiny size, the circuit implementation emphasizes simplicity. The transmitter circuitry must collect digital data from the previous stage, the decimation filter; implement the BFSK circuit (voltage-controlled oscillator and tunnel diode); and transmit the modulated signal by a small loop antenna.

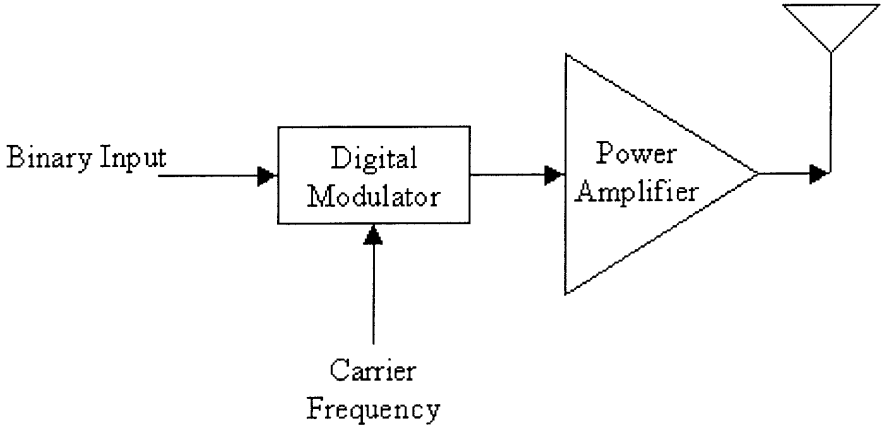


Figure 3-1 A simple transmitter for digital signals.

3.2 Oscillators

At the core of any oscillator is positive feedback at a selected frequency. With no input to the oscillator, it provides a stable and pure sinusoidal waveform [15].

3.2.1 Tunnel Diode and Oscillator Theory

In RLC series resonance circuit, Figure 3-2, its harmonic response will reduce to zero as time progresses because resistance R is a lossy component. If the total resistance in a circuit reaches zero, an undamped sinusoidal response is the output at v(i) and the circuit is called an oscillator. A negative resistance, R1 = -R, can achieve this by

providing a response to compensate the lossy resistance in the circuit. Moreover, to get the oscillation started, the negative resistance R1 is required to be less than –R. This is equivalent to the transfer function having poles in the right-hand side of the complex frequency domain [15].

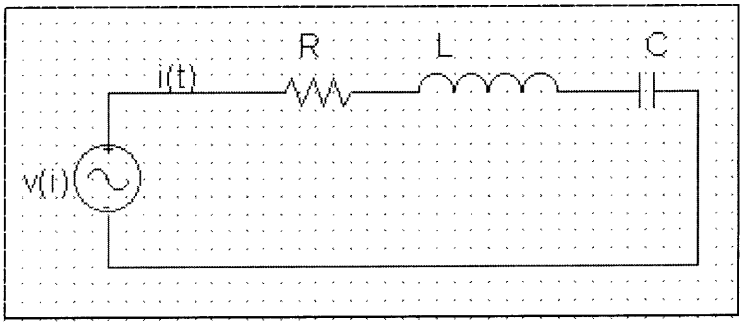


Figure 3-2 Series resonance circuit with voltage-controlled source term after [15]

A simple, direct way to implement such a negative resistance is via a tunnel diode, whose I-V characteristic is shown in Figure 3-3. When biasing voltages are in region d, the resistance is negative. At the high positive biasing voltages (more than V_{diff}), the corresponding current of tunnel diode approaches the current of the conventional pn-junction diode.

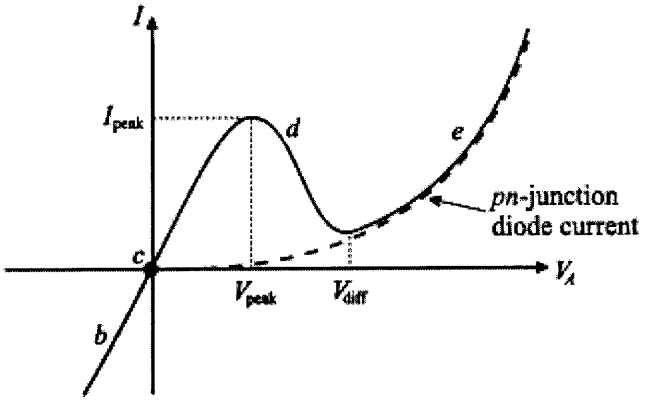


Figure 3-3 Current-voltage characteristic of the tunnel diode from [15]

Tunnel diodes are pn-junction diodes that are made of n and p layers with extremely high doping (about $10^{19} \sim 10^{20}$ cm^{-3}), shown in Figure 3-4. Thus a very

narrow depletion region is created. Moreover, the electrons and holes exceed the effective state concentrations in the conduction and valence bands. As a result, the Fermi level is shifted into the conduction band W_{Cn} of the n^+ layer and into the valence band W_{Vp} of the p^+ layer, shown in Figure 3-4. A very narrow potential barrier, d, exists.

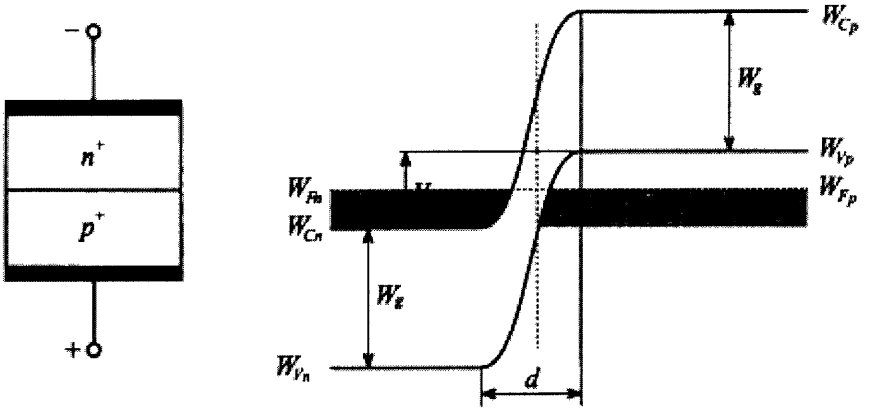


Figure 3-4 Tunnel diode structure and its energy band diagram from [15]

The phenomenon of tunneling allows electrons to be exchanged across the narrow gap rather than having to overcome the potential barrier through an externally supplied voltage. Figure 3-6 clearly illustrates how the corresponding bands deform for four biasing voltages respectively. Please refer to reference [15] for details.

The equivalent circuit of a tunnel diode is shown in Figure 3-5. Here R_S is the resistance of the semiconductor layer and L_S is the associated lead inductance. The junction capacitance C_d is in shunt with a conductance $1/r_d$. Whether r_d is negative or positive depends on the bias voltage.

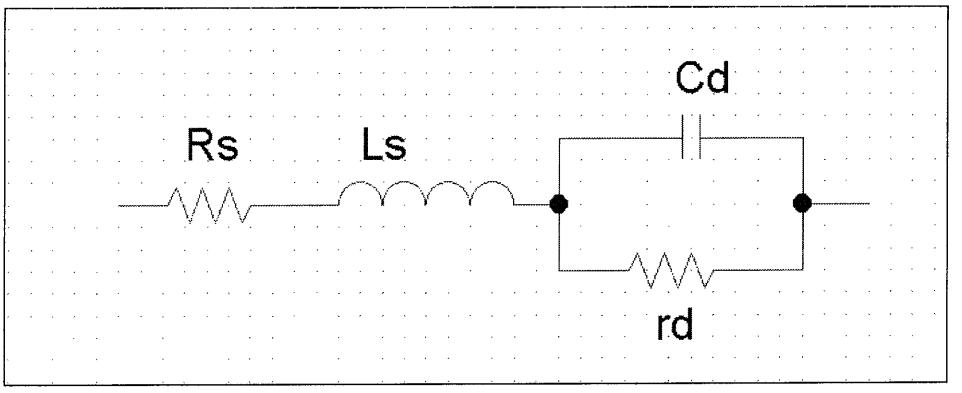


Figure 3-5 Linear circuit model for the tunnel diode

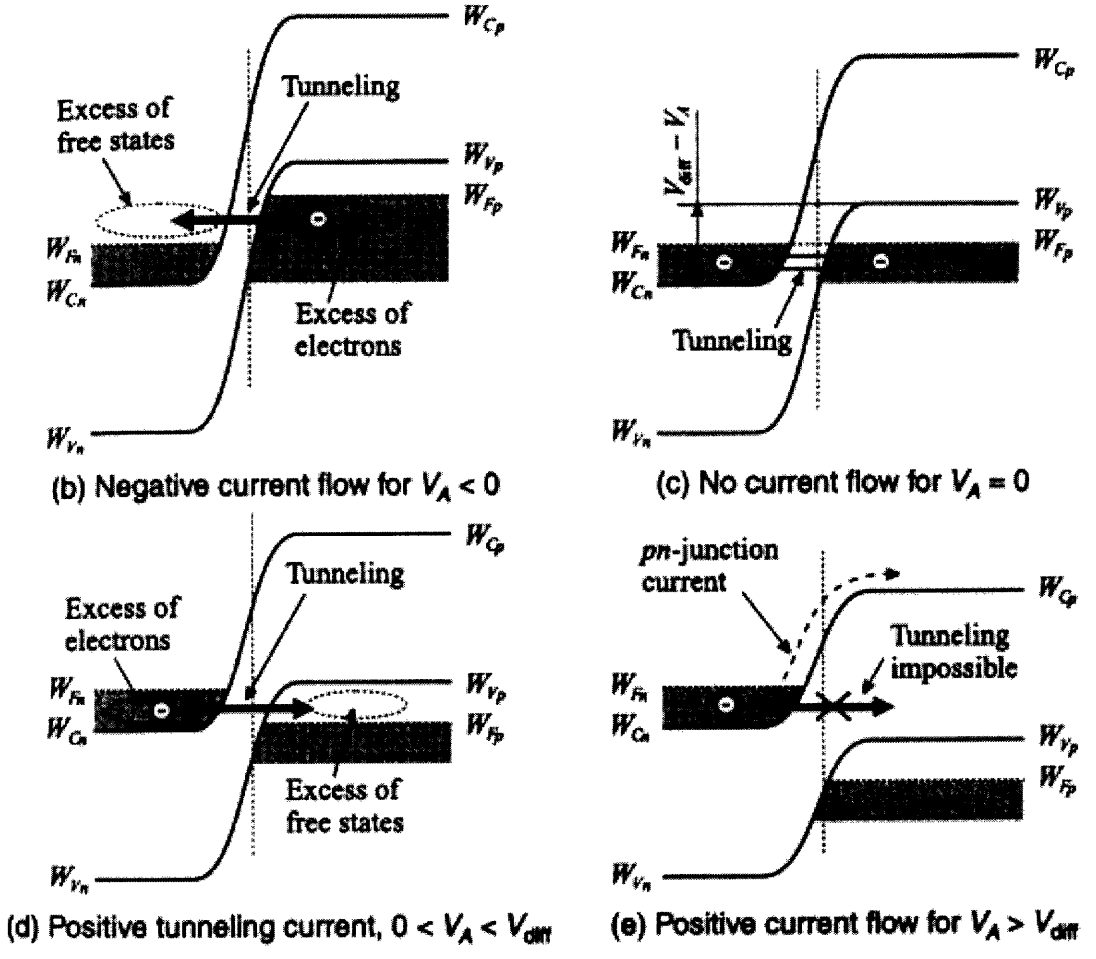


Figure 3-6 Tunnel diode energy band deformation for four distinct situations from [15].

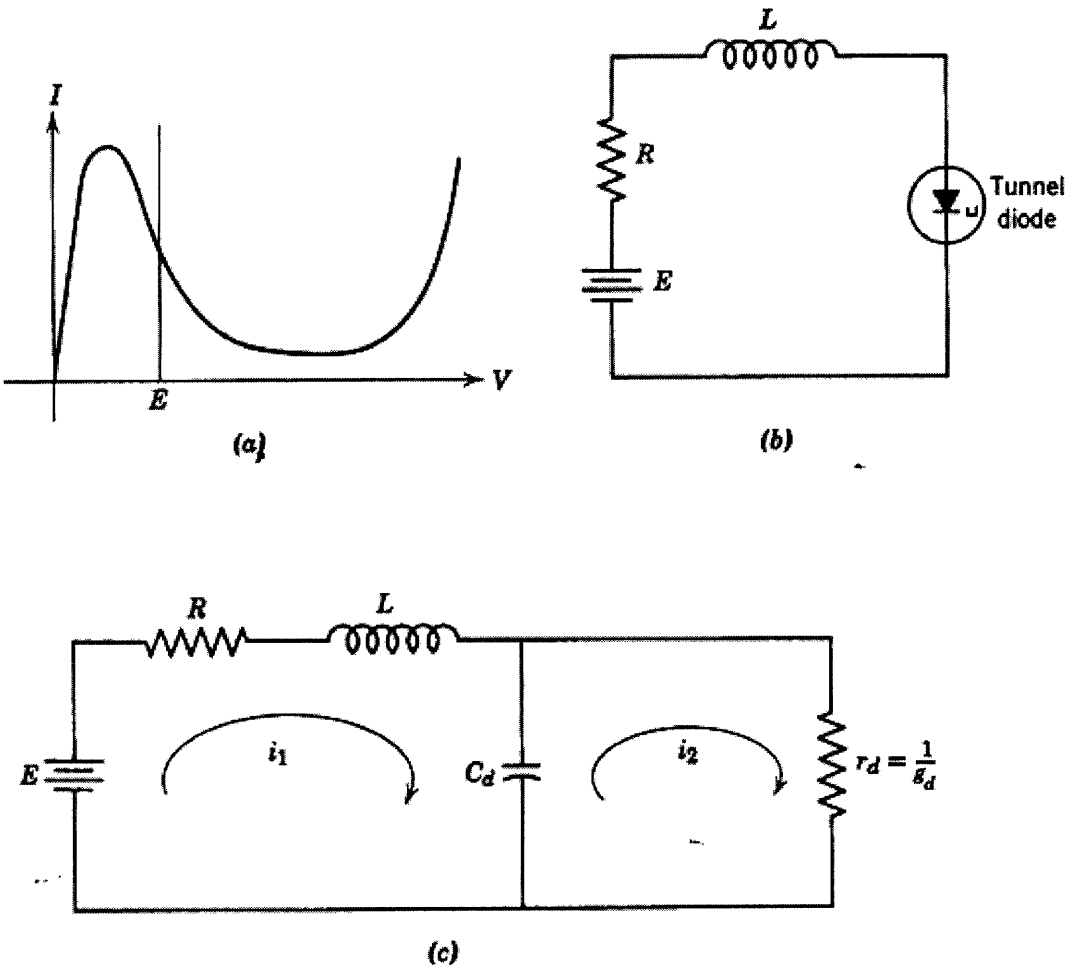


Figure 3-7 General considerations for a tunnel diode oscillator from [16]. (a) Bias point. (b) Simple oscillator circuit. (c) Linear circuit model.

Now let us analyze how to utilize the tunnel diode to make an oscillator. As mentioned before, the tunnel diode must be biased in the region where the resistance is negative, shown in Figure 3-7 (a). For the simple connection, such as Figure 3-7 (b), the oscillation starts if the net conductance of the resultant tank circuit is negative. Here, L can be the total of tunnel-diode Ls and the external inductor; R can be the total of tunnel-diode series resistance and the output resistance of the biasing voltage. Based on the equivalent circuit in Figure 3-7 (c), the loop equations are:

(3-1)

$$\begin{cases} \left(R + L\frac{d}{dt} + \frac{1}{C_d}\int dt\right) i_1 - \frac{1}{C_d}\int i_2 dt = E \\ -\frac{1}{C_d}\int i_1 dt + \left(r_d + \frac{1}{C_d}\int dt\right) i_2 = 0 \end{cases}$$

The roots of the determinant of the above equations indicate the rise or fall of current values and are given by

(3-2)

$$\lambda_{1,2} = \frac{1}{2}\left(-\frac{R}{L} - \frac{g_d}{C_d}\right) \pm \sqrt{\frac{1}{4}\left(\frac{R}{L} + \frac{g_d}{C_d}\right)^2 - \frac{1}{LC_d}\left(1 + Rg_d\right)}$$

When the expression inside square root is negative, λ_1 and λ_2 are complex numbers and the oscillation starts. Consequently, the circuit oscillation will diverge if the real part is positive; will diminish if the real part is negative; and maintain steady-state if the real part is zero, i.e.

(3-3)

$$\frac{1}{4}\left(\frac{R}{L} + \frac{g_d}{C_d}\right)^2 - \frac{1}{LC_d}\left(1 + Rg_d\right) < 0 .$$

The oscillation builds up according to the real part, $\left(-\frac{R}{L} - \frac{g_d}{C_d}\right)$.

To begin an oscillation, the real part has to be positive. The oscillation builds up in the comparatively linear negative-conductance region until its swing spreads into the positive-conductance regions of the nonlinear characteristic. Now the real part is no longer positive. Damping takes place until it falls in linear negative-conductance region. As the oscillation goes back and forth in the linear negative-conductance region, the steady-state oscillation builds up.

Till now, the simple tunnel diode is a good choice for low-power, small-size transmitter. To design the transmitter, we should understand:

1. What is the condition for DC biasing?
2. What is the start-up condition?
3. What is the oscillation frequency?

The parasitic components Ls and Rs, shown in Figure 3-5, are neglected at low frequency (such as 27 MHz) in Figure 3-8.

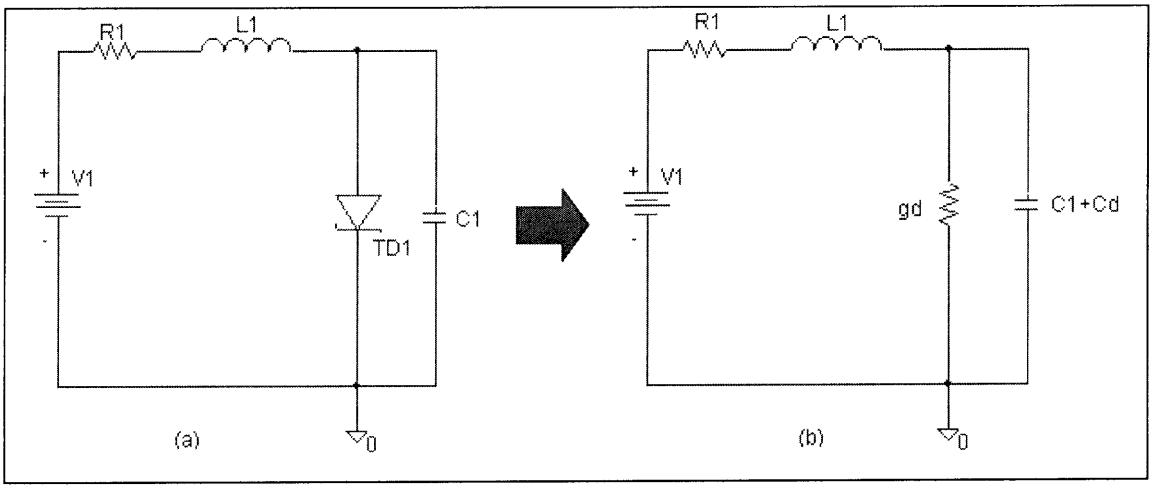


Figure 3-8 A basic oscillator with tunnel diode (a) Schematic (b) Linear circuit model

The tunnel diode is biased in the linear negative-conductance region to provide negative resistance. To oscillate, the resistance looking from the inductor should be negative and can be represented by

(3-4)

$$R_1 < \frac{1}{g_d}$$

To better understand the oscillation start-up condition and the calculation of oscillation frequency, we should start from the circuit impedance looking from V_1,

$$Z = \frac{R_1^2 + \omega^2 L_1^2}{R_1 - g_d\left(R_1^2 + \omega^2 L_1^2\right) + j\omega C_t\left(R_1^2 + \omega^2 L_1^2\right) - j\omega L_1}, \tag{3-5}$$

where $C_t = C_1 + C_{td}$

As stated previously, the condition for oscillation start-up is that the real part of Eq. (3-5) is negative. Meanwhile, the imaginary part becomes zero at resonance. In other words, start-up condition is

$$\frac{R_1}{R_1^2 + \omega^2 L_1^2} < g_d . \tag{3-6}$$

The oscillation frequency is

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L_1(C_1 + C_{td})} - \frac{R_1^2}{L_1^2}} . \tag{3-7}$$

In general, an oscillator based on a tunnel diode is a good choice for this project. Though harmonics and relaxation occur in no high-Q circuit when the oscillation passes through non-linear region, the waveform is practically sinusoidal if the buildup is small.

3.2.2 Variable capacitor using Si PN varactor and SOI MOS varactor

A voltage-controlled oscillator (VCO) is one oscillator whose output frequency can be varied by a voltage. It is usually used in RF oscillators. As a local oscillator, VCO outputs well-defined frequencies by varying voltage on one component to implement front-end down-conversion and up-conversion functions [14]. A VCO can be utilized to implement BFSK modulation in this project. The voltage-controlled capacitor is controlled by the binary data.

This project is the last stage of the wireless interface circuit for high-temperature applications. The purpose is to implement all possible parts in integrated solution to reduce parasitic effects, maximize its working temperature and minimize power consumption. The commercially available varactor works only up to 120 °C. Considering that SOI technology is used in the previous stages, the alternative is a MOSFET capacitor that is provided by the Peregrine UTSi 0.5um process.

However, a VCO implemented using a Si PN varactor is helpful for testing the transmitter circuit at ambient temperature. Shown in Figure 3-9, a varactor has three layers: p+, intrinsic layer I, n+. When it is in the reverse biasing, the capacitance is dominated by the bias-dependant space charge length of the I-layer. A suitable varactor can be fabricated by selecting the doping and thickness of the intrinsic layer.

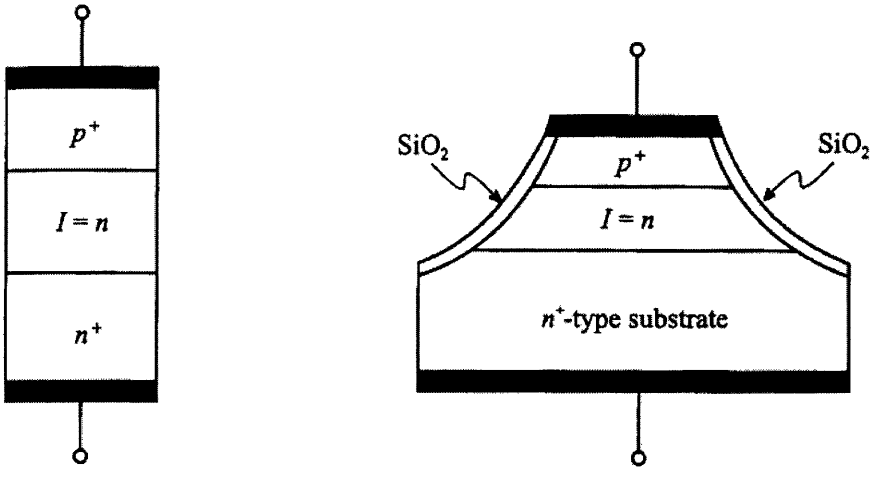


Figure 3-9 (a) Simplified structure of a varactor diode (b) Fabricated cross-section from [15]

To completely understand the SOI MOSFET capacitor, a Si MOSFET capacitor is first discussed. Figure 3-10 shows an idealized NMOS device cross-section with positive V_{GS} applied. When a negative gate voltage is applied and V_{GS} is less than its flatband voltage V_{FB}, the depletion layer collapses. The device is working in the accumulation

region and the capacitance is the gate oxide capacitance and is given by (3-8). As V_{GS} passes through V_{FB}, a small depletion layer forms and the depletion capacitance starts taking effect. Gate oxide capacitance is in series with this increasing depletion layer capacitance shown in (3-9). As V_{GS} is further increased toward threshold voltage, the depth of depletion layer increases to the maximum. The depletion layer in p type could not provide enough thermally generated electrons to respond to the gate. However, the induced inversion layer appears and n+ diffusions (source and drain) provide a very large soruce of electrons. Therefore, the capacitance in inversion mode is dominated by the gate oxide capacitance. Figure 3-11 illustrates the three capacitance regions.

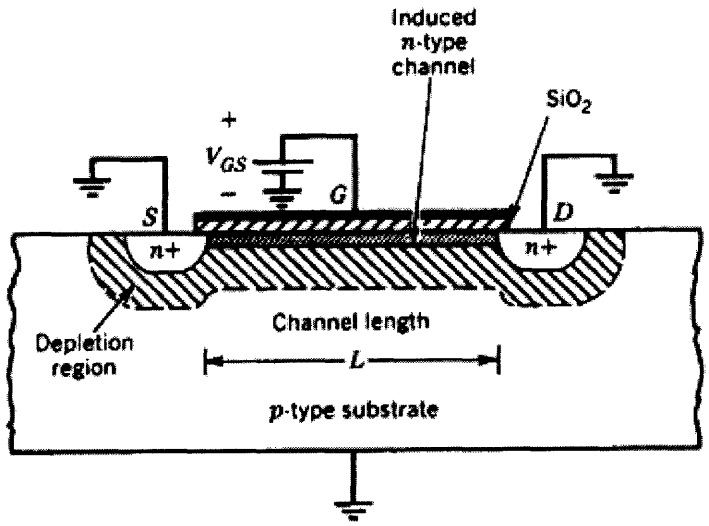


Figure 3-10 Idealized NMOS device cross-section with positive V_{GS} applied, showing depletion regions and the induced channel from [10]

(3-8)

$$C_{accumulation} = C_{inversion} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

(3-9)

$$C_{depletion} = C_{ox} + C_d = \frac{\varepsilon_{ox}}{t_{ox}} + \frac{\varepsilon_{Si}}{d}$$

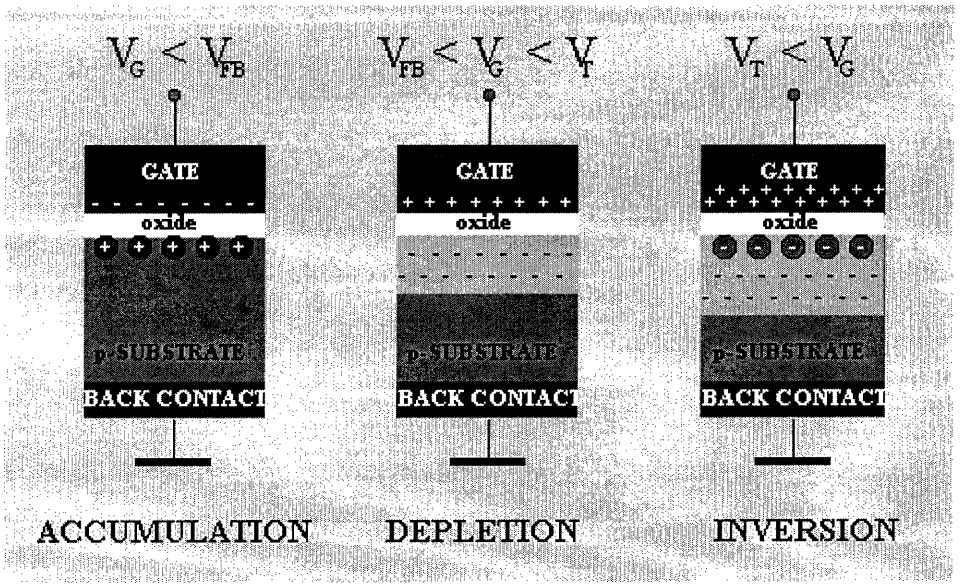


Figure 3-11 Illustration of an MOSFET capacitor.

Figure 3-12 shows MOSFET capacitance versus gate voltage. The model is from the TSMC 0.35um process T06G fabrication, and the simulation was done for NMOS W/L= 100μm/50μm. This simulation model has a very abrupt transition between depletion and inversion which is idealized, but fairly accurate considering that the source and drain are tied to the bulk.

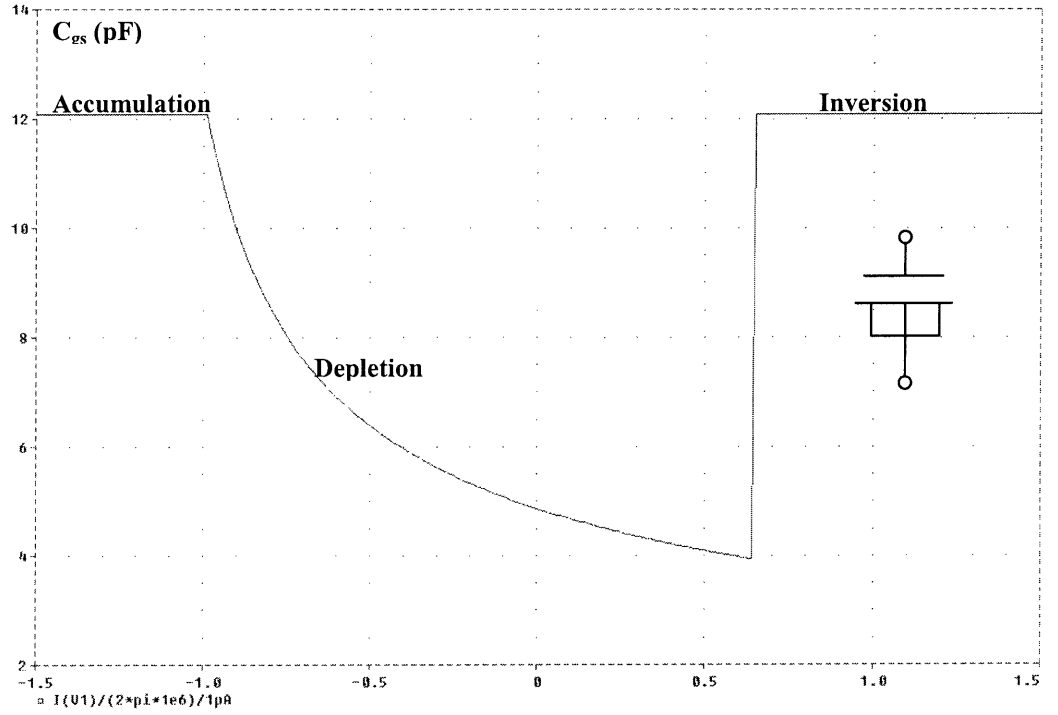


Figure 3-12 Simulated n-channel MOSFET capacitance versus gate voltage for TSMC 0.35 um process T06G model, W=100um, L=50um.

In the Peregrine UTSi 0.5μm process, the substrate of the MOSFETs is fully depleted. MOSFET capacitance consists of overlap capacitance and parallel place capacitance [18].

The overlap capacitance is created by the overlap of the gate polysilicon over the edge of the Lightly-Doped Drain (LDD) region. This capacitance is relatively constant with the applied gate voltage and is defined in the SPICE models as Cgs and Cgd. The parallel plate capacitance is the gate oxide capacitance in Si process, which is highly variable, depending on V_{GS}.

When V_{GS} is above threshold voltage (positive for N-channel; negative for P-channel), the device is operating in the inversion region, and there is a source of electrons in the source and drain that create a sheet of electron inversion charge. The capacitance is dominated by the parallel plate capacitance (C_{ox}), shown in Figure 3-13. When the

devices are in accumulation mode, there is no source of holes present to respond to the gate surface, so the capacitance is very low. Essentially, there is no second plate in the parallel plate capacitor to match the gate poly because the channel region of the transistor is fully depleted. The transistor capacitance is therefore very low below threshold (Figure 3-13) and consists mainly of overlap capacitance [18]. This is good for our BFSK application because the data stream output from the decimation filter consists of two voltages: 0V and 3.3V. If we use either the RN or RP transistor, we can obtain two distinct capacitances that in turn affect the oscillation frequency. Thus, the SOI transistor is used to implement the voltage-controlled oscillator.

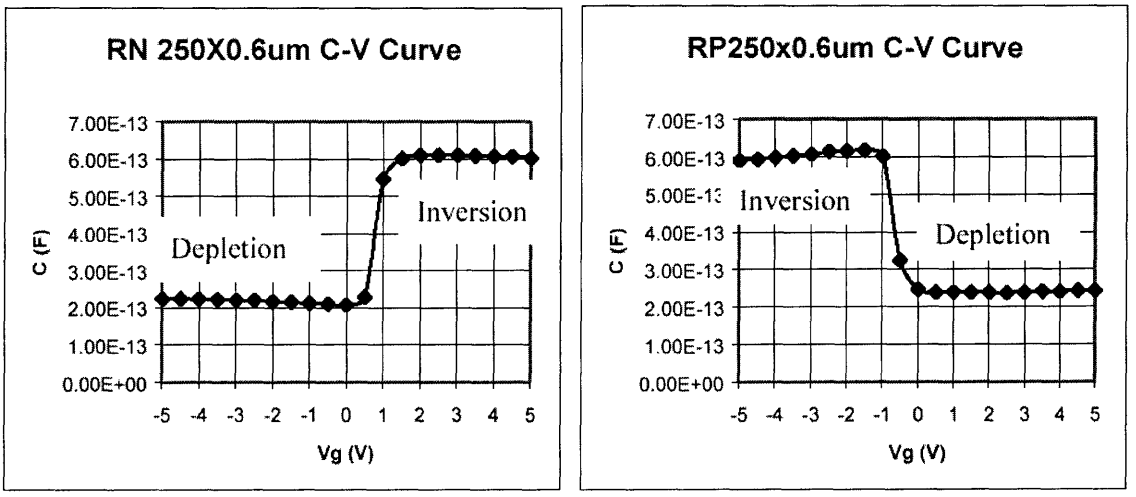


Figure 3-13 RN and RP capacitance versus gate voltage for Peregrine UTSi 0.5um process from [18]

For MOSFET capacitors in both the Si and SOI process, quality factor Q depends on the channel resistance, which is given by

(3-10)

$$r_{ds} \approx \left[\mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) - V_{DS}/2 \right] \right]^{-1}.$$

We can use the model in Figure 3-14 to calculate Q factor. The model identifies the maximum resistance – that from the center of the channel to the source-drain

connection – and puts that worst-case value in series with all the capacitance. Nevertheless, the practical minimum-device length is suggested to minimize the r_{ds}.

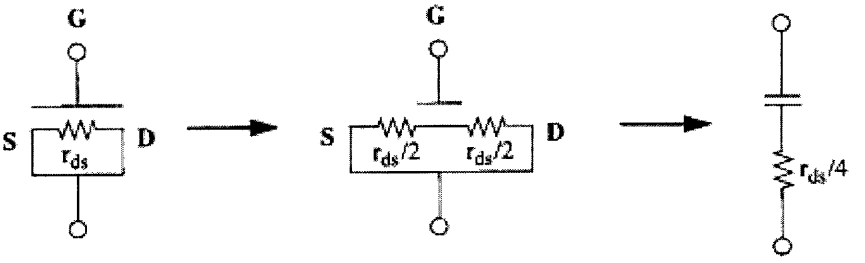


Figure 3-14 Evolution of the lumped gate capacitor model (from [9]).

3.3 Transmitter Circuit Design and Analysis

The transmitter consists of a small, planar loop antenna (inductor), a tunnel diode and the SOI MOSFET or Si PN varactor. The simplified circuit is shown in Figure 3-15.

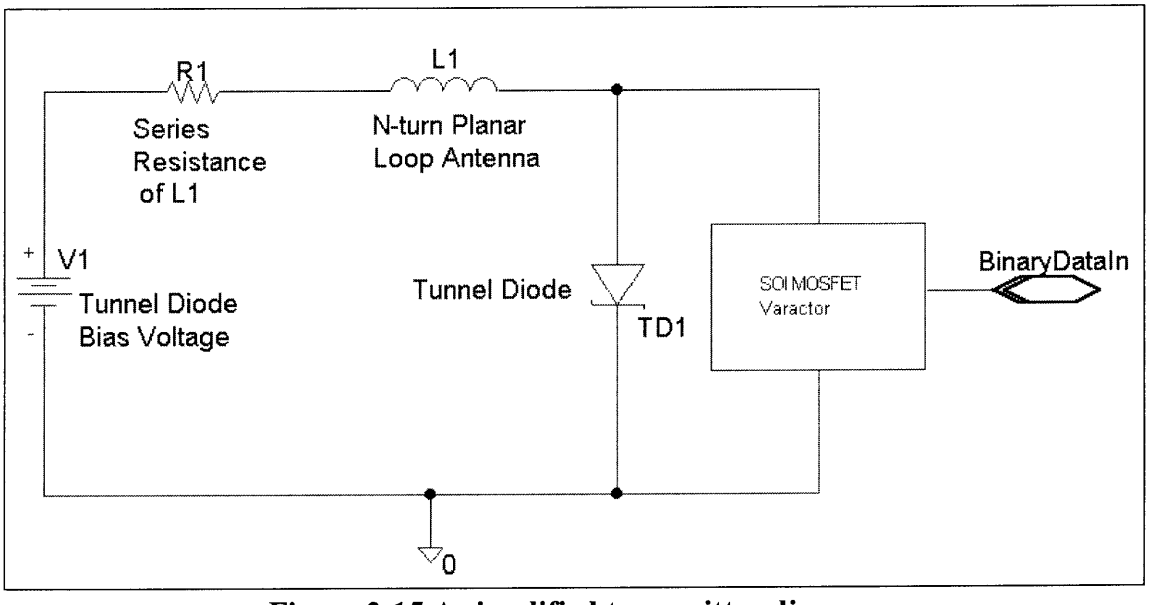


Figure 3-15 A simplified transmitter diagram

3.3.1 N-turn Planar Loop Antenna and its inductance

The quality of the antenna can be quantified using its radiation efficiency, which is defined as the ratio of the power delivered to the radiation resistance R_r to the power delivered to R_r [19] and the loss resistance R_L. It is written as

(3-11)

$$e_{cd} = \frac{R_r}{R_r + R_L},$$

where R_r is proportional to the square of N while R_L is proportional to N. The loss resistance is the total ohmic resistance, including surface impedance of conductor, ohmic resistance and ohmic skin effect resistance [19].

The planar loop antenna in this project was implemented on a printed circuit board for convenience at this stage, and will ultimately be implemented on a high-temperature technology, such as gold-on-ceramic. The circuit size must be minimized. Considering the transmission distance is about 1 meter, the antennae operate in the near field (r << wavelength). For a small loop antenna, radiation in the near-field is inductive [19]. With the goal of 2-cm diameter, the square loop was selected to maximize the area because radiation power is proportional to the square of loop area and 2cm x 2cm square loop has larger area than 2cm diameter circular loop. To further increase the radiation power, a 2-turn, square-shape with 2 cm side length planar loop antenna is employed. From the aspect of inductance, the feasible capacitance must be considered to ensure that the resonant frequency is 27MHz.

A small loop antenna is primarily inductive and its impedance is given by [19]

(3-12)

$$Z = (R_r + R_L) + j(\omega L_A + \omega L_i),$$

where

R_r : radiation resistance

R_L : loss resistance of loop antenna

ωL_A : external inductive reactance of loop antenna

ωL_i : internal high-frequency reactance of loop conductor

Eq. (3-12) is stated in reference [19], but the calculation for L_A and L_i doesn't apply for the multi-turn planar loop. There are two books and one paper which discuss the inductance of a planar loop inductor. Thomas H. Lee analyzed the planar spiral inductor for on-chip inductor in his book [9]. The value of the hollow spiral inductor was given by

(3-13)

$$L \approx \frac{45\mu_0 n^2 a^2}{22r - 14a},$$

where a is the square spiral's mean radius, defined as the distance from the center of the inductor to the middle of the windings. $2r$ is the width of the outmost side. μ_0 is the permeability of the free space. (3-13) has an error of fewer than 5%. The idea of the hollow spiral inductor, Figure 3-16, is excellent for our application. With the removal of several innermost turns, the inductor Q is improved and the center space can be utilized for all the other components to minimize total circuit size.

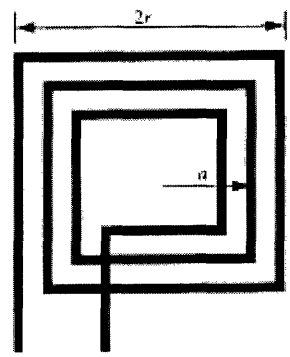


Figure 3-16 Hollow spiral inductor from [9]. A two-turn inductor was used in this work.

Reference [22] presents simple and accurate expressions for planar spiral inductances. The modified wheeler formula was given by

(3-14)

$$L_{mW} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho},$$

where the average diameter $d_{avg} = \frac{d_{out} + d_{in}}{2} = 2a$, the fill ratio $\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$.

Parameter d_{out} is the outermost diameter, d_{in} is the innermost diameter. The coefficients K1 and K2 are layout dependant and are shown in Table 3-1. The fill ratio represents how hollow the inductor is. The two inductors with the same d_{out}, but different fill ratio have the different inductances. The full one has a smaller inductance because its inner turns are closer to the center of the spiral and so contribute less positive mutual inductance and more negative mutual inductance [22].

Table 3-1 Coefficients for the modified Wheeler expression

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

J.M.C. Dukes also analyzed the flat spiral coil inductor on printed circuit board in 1961. The formula was borne out from experiment and was given by [23]

(3-15)

$$L = 0.0241 a N^{\frac{5}{3}} \log \frac{8a}{c} (\mu H),$$

where a is the mean radius, $a = \frac{1}{2} d_{avg}$, N is the number of turns, c is the radical depth of winding, $c = \frac{1}{2}(d_{out} - d_{in})$.

Table 3-2 shows the calculated inductances for a 2-turn, square spiral inductor. Its d_{out} is 2.286cm, and d_{in} is 1.905cm.

Table 3-2 Calculated inductances using three methods

	Equation (3-13)	Equation (3-14)	Equation (3-15)
Inductance	237 nH	198 nH	305 nH

3.3.2 Tunnel Diode Based Oscillator

A Germanium tunnel diode is proposed for the high-temperature environment. Referring to the calculated inductances and the tunnel diode's equivalent circuit model shown in Figure 3-5, the junction capacitance C_d plays an important role on selecting tunnel diode while taking the other parameters in Figure 3-3 into consideration. The peak current dominates the power consumption of the oscillator. The difference between the peak and the valley current leads the oscillation amplitude. The mean of the voltages at the peak current and valley current is the biasing voltage and the mean of the peak current and valley current is the biasing current.

The Silicon tunnel diode 1N4397 from American Microsemiconductor Inc. was used in this work to test the principle of operation. Its parameters are shown in Table 3-3. The manufacture-specified temperature is 200 C. The junction capacitance can be up to 200 pF due to manufacturing variation. Assuming the inductance is 200 nH, the resonance frequency is about 25 MHz. With the variation of devices, a resonance frequency of 27 MHz is feasible. A Germanium tunnel diode having the same

performance is available from this company and it is able to work at temperatures up to 300 C.

A polynomial model of the tunnel diode has been frequently used in SPICE simulation [24]. In this work, a 3-region behavior model based on the physics of the device is used in this project. Behavioral Modeling is the process of developing a model for a device from the viewpoint of externally observed behavior [24]. Besides used in modeling for new device types, it can be used as a black-box modeling of complex systems [24]. The main characteristics of a tunnel diode I-V curve consist of peak voltage and current, valley voltage and current and projected peak voltage. Shown in Figure 3-17 and Table 3-3, the specific tunnel diode model is utilized in simulation to implement the design. Its current flow can be approximated impacted by three distinct effects: (1) thermal current, which is analogous to the conventional diode; (2) tunnel current, which is from direct tunneling; (3) excess current, which is not from direct tunneling [24]. The above three effects are represented by PSPICE transconductance devices G1, G2 and G3 respectively in Figure 3-17, Eq.(3-16), Eq.(3-17) and Eq.(3-18). As I-V curve shown in Figure 3-18, all the parameters are within the specification limit. The bias condition can be done in the middle of linear region, whose voltage is about 210 mV and the current is 1.75 mA. The power consumption for this tunnel diode oscillator is only 370 uW, which satisfies our low-power goal.

Table 3-3 Parameters of the 1N4397

V(f) at I_{peak}	690 mV
I_{peak} Max.	2.2 mA
I_{peak} Tolerance	0.22 mA
V_P at I_{peak}	80 mV
V_v at I_{valley}	510 mV
I_{peak} / I_{valley}	2.5
I(f) Max.	4.5 mA
r(s) Max.	2 ohm
C(t) Max.	200 pF
T(operating) Max.	200 C

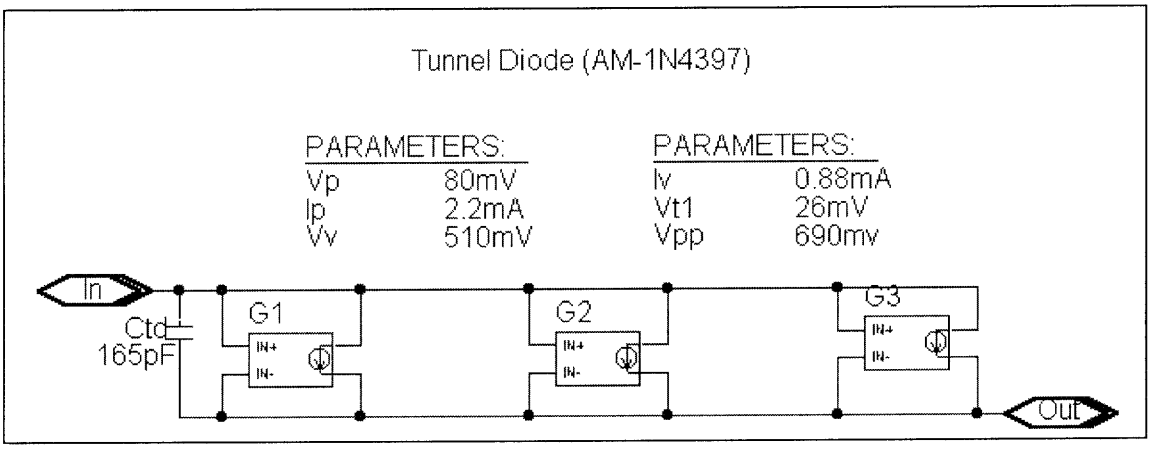


Figure 3-17 Behavioral model for the 1N4397 using PSpice

(3-16)

$$I_1 = I_p e^{-\frac{V_{pp}}{V_{t1}}} e^{\left(\frac{V(\%IN+,\%IN-)}{V_{t1}}-1\right)}$$

(3-17)

$$I_2 = I_p V(\%IN+,\%IN-) e^{\left(\left(1-\frac{V(\%IN+,\%IN-)}{V_p}\right)*0.8\right)}$$

$$I_3 = I_v \frac{V(\%IN+,\%IN-)}{V_V} e^{(V(\%IN+,\%IN-)-V_V)} \quad \textbf{(3-18)}$$

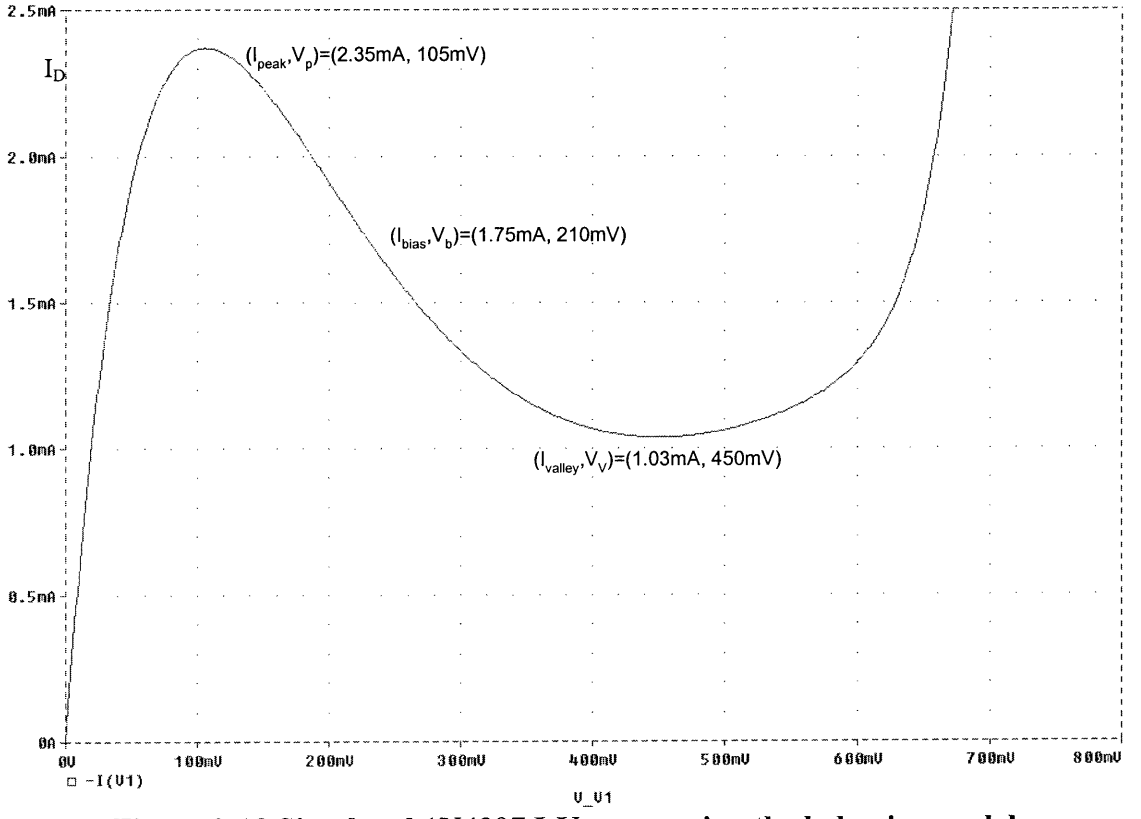


Figure 3-18 Simulated 1N4397 I-V curve using the behavior model

As shown in Figure 3-18, the tunnel diode-based oscillator is biased by 210 mV. It could not be biased by current because there are several voltages existing with the same biasing current, i.e. there exists uncertainty for current biasing. The negative resistance – g_d = -7 mA/V is obtained from the simulation model. Table 3-4 shows the used parameter. Referring to section 3.2.1, the condition for DC biasing and oscillation start-up, and the calculation of resonance frequency are analyzed with this tunnel diode and the 2-turn planar square spiral inductor, shown in Table 3-5. The power supply's output resistance is critical and should keep as low as several ohms. Therefore a large bypass

capacitor is loaded in shunt with the power supply in order to ensure the impedance across the power supply is very low at resonance.

Table 3-4 Parameters used in tunnel-diode-based oscillator

Description	Equation	Value
g_d	$-g_d = \frac{\Delta i}{\Delta v}$	7 mA/V
L1	$L_{mW} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}$	200 nH
Ctd		170 pF

Table 3-5 Operating conditions for tunnel-diode-based oscillator

Description	Equation	Value
DC bias condition	$R_1 < \frac{1}{g_d}$	R1 < 140 ohm
Start-up condition	$\frac{R_1}{R_1^2 + \omega^2 L_1^2} < g_d$	Yes
Resonance Frequency	$f = \frac{1}{2\pi}\sqrt{\frac{1}{L_1(C_1 + C_{td})} - \frac{R_1^2}{L_1^2}}$	27.31 MHz

The simulation was also done to verify the above analysis. In Figure 3-19, an output resistance R1 = 6.7 ohm was used. If R1 is too large, the start-up condition would not be satisfied and the circuit will not oscillate. If R1 is very small, the current going through the tunnel diode is distorted. This would not have much impact on the oscillator being used as a transmitter. The most effective part to radiate is the inductor, not the tunnel diode. R1 will also affect the resonance frequency, as shown in Eq (3-7). When R1 is close to zero, only the inductor L and the capacitance C dominate the resonance

frequency, which is same as the ideal LC tank oscillator. In our project, the series resistance R1 from inductor and the power supply output is very small and is negligible. Though the biasing power supply output resistance might not be that small, we can always place a shunt capacitor, which should have the extreme low impedance at resonance frequency. As we see the current going through the tunnel diode from Figure 3-19, there is little distortion on the peak. The inductor current appears to be a pure sine wave.

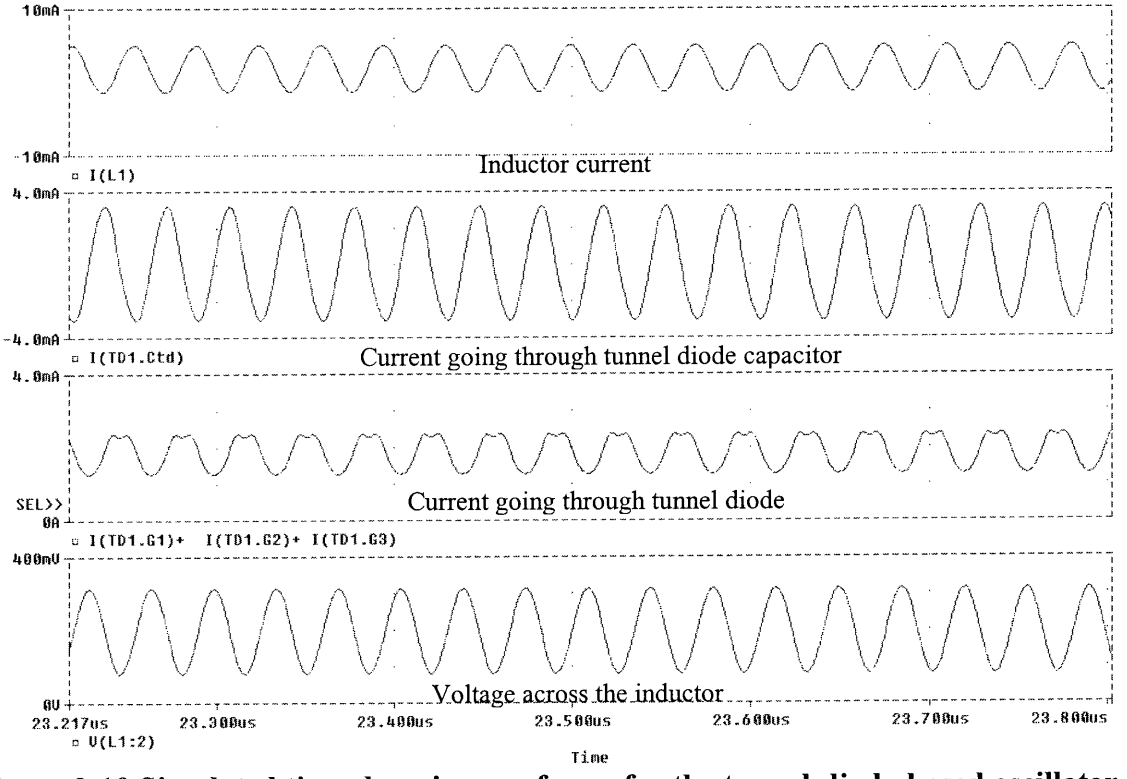


Figure 3-19 Simulated time-domain waveforms for the tunnel-diode-based oscillator (R1 = 6.7 ohm)

3.3.3 Tunnel-Diode-Based, Voltage-Controlled Oscillator using SOI MOSFET Capacitors

With the implementation of tunnel-diode-based oscillator, the next step is to accomplish a BFSK modulator. As stated in 3.2.2, SOI MOSFET capacitor was

employed in this project. When V_{GS} exceeds the threshold voltage, the MOSFET is in inversion and the capacitance is represented by

(3-19)

$$C_{inversion} = W \cdot L \cdot C_{ox} = W \cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

When V_{GS} is below threshold, the device is fully depleted and the capacitance is given by

$$C_{depletion} = L\left(C_{gs0} + C_{gd0}\right)$$

t_{ox} provided by Peregrine UTSi 0.5um process is 10.5 nm, both C_{gs0} and C_{gd0} are 3.6 x 10^{-10} F/m. The capacitance in inversion mode is 19.98 pF for a device with W=120 um, L=50 um. The calculated depletion capacitance for the same device is 36 fF. The calculation was also verified by simulation. The results are very close as shown in Table 3-6.

Table 3-6 Comparison of calculated and simulated NMOS capacitance

t_{ox}	10.5 nm	
W	120 um	
L	50 um	
C_{gs0}, C_{gd0}	3.6 x 10^{-10} F/m	
	Calculation	**Simulation**
$C_{inversion}$	19.98 pF	19.72 pF
$C_{depletion}$	36 fF	87 fF

The same-size PMOS device was used in this project. By choosing Cg much more than the required modulation capacitance, we can use off-chip tuning capacitor to tune the modulation bandwidth in order to adapt to the variation.

The SOI MOSFET capacitance is controlled by the data stream, which is the output of digital circuit. This changes the equivalent circuit model, which is given in

Figure 3-8. The new schematic and its small-signal equivalent circuit are shown in Figure 3-20, in which a PMOS transistor is used as the varactor. R1 was eliminated because it can be negligible by shunting a capacitor whose impedance at resonance 27 MHz is extremely small. The admittance is given by

(3-20)

$$Y = \frac{1}{j\omega L_1} - g_d + j\omega C_{td} + \frac{1}{R_2 + \frac{1}{j\omega C_{mg}}}$$

(3-21)

$$Y = -g_d + \frac{\omega^2 R_2 C_{mg}^2}{1+\omega^2 R_2^2 C_{mg}^2} + \frac{1}{j\omega L_1} + j\omega C_{td} + \frac{j\omega C_{mg}}{1+\omega^2 R_2^2 C_{mg}^2}$$

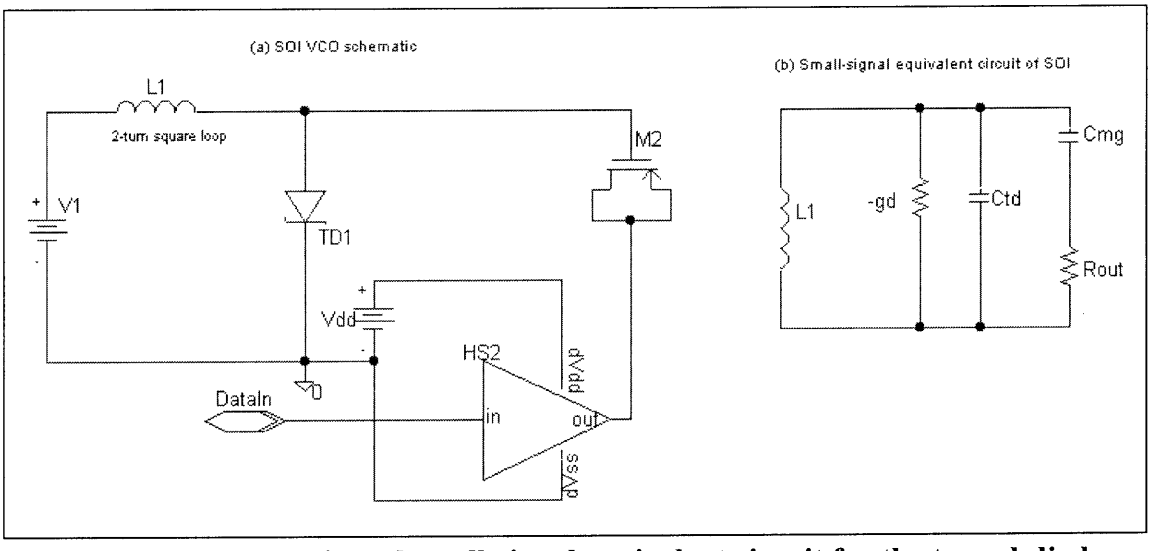


Figure 3-20 Schematic and small-signal equivalent circuit for the tunnel-diode-based oscillator

As stated in 3.2.1, the condition for oscillation start-up is to ensure the negative real part. The oscillation frequency is determined by the imaginary part, which is equal to zero upon resonance. To simplify the above circuit, the high-Q branch of SOI

MOSFET capacitor in series with the digital buffer's output resistance was desired, i.e. Eq. (3-22) should be satisfied.

$$\omega^2 R_2^2 C_{mg}^2 = \omega^2 \left(R_{mg} + R_{out}\right)^2 C_{mg}^2 << 1 \quad \textbf{(3-22)}$$

The digital buffer's output resistance, R_{out}, was designed very small by increasing the ratio of width to channel length. Obviously, the series resistance of M2 in Figure 3-20, R_{mg}, is dominant because the ratio of W/L is only 300/125. R_{mg} can be calculated by Eq. (3-10). Referring to Figure 3-14, $R_{mg} = \frac{1}{4} r_{ds} = 1800/4 = 450\Omega$. Under the condition of 27 MHz, Eq. (3-22) is not satisfied (2.32 > 1). The denominator of Eq. (3-21) at 27 MHz is 3.3 and it can be simplified to

$$Y \cong -g_d + \frac{\omega^2 R_2 C_{mg}^2}{3} + \frac{1}{j\omega L_1} + j\omega C_{td} + \frac{j\omega C_{mg}}{3} \quad \textbf{(3-23)}$$

The start-up condition is still met because g_d is 7 mA/V, shown in Table 3-4 while $\frac{\omega^2 R_2 C_{mg}^2}{3} = 1.7$ mA/V.

Regarding the oscillation frequency, the SOI MOSFET capacitance C_{mg} is only one third of the capacitance without series channel resistance. The larger the channel series resistance is, the higher the oscillation frequency is. When the channel series resistance is increased, the effective capacitance is less than the total capacitance, further leading to the total capacitance decreasing, in the other hand, the oscillation freq is going up. The simulation further proved the above analysis. Shown in Table 3-7, the simulation matches with the calculation.

Table 3-7 The effect of channel shape factor on oscillation frequency

W/L (um/um)	600/10	120/75
L1 (H)	2.00E-07	2.00E-07
C_{td} (F)	1.50E-10	1.50E-10
C_{mg} (F)	1.97E-11	6.57E-12
f (calculated) (Hz)	**2.73E+07**	**2.84E+07**
f (simulated) (Hz)	**2.74E+07**	**2.83E+07**

For a high-Q system, which satisfies Eq. (3-22), the start-up condition and the oscillation frequency are shown in Table 3-8.

Table 3-8 Oscillator parameters for high-Q oscillator using MOSFET varactor

Start-up condition	$\omega^2 R_{mg}^2 C_{mg}^2 < g_d$
Oscillation Frequency	$\omega = \sqrt{\frac{1}{L_1(C_{td}+C_{mg}) - R_{mg}^2 C_{mg}^2}}$

The comparison between hand calculation and simulation was also made when the SOI PMOS capacitor are not in effect. It was done based on the schematic in Figure 3-20 and the result is shown in Table 3-9.

Table 3-9 Calculated and simulated frequency for C_{mg}=0

W/L (μm / μm)	120/50
L_1 (nH)	200
C_{td} (pF)	165
f (hand calculated) (MHz)	27.71
f (simulation) (MHz)	27.23

3.3.4 Buffer Design

The digital buffer is required to provide a fast transient response. Only the PMOS capacitor is effective when its drain/source-gate voltage is larger than its absolute

threshold voltage, as shown in Figure 3-13 and Table 3-6. For an inverter buffer, its PMOS takes more important role than its NMOS (the PMOS is in triode while the NMOS is off). Therefore, the rising time, which is defined by the time from the low voltage to 90% of the high voltage, is the focal point and given by

(3-24)

$$t_x = \tau_p \left[\frac{|V_{TP}|}{(|V_{gs}| - |V_{TP}|)/2} + \ln\left(\frac{|V_{gs}| - |V_{TP}|}{(V_{hi} - V_x)/2} \right) \right] \text{[25]}$$

where τ_P is represented by

(3-25)

$$\tau_P = \frac{C}{\left(\frac{W}{L} u_p C_{ox} (|V_{gs}| - |V_{TP}|) \right)} \text{[25]}$$

The data rate output from the decimation filter is 125 kbps, i.e. the period for each bit is 8 μs. The transition time must be much less than 8 us. Suppose that t_x is << 10% of bit period (8 us), for this case, the τ_P must be << 0.26 us for Peregrine UTSi 0.5um process. In Eq. (3-25), C is the load capacitance that is SOI PMOS capacitor, 20pF. All the other parameters are known, the condition for the W/L ratio is given by

(3-26)

$$\frac{W}{L} >> 0.3$$

The propagation delay is another factor of the fast transition. The unit buffer was designed in Figure 3-21. In digital circuit design, the regular N-channel and the P-channel transistors were used in order to minimize the current leakage. To minimize the propagation delay, the optimized number of the buffers is given by

$$N = \ln\left(\frac{C_L}{C_U}\right) \tag{3-27}$$

where C_L is the load capacitance, 20 pF in our project; C_U is the input capacitance of the unit buffer, including the gate-source capacitance for both PMOS and NMOS, the gate-drain capacitance for both PMOS and NMOS. C_u is represented by

$$C_U = \left(C_{gs0}W + WLC_{ox}\right)_p + \left(C_{gd0}W\right)_p + \left(C_{gs0}W + WLC_{ox}\right)_n + \left(C_{gd0}W\right)_n \tag{3-28}$$

N is about 7 based on the above data. Though it is the optimized value, the practical number of buffer is about 3 to 4. The four-stage buffer was used in this project. Their W/L ratios are 1x, 3x, 4x, 3x. The total propagation delay is 36 times of the unit delay, which is the delay of the decimation filter output.

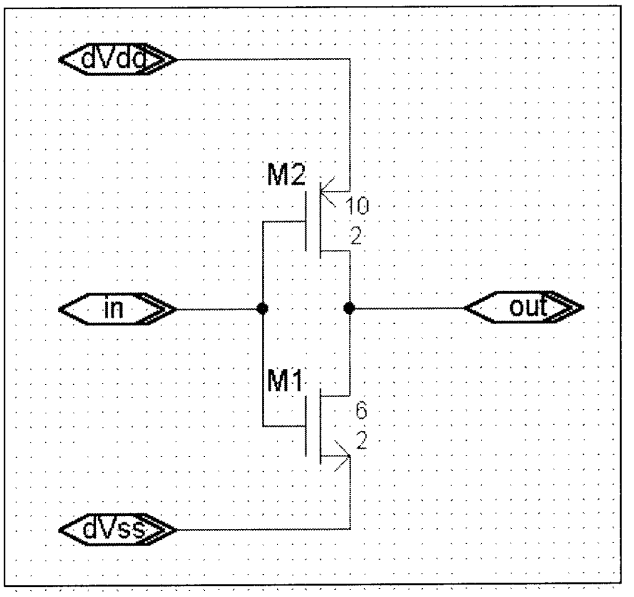


Figure 3-21 Unit inverter design in Peregrine UTSi 0.5um process

3.3.5 *Complete Oscillator Design*

The final circuit was designed using two SOI PMOS capacitors to decrease the size of its driving buffer, shown in Figure 3-23. The layout is shown in Figure 3-28 (b). The above analysis about the oscillation frequency can be applied too. Shown in Figure 3-22, the two parallel PMOS capacitors can be regarded as the capacitor doubled while the resistor is half. Because the product of the $R_{mg}/2$ and $2C_{mg}$ doesn't change, Eq. (3-23) is still applicable.

In Figure 3-23, the circuit enclosed by the blue box is the part of SOI IC that includes A/D converter, decimation filter as well. Figure 3-28 (b) illustrates this. The left of the circuit is on PCB. In the last stage of the digital buffer, the size of the PMOS transistor (320/4) was designed much larger than the size of the NMOS transistor (22/2). The PMOS transistor plays a role in oscillation (changing the frequency to implement VCO) and the NMOS does not, but later the author is aware that both of them have impacts on the transition time.

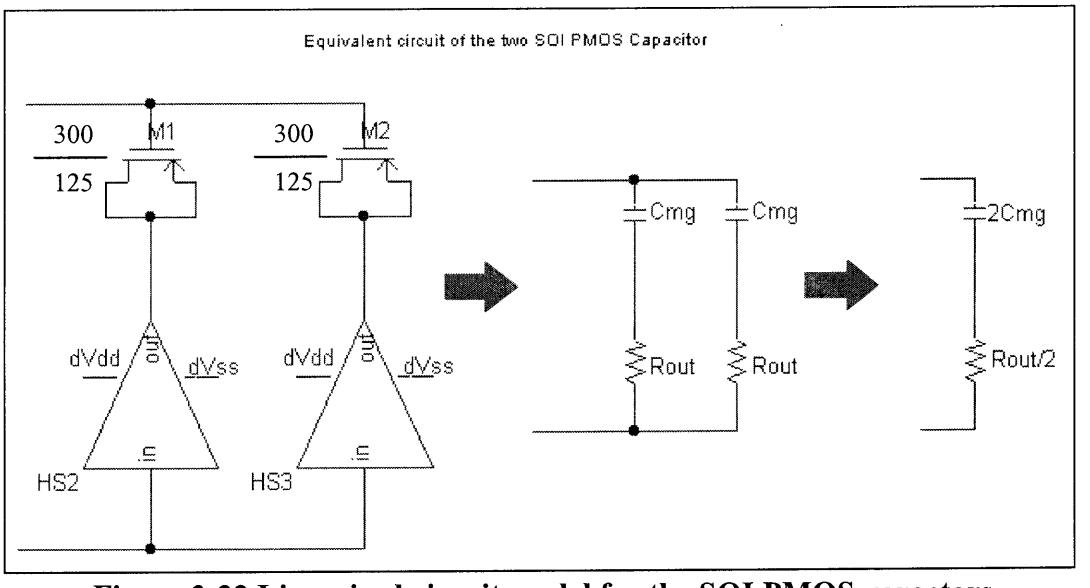


Figure 3-22 Linearized circuit model for the SOI PMOS varactors

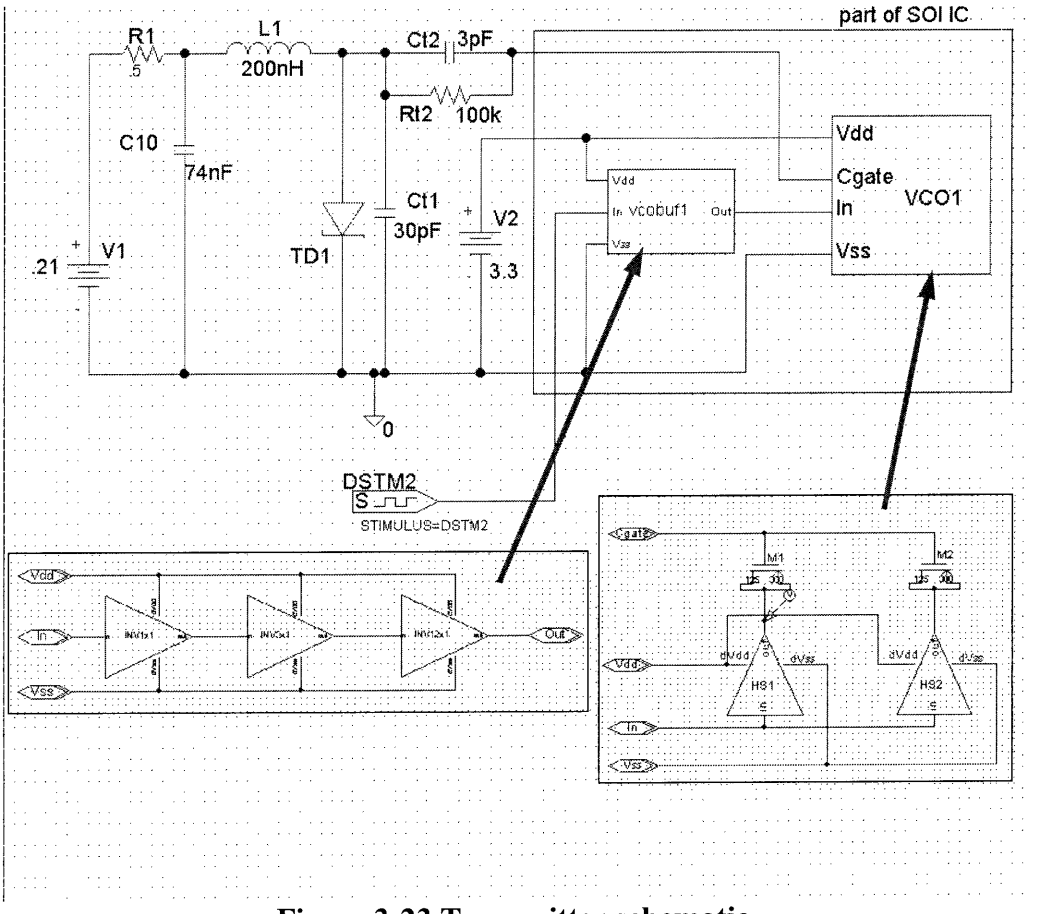


Figure 3-23 Transmitter schematic

The transition time, which is defined by the frequency settling time after data bit switches from 0 to 1 or from 1 to 0, indicates the bandwidth limit. A simulation was done to verify the above circuit. An aperiodic signal was employed in Figure 3-24. Green plot in the top figure is the ideal decimation output from the decimation filter and is buried under the red plot. Meanwhile, Figure 3-23 points out where these plots are from. Due to the size of the PMOS was designed much larger than the NMOS, the amplitude settling time is clearly seen at the falling edge, in which the NMOS dominates the transition time. On the other hand, the amplitude settling time of the rising edge is hardly seen in Figure 3-25. This tells us: to have the same amplitude settle-down time for both the falling and the rising edges, the size of the PMOS and the NMOS should be

comparable. Nevertheless, the settling time of the frequency is more important in this project because the FSK receiver is more dependent on frequency rather than amplitude.

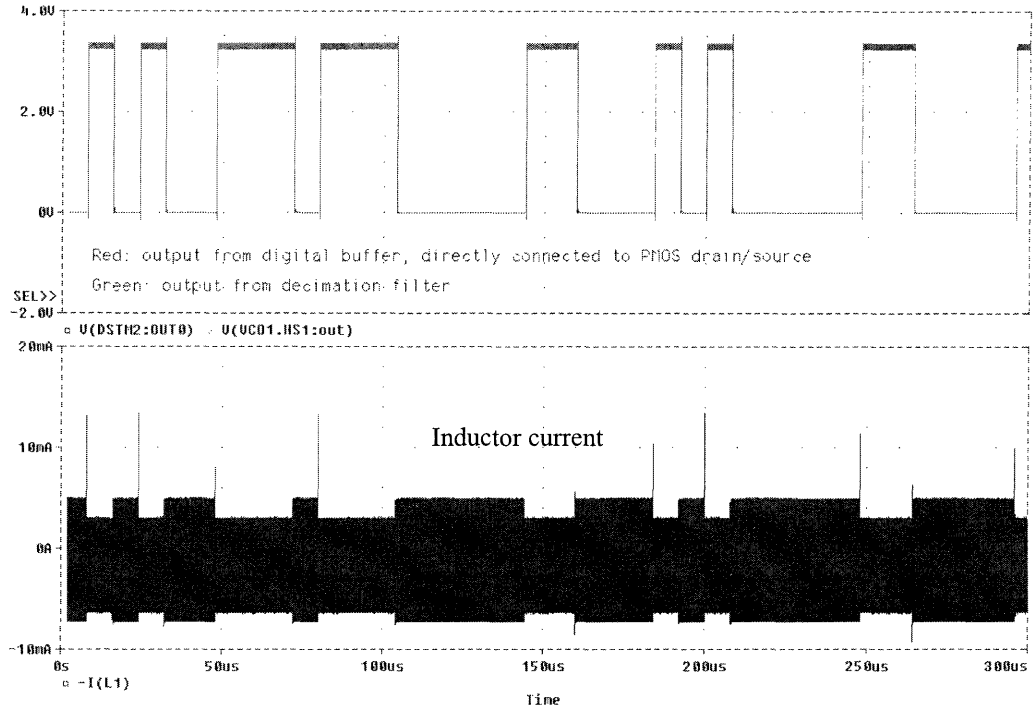


Figure 3-24 Simulation of the transmitter circuit

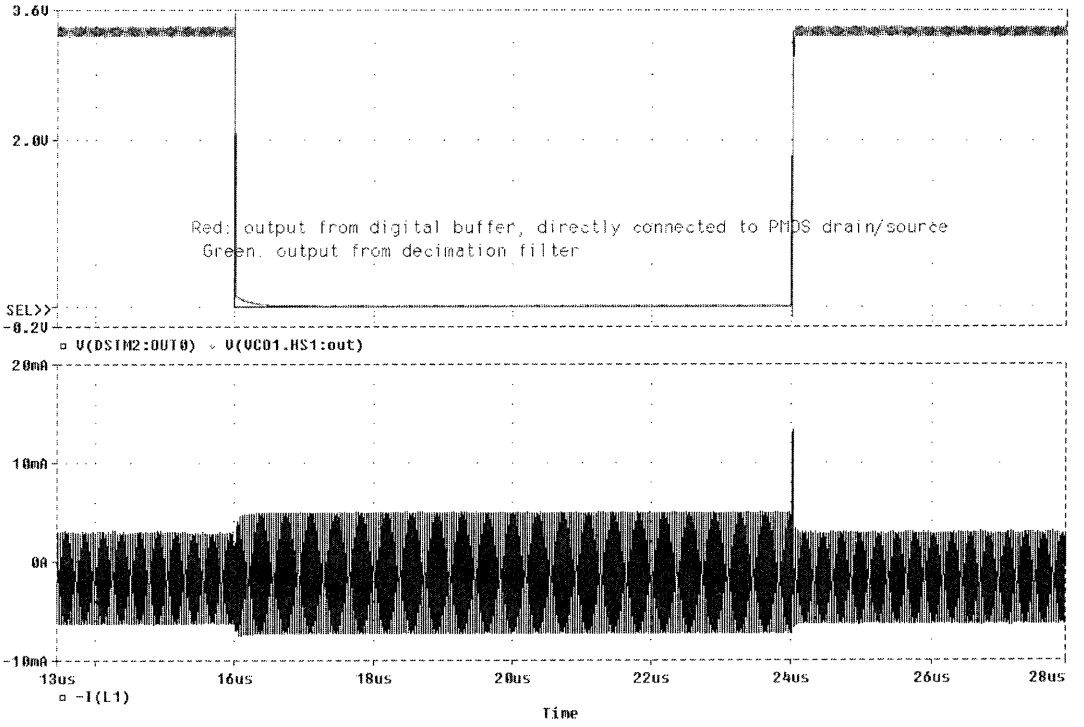


Figure 3-25 Transmitter simulation with expanded time scale

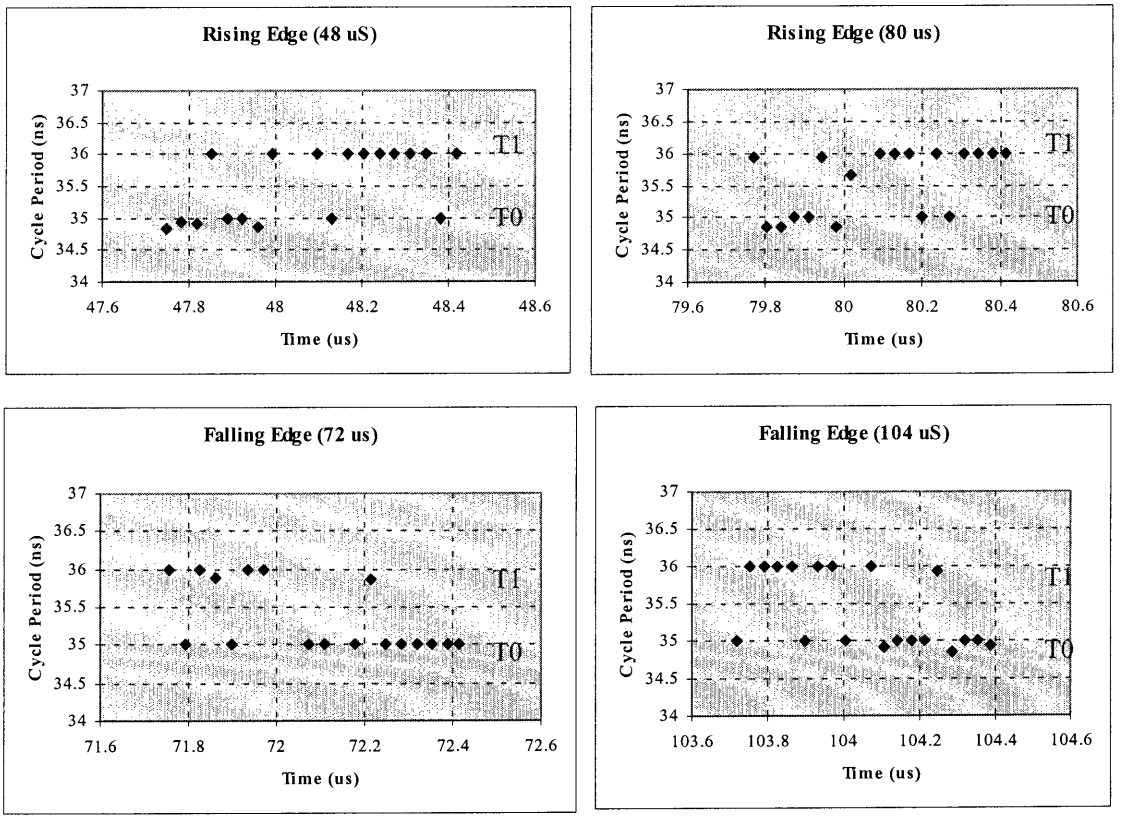


Figure 3-26 Oscillator period before and after the transition in the binary input

The cycle period around the rising and the falling edges at the different time are shown in Figure 3-26. The high-low period is easily seen before and after the transition. During the transition, the period becomes abnormal. The approximate transition time from Figure 3-26 is summarized in Table 3-10. For both cases, the transition time is much less than the 10% of the bit period (8 us). This indicates that the circuit works well with 125 kbps bandwidth. Though the amplitude settling time takes longer at the falling edge (NMOS takes effect), the frequency setting time at the falling edge is comparable to the time at the rising edge, even smaller. Upon the falling edge, the SOI PMOS capacitor plays no role after the transition. Therefore, the inverter NMOS has no or less impact on the frequency settling. While the SOI PMOS capacitor plays a frequency-shift role after the rising edge, its series channel resistance dominates the frequency settling time although the inverter PMOS was designed big to minimize the impact. The existing circuit design is not perfect; however, the size of NMOS is not critical in this project. For the future improvement, the SOI PMOS ought to be designed with the minimum series channel resistance while the inverter PMOS and NMOS should be designed with the comparable size.

Table 3-10 Summary of transition times for rising and falling edges

	Rising (ns)	Falling (ns)
First	74	69
Second	77	69

Figure 3-27 shows the FSK modulation from simulation. The simulation was done supposing the tunnel-diode junction capacitance is 150 pF with the tuning capacitance 15 pF. The frequency spacing is about 500 kHz, four times of the data bit rate. This offers even more robust communication than the two times of the bit rate

mentioned in chapter 2. The wider frequency spacing provides larger error-free region for the receiver. However, the higher bandwidth is required for the receiver.

Two tuning capacitors are added to adjust the center frequency (C_{t1}) and the bandwidth (C_{t2}), shown in Figure 3-23. C_{t1} is in parallel with the tunnel diode. The capacitance C_{td} in (3-23) becomes the sum of C_{td} and C_{t1}. As the sum is much more than the PMOS capacitance, the two FSK frequencies shift while adjusting C_{t1}. When the digital buffer outputs low, the two PMOS are in depletion mode and their capacitances are close to zero. The high frequency is independent of the two PMOS capacitors. When the digital buffer outputs high, the voltage across the drain and gate is above threshold and the two PMOS are in inversion mode and their capacitance decides the low frequency. Therefore,

(3-29)

$$\left(\frac{\omega_0}{\omega_1}\right)^2 \cong 1-2\frac{\Delta\omega}{\omega_c} \equiv 1-\delta ,$$

where ω_0, ω_1, ω_c and $\Delta\omega$ represent the low frequency in radians, the high frequency in radians, the center frequency in radians and the bandwidth in radians, respectively. $\delta << 1$. Another equation is given by

(3-30)

$$\left(\frac{\omega_0}{\omega_1}\right)^2 = \frac{C+C_0}{C+C_1},$$

where C, C0 and C1 represent the sum of Ct1 and Ctd, the capacitance in depletion mode and the capacitance in inversion mode, respectively. Equalizing Eq.(3-29) and Eq. (3-30), the relationship between the bandwidth and C1, C0 is given by

$$\delta = \frac{C_1 - C_0}{C + C_1} \cong \frac{C_1}{C}, \text{ if C} >> \text{C1} \tag{3-31}$$

Ct2 in Figure 3-23 can be used to adjust C1, i.e. adjust to the bandwidth.

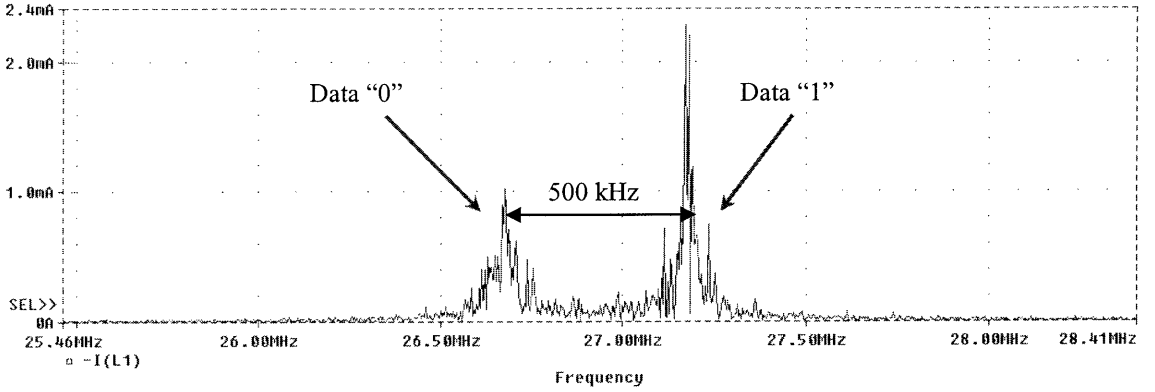


Figure 3-27 Transmitter simulation using aperiodic binary input

As a portion of the wireless communication interface IC, the two parallel SOI PMOS capacitor and the digital buffer were fabricated with the sigma-delta A/D converter and the decimation filter. The chip is 2 mm x 2 mm, which is illustrated in Figure 3-28 (a). A microphotograph of the die will be exhibited in section 3.5.3. The chip has the clear separation of the analog and the digital parts, which can protect the sensitive analog circuits against the disturbance from the "noisy" digital circuit – the decimation filter. For the same purpose, there exist the analog pads and the digital pads. The analog pads are the two analog power supply pads (AVdd, AVss) and the analog input/output pad. The digital pads are the two digital power-supply pads (DVdd, DVss), the digital in and the digital out. The transmitter portion has both the analog part and the digital part. The analog part is the two SOI PMOS capacitor while the digital part is the chain of inverters as the digital buffer. RFgate is the analog in/out, VCOin is the digital

in, and the digital buffer uses the digital pads. All pads have ESD protection. The analog pads have ESD protection connected with AVdd, AVss while the digital pads have ESC connected with DVdd, DVss.

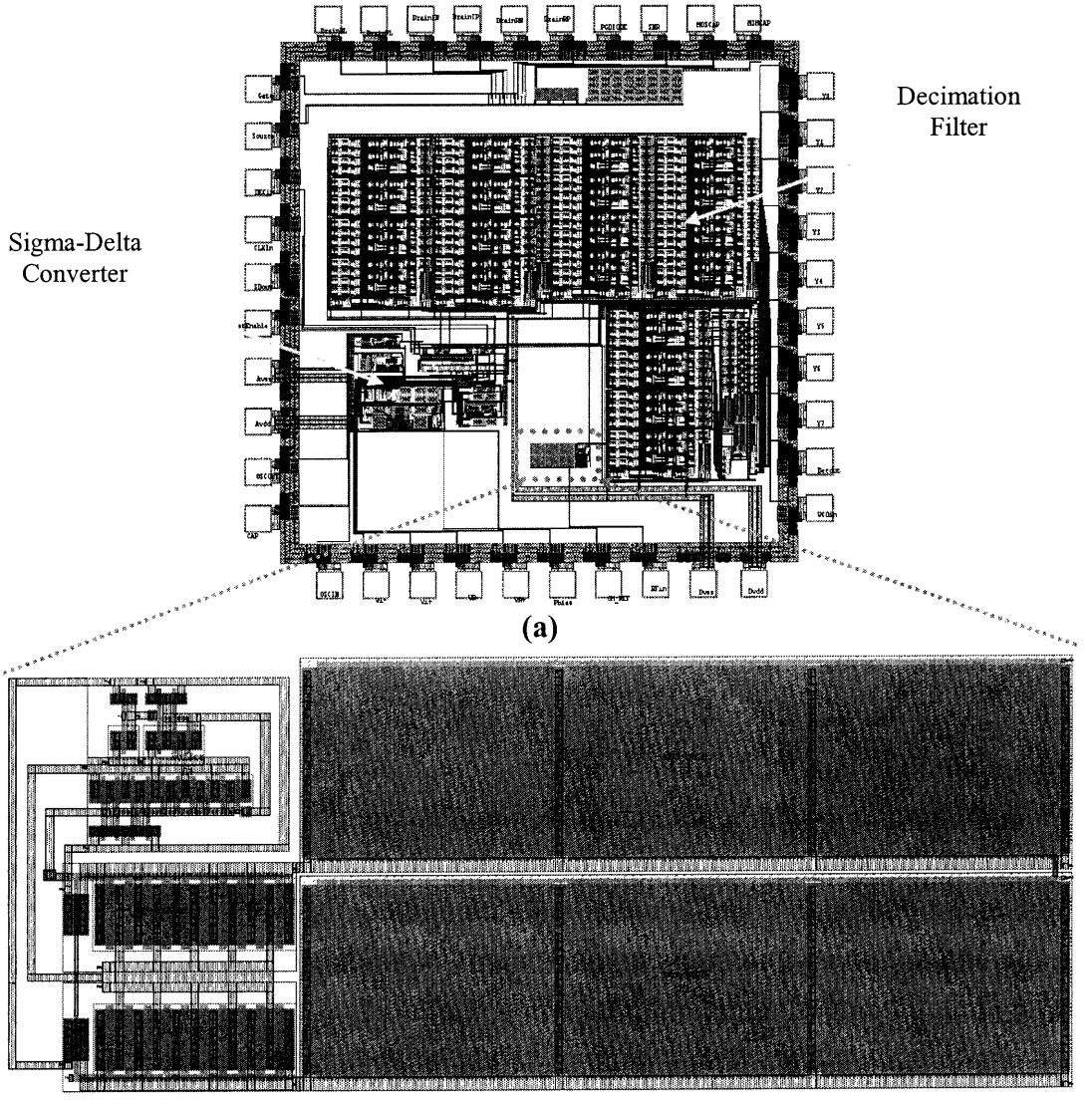


Figure 3-28 (a) CAD layout of the SOI test chip. Die size is 2 mm by 2 mm in the 0.5-µm process (b) The FSK transmitter

3.4 Transmitter PCB Design

A PCB was designed to work with the PN varactor or work with the SOI die, as shown in Figure 3-29. The room-temperature version was manufactured double-sided by ExpressPCB [26], as shown in Figure 3-30. The size is 4.6 cm x 2.5 cm, including 6-pin Molex connector. The laminate is 0.062" FR-4 epoxy glass with ½ ounce copper, the additional ¾ ounce copper is plated [26]. The final finish is tin-lead reflow [26]. The dielectric constant of the FR-4 laminate ranges from 4.2 to 5.0 [26]. The maximum operating temperature can be up to 125 C [26].

Except for the tunnel diode, all discrete components are surface-mountable (SMT 0805). The PCB was designed using two sides. To avoid eddy current, all unused pieces of metal on the two sides were removed. In Figure 3-30, "Bypass" will be used for a bypass capacitor that is shunted with the tunnel-diode biasing voltage. It keeps the supply impedance less than one ohm at the operating frequency. C1 is the tuning capacitor used to tune the transmission frequency. Inside the 2-turn square planar loop antenna/inductor, there are places for the varactor circuit (R2, C2 and VC) and the SOI die. The traces for the antenna/inductor and the ground are 20 mil in width. The other traces are 8 mil in width.

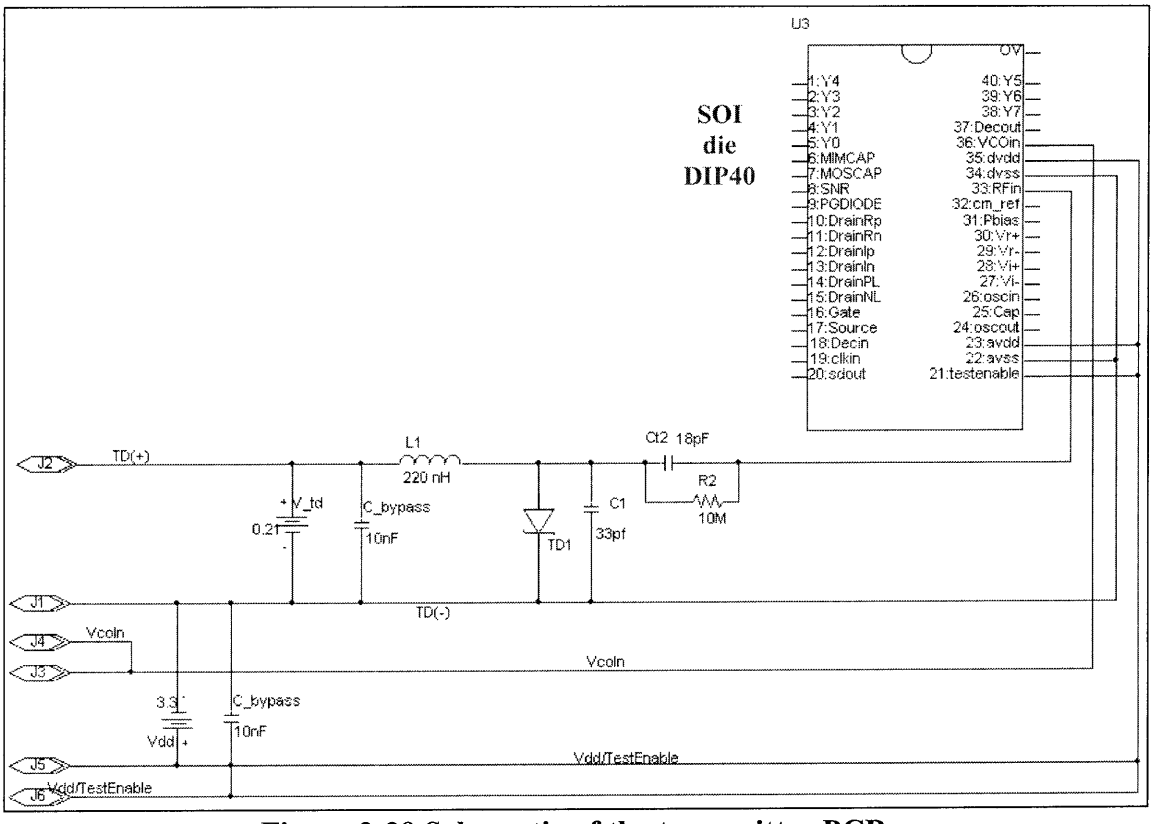


Figure 3-29 Schematic of the transmitter PCB.

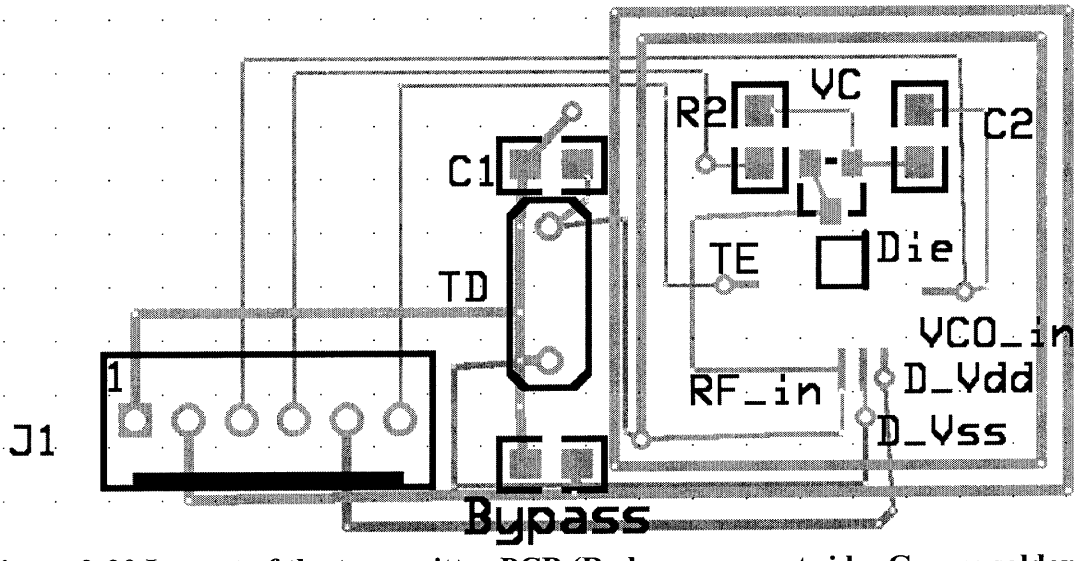


Figure 3-30 Layout of the transmitter PCB (Red: component side; Green: solder side).

3.5 Measured oscillator performance and antenna coupling factor

3.5.1 Tunnel diode measurements

The antenna inductance and the tunnel diode characteristics were first measured. The purpose is to fully understand the devices, verify the design and minimize the uncertainty in the project. The measurements consist of an I-V curve for the diode, its junction capacitance, and the antenna inductance.

The tunnel diodes were measured using an Agilent semiconductor analyzer and test fixture. The measured I-V curve is shown in Figure 3-31. Compared to Figure 3-18, the peak current is very close while the simulation model has a little higher voltage at the peak current. The valley current is about 0.65 mA, the ratio of Ip and Iv is more than 3, which is larger than the specification, shown in Table 3-3. The difference should not have a bad impact on oscillation because it increases the negative-slope region. Meanwhile, the bias current is lower than expected, so the power is less.

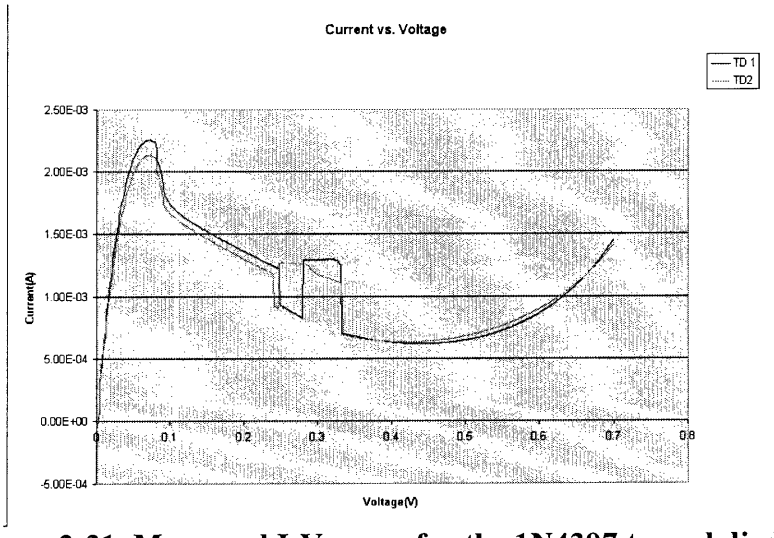


Figure 3-31 Measured I-V curve for the 1N4397 tunnel diode.

The junction capacitance, C_{td}, is another important parameter of the tunnel diode. Since this value is much higher than for the PMOS capacitor (the maximum can be up to 200 pF), it dominates the oscillation frequency.

The schematic of the test circuit used to measure the tunnel diode junction capacitance C_{td} is shown in Figure 3-32. The 10-nF bypass capacitance ensures that the low impedance from the biasing source V1. C1 is a tuning capacitor with a known value. By adjusting the value of the tuning capacitor, the oscillation frequency can be shifted. Six different values of capacitors were used in this measurement. A simple one-turn loop antenna placed at a very close distance was used to detect the signal recorded using an Agilent 4395A spectrum analyzer. A 10:1 oscilloscope probe was used to measure the voltage across tunnel diode.

The waveform oscillated around a bias point, 0.21V, as shown in Figure 3-33. The peak-to-peak voltage is 350 mV. The simulated peak-to-peak voltage is 200 mV.

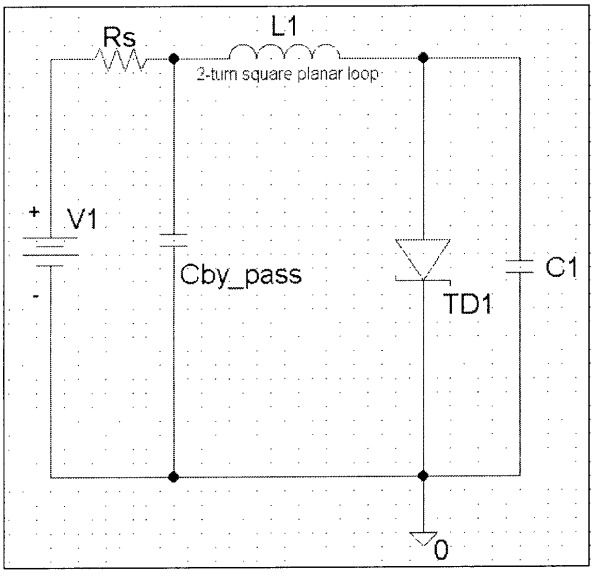


Figure 3-32 Schematic of the circuit used to measure the tunnel diode junction capacitance C_{td} and loop antenna inductance.

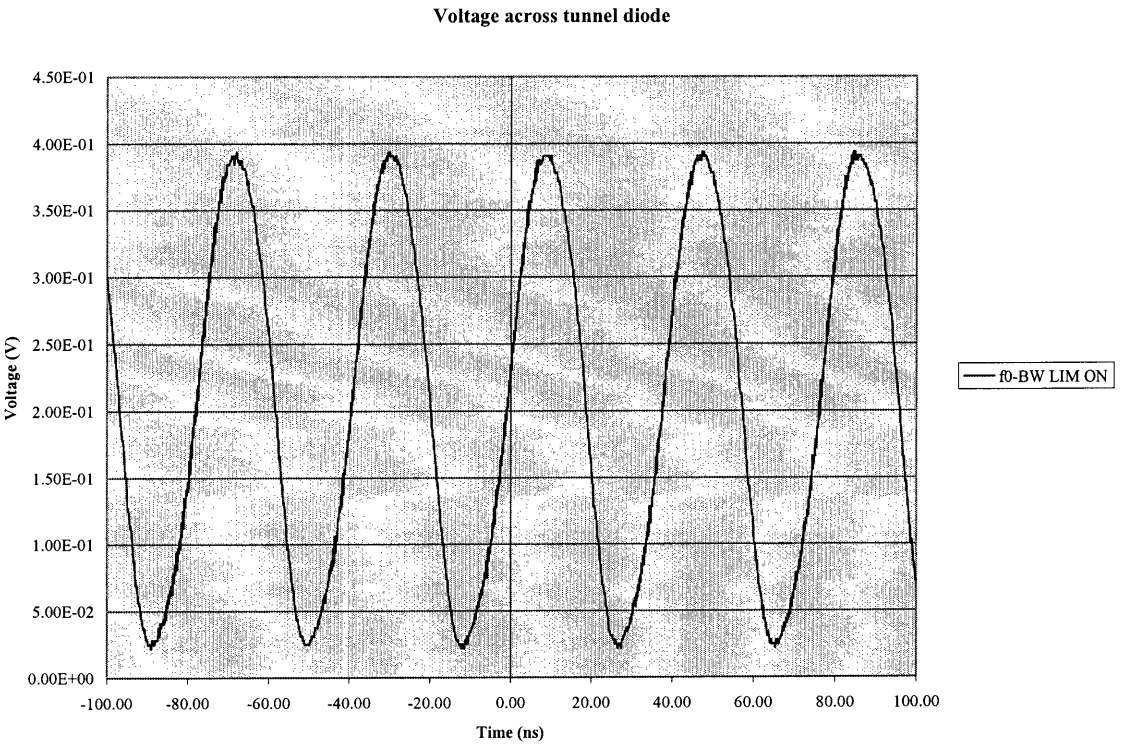


Figure 3-33 The waveform across the tunnel diode, probed by HP54615B oscilloscope.

The measurement is used to determine the frequency, not the power. The distance is not critical in this test. The oscillation frequency can be calculated using

(3-32)

$$L_1 C_x = \frac{1}{\omega_x^2},$$

where C_x is the sum of C_{td} and C_1. C_x and $\frac{1}{\omega_x^2}$ have a linear relationship. The least squares fitting method was used to fit a line to the measured data, which is given in Table 3-11.

As shown in Figure 3-34, the measured curve and the fitting line are well matched, which validate the model. The inductance of the two-turn 2-cm square planar

loop antenna is the slope of the fitting line. The Y-intercept is the product of the inductance and the tunnel diode's junction capacitance C_{td}. The results are summarized in Table 3-12.

Table 3-11 Measurd oscillator data with varying C_1

C1 (pF)	f_x (MHz)	$1/\omega^2$	Best-fit Calculation
0	41.4	1.48e-17	1.48e-17
10	38.6	1.70e-17	1.70e-17
18	36.7	1.88e-17	1.88e-17
27	35.0	2.08e-17	2.08e-17
36	33.4	2.28e-17	2.27e-17
56	30.7	2.70e-17	2.72e-17
100	26.2	3.70e-17	3.69e-17

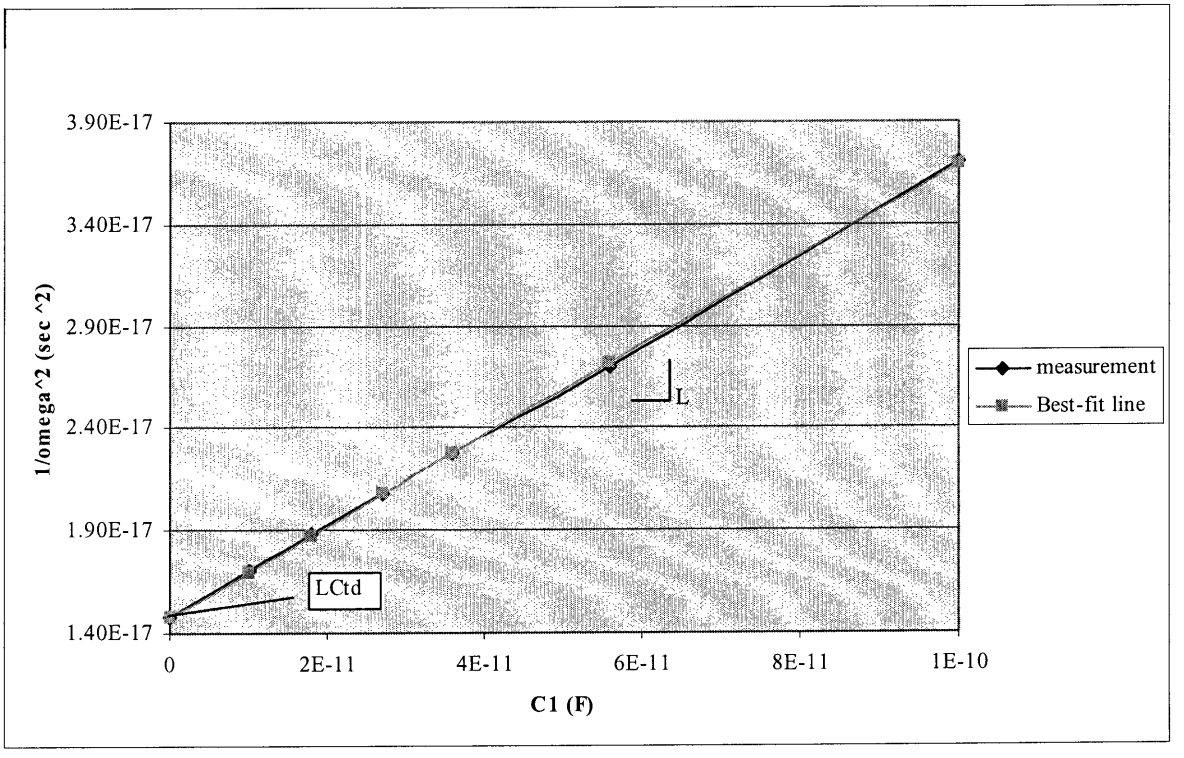


Figure 3-34 Best-fit line and the measured curve with different capacitances

Table 3-12 Extracted values of L_1, C_{td}

L_1	218 nH
C_{td}	68.3 pF

From the test, the approximation values presented in Table 3-2 are close to the measurement, especially the equation from [9]. The tunnel diode capacitance is even smaller than the half of its maximum value, which indicates that the oscillation frequency will shift up without the tuning capacitor. The tuning capacitor is inevitable anyway. Our final circuit design in Figure 3-23 will work well with the tunnel diode. Figure 3-35 shows the setup corresponding to Figure 3-32.

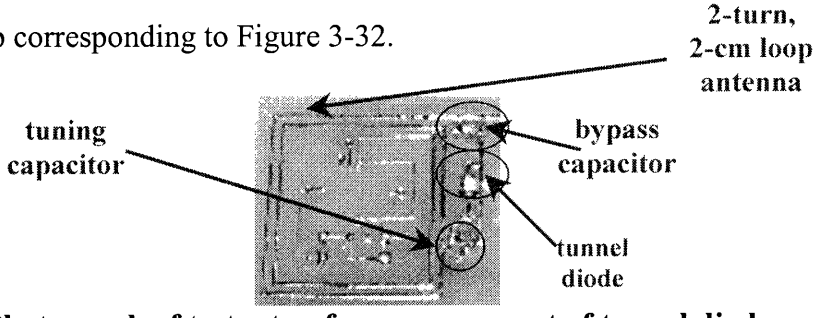


Figure 3-35 Photograph of test setup for measurement of tunnel diode capacitance and loop antenna inductance

3.5.2 Transmitter measurements using PN varactor

This measurement verifies the concept of FSK modulation. A Zetex varactor ZC933 was used to modulate the carrier frequency based on the oscillator design in Figure 3-32 and the PCB design in Figure 3-30. As shown in Figure 3-36, the varactor is reverse-biased.

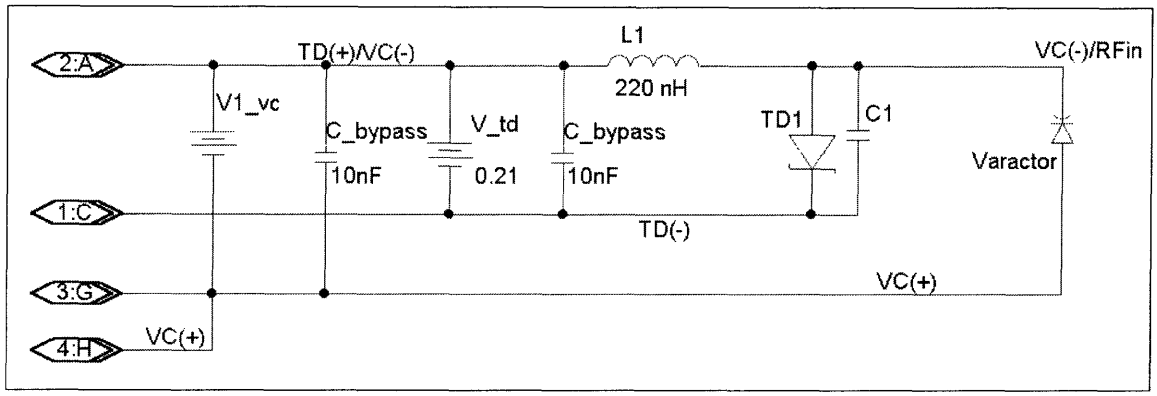


Figure 3-36 Schematic of the transmitter using pn varactor.

The bit rate 125 kbps and FSK modulation determine that the frequency spacing should be at least two times bit rate, i.e. >= 250 kbps. The relationship between the frequency change (*df*) and capacitance change (*dc*) are given by

$$\frac{df}{dc} = \left(\frac{1}{2\pi\sqrt{LC}}\right)' = \left(-\tfrac{1}{2}\right)\frac{1}{2\pi\sqrt{LC}}C^{-1} = -\frac{f}{2C} \tag{3-33}$$

where f is the oscillation frequency, 27 MHz, L is 200 nH and C is the total capacitance, 174 pF. *df/dc* is about –78 kHz/pF, i.e., for 3 pF capacitance increment, the oscillation frequency shifts down by 250 kHz.

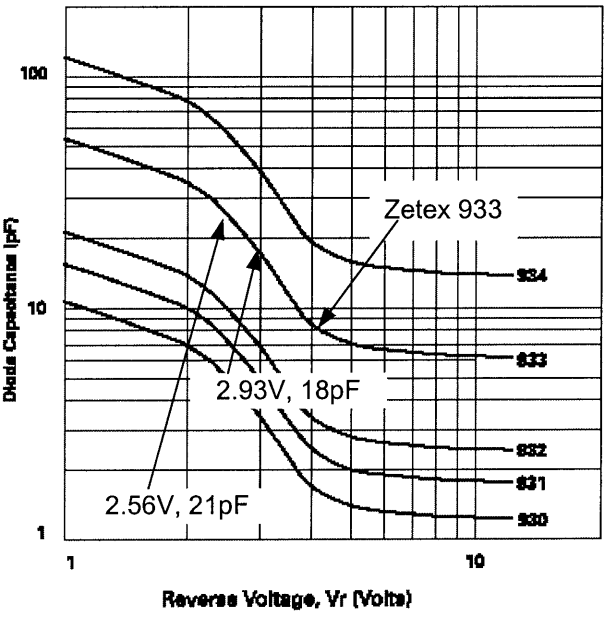


Figure 3-37 Zetex ZC933 C-V curve from [33].

As shown in Figure 3-37, the capacitance is 21 pF when the varactor is reversely biased at 2.56V, 3 pF lower when V_r = 2.93 V. By applying these voltages into the transmitter in Figure 3-36, the two frequencies should have 250-kHz spacing. The measurement in Figure 3-38 shows 255-kHz frequency spacing when V_r = 2.56 V and V_r = 2.92 V, which is very close to the estimated. If the varactor were used as FSK modulator, a voltage converter would be required. It will convert the digital data to the proper reverse voltage for frequency modulation. Figure 3-39 shows the measured voltage across the inductor using HP54615B oscilloscope.

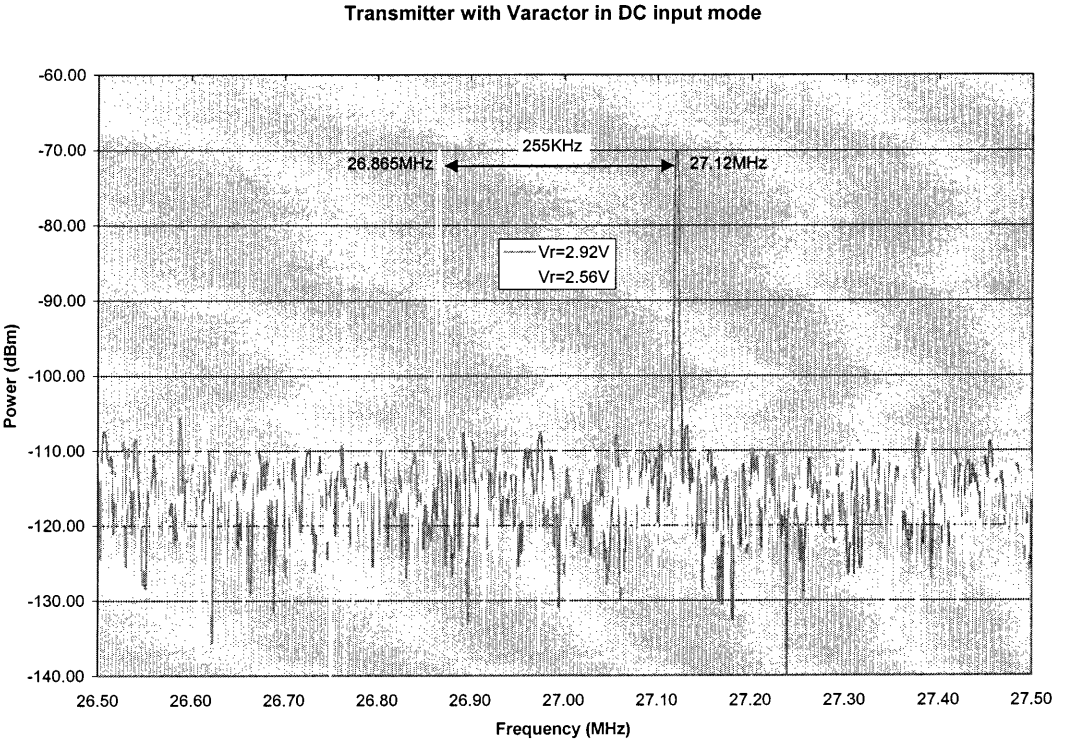


Figure 3-38 Measured frequency spacing in FSK transmitter with varactor.

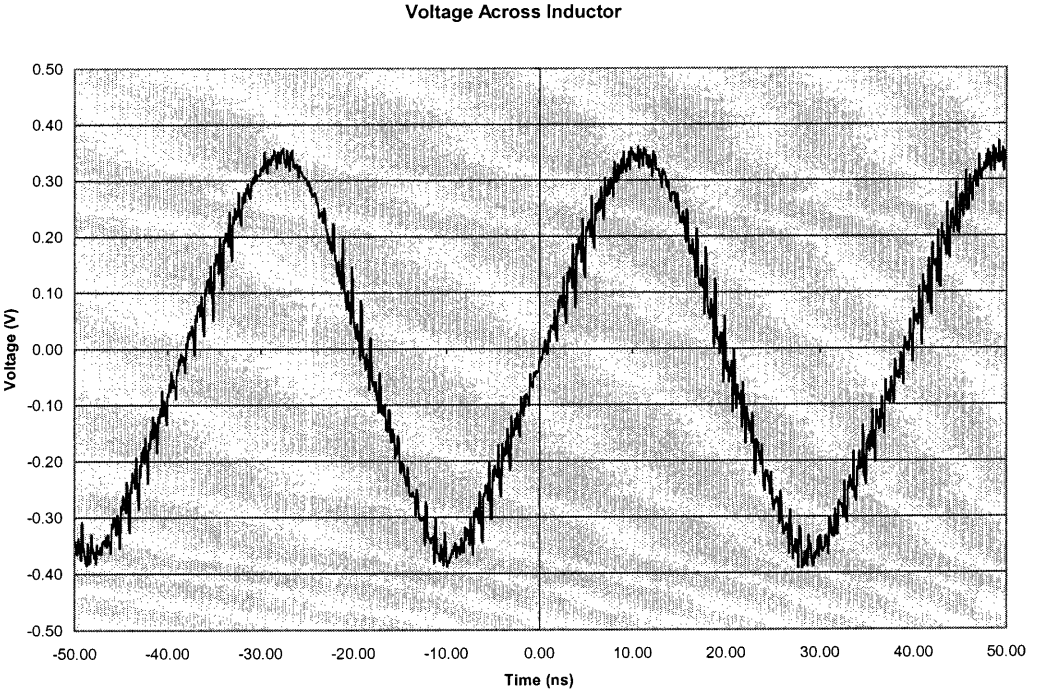


Figure 3-39 Measured voltage across the inductor in the FSK transmitter with pn varactor.

3.5.3 Transmitter measurements using SOI PMOS capacitor

The main goal in this work is to explore the feasibility of FSK transmitter using an SOI PMOS varactor, which can be used in a high-temperature environment. Previous measurements demonstrate that the PCB in Figure 3-30 works well with a tunnel diode oscillator and FSK transmitter using pn varactor. The same PCB is reconfigured for FSK transmitter with SOI PMOS varactor. The goal is that the two modulated frequencies should be separated about 250 kHz by applying the different digital output levels to the buffer.

An extra PMOS (W/L=120μm / 50μm) transistor on the SOI die was designed for these tests. Its size is the same as the size of PMOS varactor used in FSK transmitter. A C-V measurement was done to verify its actual characteristics. Figure 3-40 shows the measurement result at 500 kHz using a Keithley 590 C-V meter and 4200 semiconductor analyzer. The measurement shows good agreement with the simulation, shown in Figure 3-41. It also demonstrates that the SOI PMOS transistor can be used as a varactor, i.e. the capacitance changes when the gate-source voltage changes.

Because of channel resistance, the capacitance will decrease as frequency increases. Figure 3-42 shows that capacitance is about 20 pF below 1 MHz, decreases to 3.74 pF at 27 MHz. With two parallel PMOS transistors on the chip, the total capacitance is 7.5 pF at 27 MHz, which can provide a 580-kHz frequency spacing.

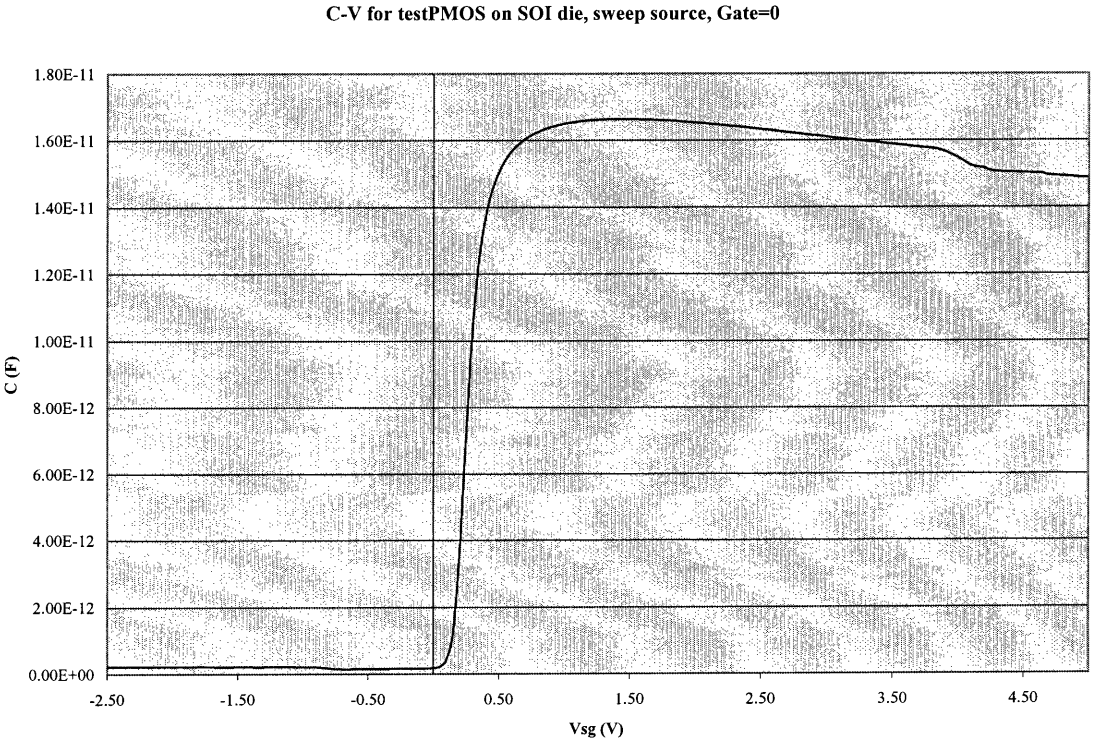


Figure 3-40 C-V measurement for the test PMOS transistor (120µm/50µm) on the SOI die.

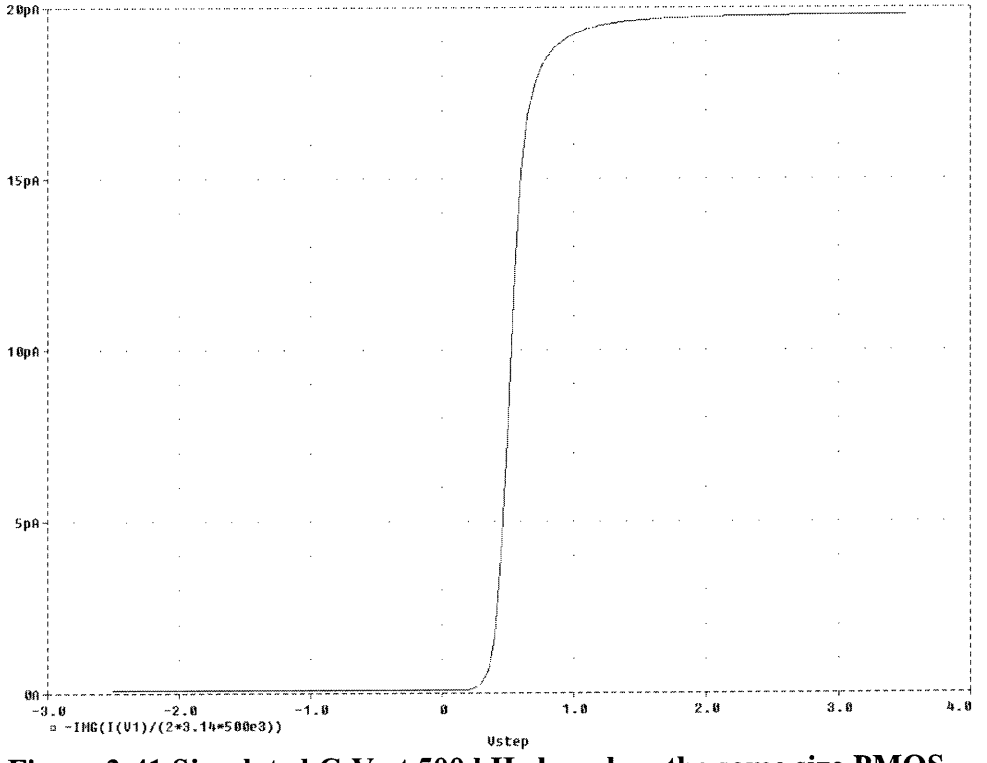


Figure 3-41 Simulated C-V at 500 kHz based on the same size PMOS.

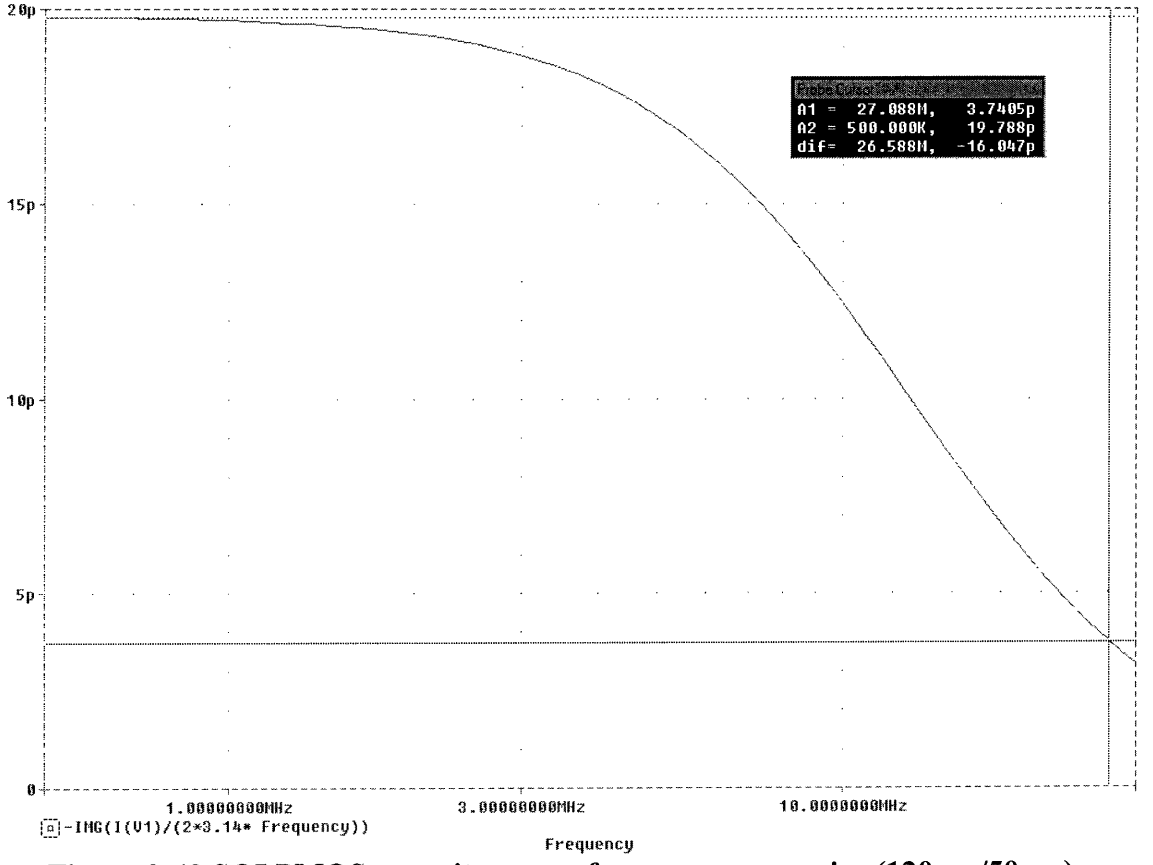


Figure 3-42 SOI PMOS capacitance vs. frequency, same size (120μm/50μm).

Figure 3-29 shows the PCB connections for the FSK transmitter, which is implemented using an SOI PMOS varactor. An SOI die, shown in Figure 3-28, was packaged in a ceramic package by MOSIS. The package is a standard DIP40. As in the FSK transmitter using a Si pn varactor, by-pass capacitors were added to ensure a low impedance from bias and power supplies. The tuning capacitor, C_{t1}, is used to tune the high frequency.

The SOI PMOS varactor is used to provide the capacitance difference, as discussed in section 3.5.2. As compared to the pn varactor, the SOI PMOS varactor provides only two values. When the source-gate voltage is lower than its threshold voltage, the capacitance is very small and the oscillation frequency depends mainly on

the tunnel diode junction capacitance and the tuning capacitor. By adding another tuning capacitor, C_{t2}, the frequency spacing can be tuned to less than 580 kHz. R_2 provides the bias for the gate of the PMOS varactor. The test setup is presented in Figure 3-43.

Because the gate of the SOI PMOS uses an analog pad whose ESD protection is guarded by the analog supply voltages, AVdd and AVss were connected to DVdd and DVss, respectively. In addition, the TestEnable control input is used to separate different modules on the chip. For the transmitter measurement alone, TestEnable was connected to DVdd. The grounding must be done carefully. Twisted pairs of wires or co-axial cables were used so that the current flows from the positive supply terminal, through the circuit, and returns to the negative supply terminal. Earth ground was connected at one point, only.

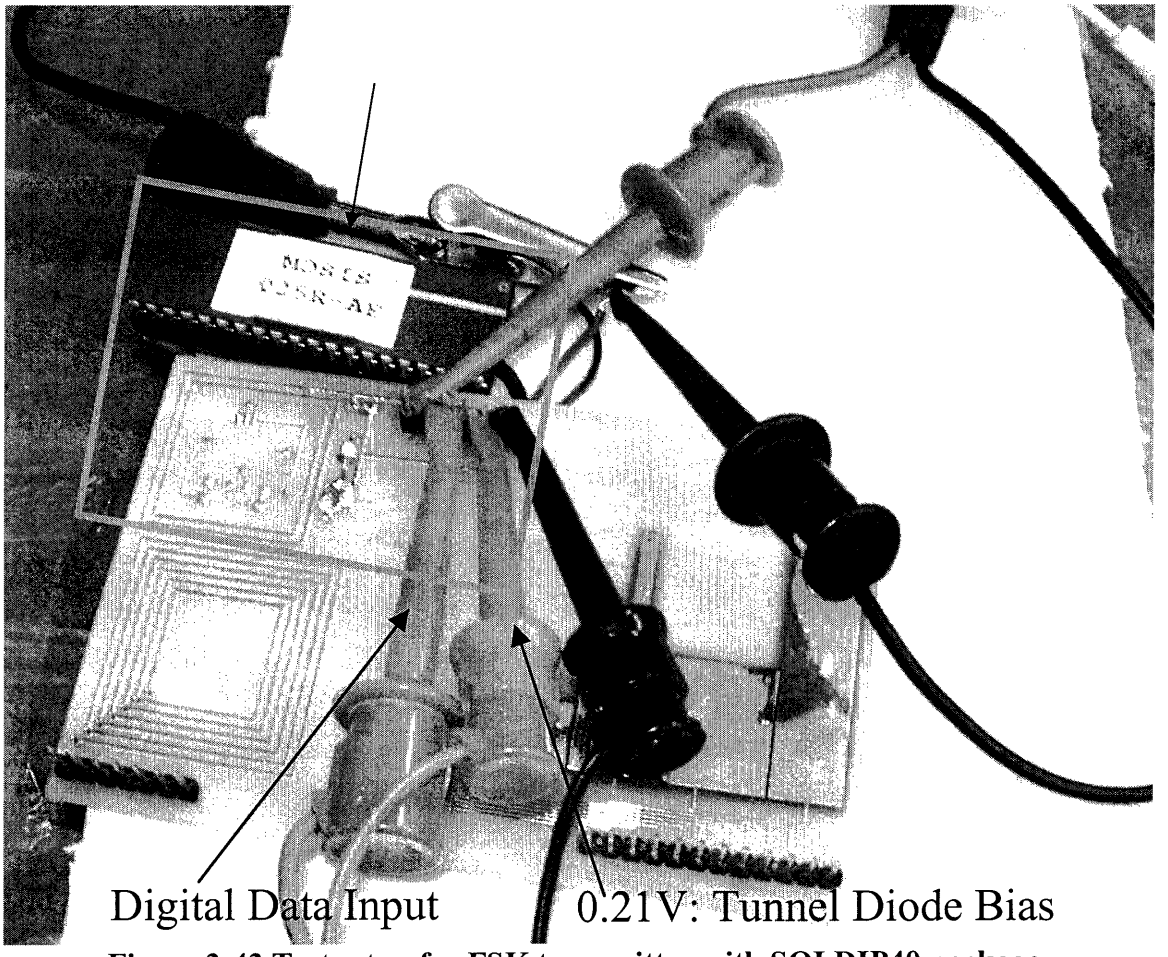


Figure 3-43 Test setup for FSK transmitter with SOI DIP40 package.

The circuit was first tuned to a frequency above 27 MHz by applying a low voltage, Vss, to the digital data input. Figure 3-44 presents three measurements for each value of the digital input and the modulated frequencies are stable. With C_{t2} = 18 pF, the frequency spacing is 230 kHz. In analysis, an effective 7.5 pF from the PMOS varactor is in series with C_{t2}, so the total capacitance is about 5.3 pF and we expect a 410-kHz frequency spacing.

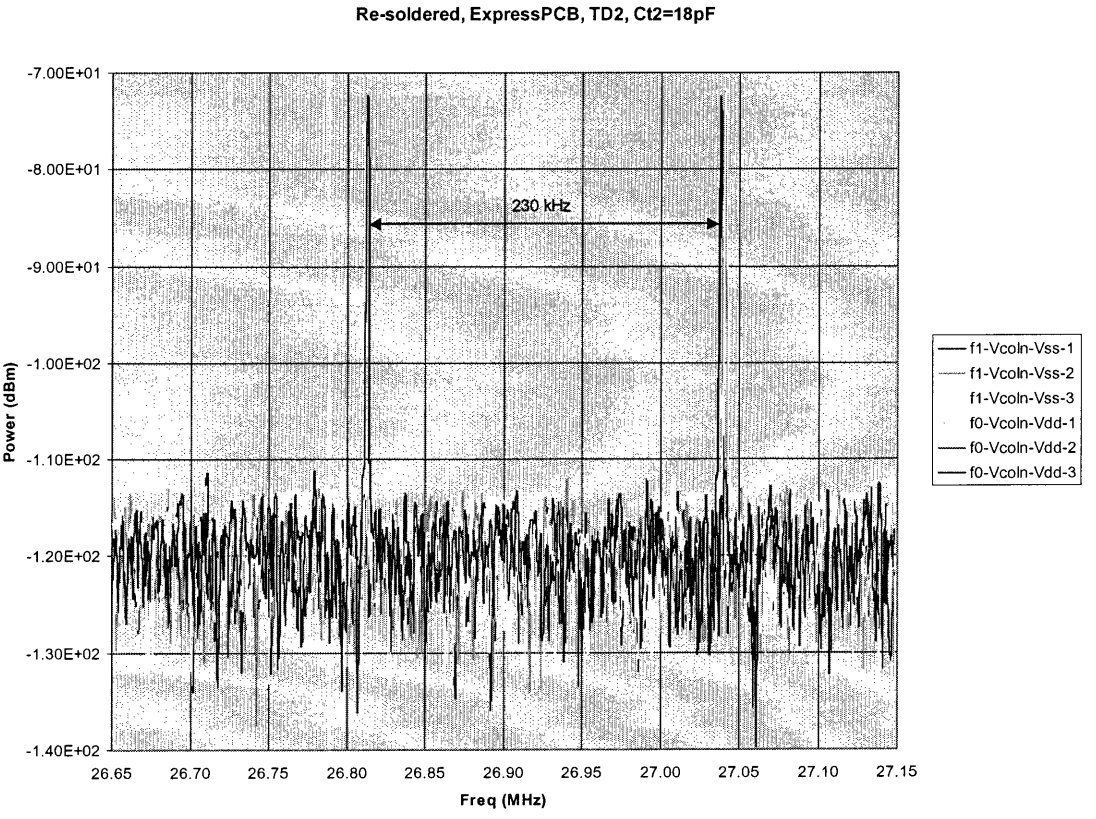


Figure 3-44 Two modulated frequencies using FSK transmitter with an SOI PMOS varactor.

The maximum frequency from the decimation filter is 62.5 kHz. A 3.3-V peak-to-peak, 62.5-kHz sine wave voltage signal was applied to the digital buffer in order to test the modulation capability. Due to the amplification of the four-stage non-inverting buffer, the waveform output from the buffer is square. Figure 3-45 clearly shows the 62.5-kHz modulation.

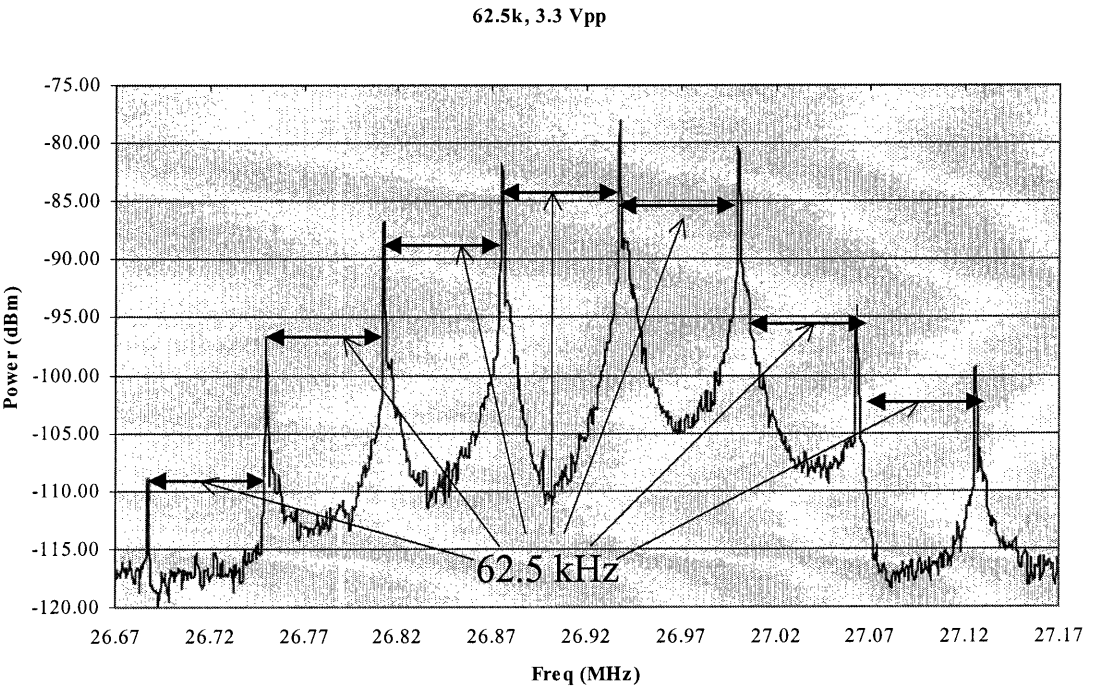


Figure 3-45 Modulation with a 62.5-kHz, 3.3-V peak-to-peak input.

The coupling coefficient k was measured using another 2-turn, 2-cm square loop antenna. The setup is shown in Figure 3-46. The planar inductors were laid flat on a non-conducting surface, and moved horizontally. The data were collected using an Agilent 4395A spectrum analyzer. Converting these data to the induced voltage, the coupling factor can be calculated as shown in Table 3-13. The measurement was done for both f1 and f0, as shown in Figure 3-47.

The coupling factor is expected to vary as distance to the power N, and this model was used to perform a least-square fit to the data. This model provides a good fit, and the coupling factor at a 1-meter distance is extrapolated to be about 8.9×10^{-7}. This value is close to the expected value used in design of the receiver pre-amplifier. The extrapolated N is –2.17.

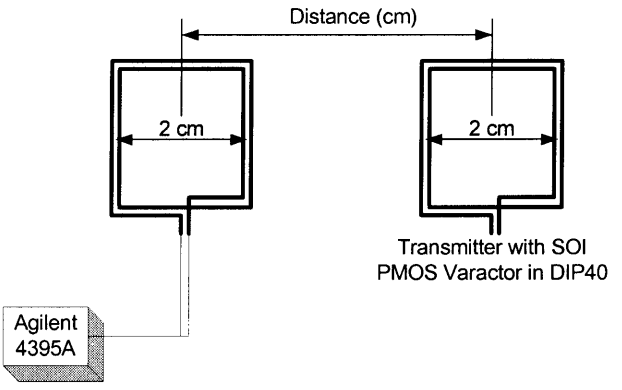


Figure 3-46 Diagram of the coupling-factor test setup.

Table 3-13 Coupling factor at different distance

	Distance (cm)	Measured Power @ 4395A (dBm)	Induced Voltage (μV, rms)	Calculated k
Equation			$10^{\frac{power(dBm)}{10}} \cdot R \cdot 1mW$	$\frac{v_2}{v_1}\sqrt{\frac{L_1}{L_2}}$
f1	5	-71.4	60.0	2.6×10^{-4}
	10	-77.9	28.5	1.2×10^{-4}
	20	-90.5	6.7	2.9×10^{-5}
	30	-98.4	2.7	1.2×10^{-5}
	40	-107	1.0	6.5×10^{-6}
f0	5	-72.0	56.2	2.6×10^{-4}
	10	-77.9	28.5	1.3×10^{-4}
	20	-90.5	6.7	3.0×10^{-5}
	30	-99.3	2.4	1.1×10^{-5}

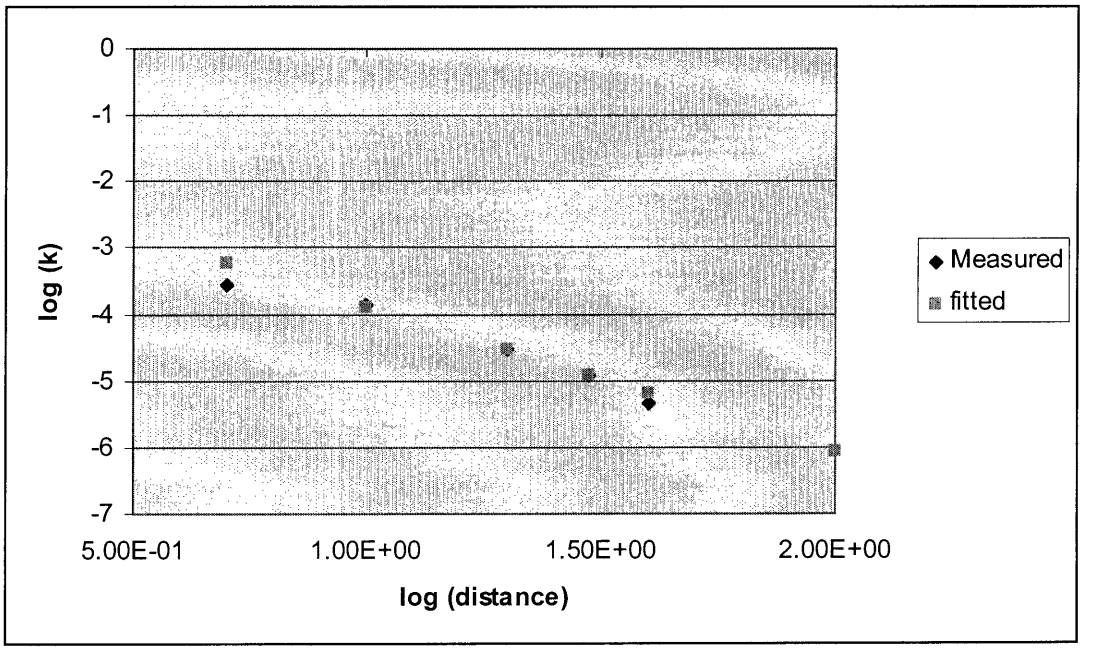


Figure 3-47 Calculated coupling factor based on measurement and their fitted line for two modulated frequencies

Referring to the amplitude modulation in Figure 3-25, another measurement was done to check voltage amplitude across tunnel diode for the two modulated frequencies. The voltage was measured for both modulated frequencies, and the amplitude is same.

4 Receiver Pre-Amplifier with Optimized SNR

4.1 Introduction

As shown in Figure 4-1, a simple BFSK receiver consists of a pre-amplifier, two band-pass filters which pass one frequency and filter out the other frequency, two envelope detectors which convert the AC signal to DC signal, and a comparator which compares the output from the two envelope detectors and retrieved the binary signal.

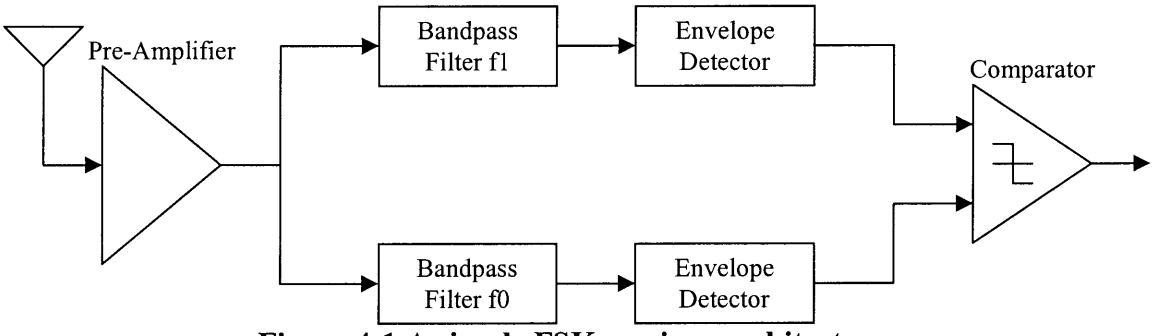


Figure 4-1 A simple FSK receiver architecture.

Commercial ICs are available on market for receiving 27 MHz signal. In exploration, all these ICs, including receiver, transceiver and IF receiver either could not receiver the signal at μV level or do not have the bandwidth up to 400 kHz. This thesis includes a pre-amplifier design, shown in Figure 4-2, which collects the signal from the antenna and amplifies it to a required level to drive an oscilloscope, spectrum analyzer or FSK demodulator.

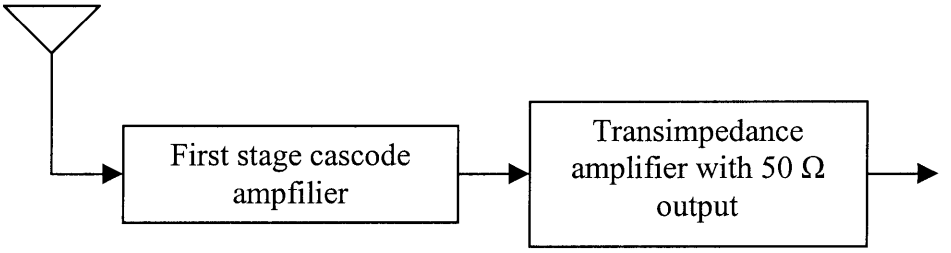


Figure 4-2 Block diagram of pre-amplifier.

4.2 Coupling Theory

As discussed in Chapter 3, the wireless transmitter uses a 2-turn, 2-cm square loop antenna and the carrier frequency is 27 MHz. The transmitter and receiver antennas operate in the near field and function as coupled inductors.

In the previous work [11], the coupling co-efficient had been studied between two coils with different dimensions and distance, aligned or misaligned. Experiments did not closely match theoretical analysis, probably due to measurement parasitics, so this work is based on the theoretical result. The GMI project targets a 1-meter distance and the coupling coefficient is about 10^{-6} [30][11]. A lumped model for the wireless link is shown in Figure 4-3.

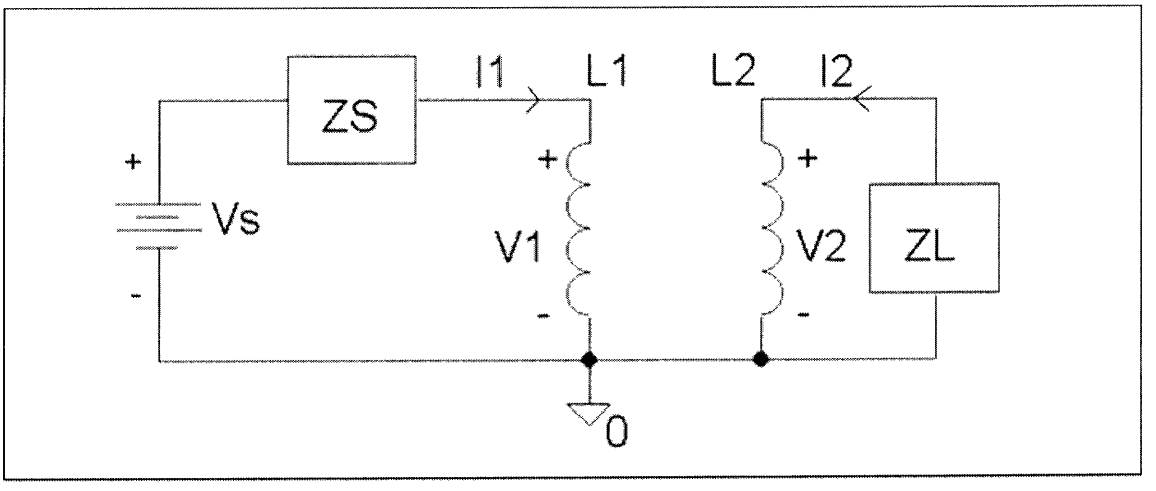


Figure 4-3 Block diagram of mutual inductance.

Referring to Figure 4-3, the voltage equations for the primary and secondary circuits are given by

$$\begin{cases} V_1 = j\omega L_1 I_1 + j\omega M I_2 \\ V_2 = j\omega M I_1 + j\omega L_2 I_2 \end{cases}, \tag{4-1}$$

where the mutual inductance $M = k\sqrt{L_1 L_2}$, and k is the coupling coefficient.

Using KVL in the secondary circuit, we have

$$V_2 = -Z_L I_2 \tag{4-2}$$

By inserting Eq. (4-2) into Eq. (4-1), the impedance Z_1 looking from L_1 in the primary circuit is found to be

$$Z_1 = \frac{V_1}{I_1} = j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + Z_L} = j\omega L_1 + \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + Z_L} \tag{4-3}$$

With k near 10^{-6}, k^2 makes the second term negligible, so

$$Z_1 \cong j\omega L_1 \tag{4-4}$$

This indicates that the receiver does not affect the impedance seen by the transmitter, for the range of k under consideration. This approximation is used later in this chapter when analyzing transmitter behavior.

4.3 Antenna Model

A commercial antenna is preferred for the receiver because reliable quality, high sensitivity are required and other requirements are related (miniaturization and temperature). Thus, the TriCOME integrated miniaturized antenna for 27-MHz wireless RF applications signal, TCA51B, was selected [31]. Its 400-KHz bandwidth is

acceptable for our project. It has been typically used in applications such as wireless keyboard and mouse, hand-free earphone, RF toys and remote control units.

To completely optimize the GMI system characteristics, an antenna model is required. Since this information is not provided by the manufacturer, a model was derived by measurement of its characteristics. Two test setups were used. The first setup used the Agilent 4395A Network/Spectrum/Impedance Analyzer as shown in Figure 4-4. The center lead of the antenna was driven by the analyzer, and the outer lead was connected to its measured input.

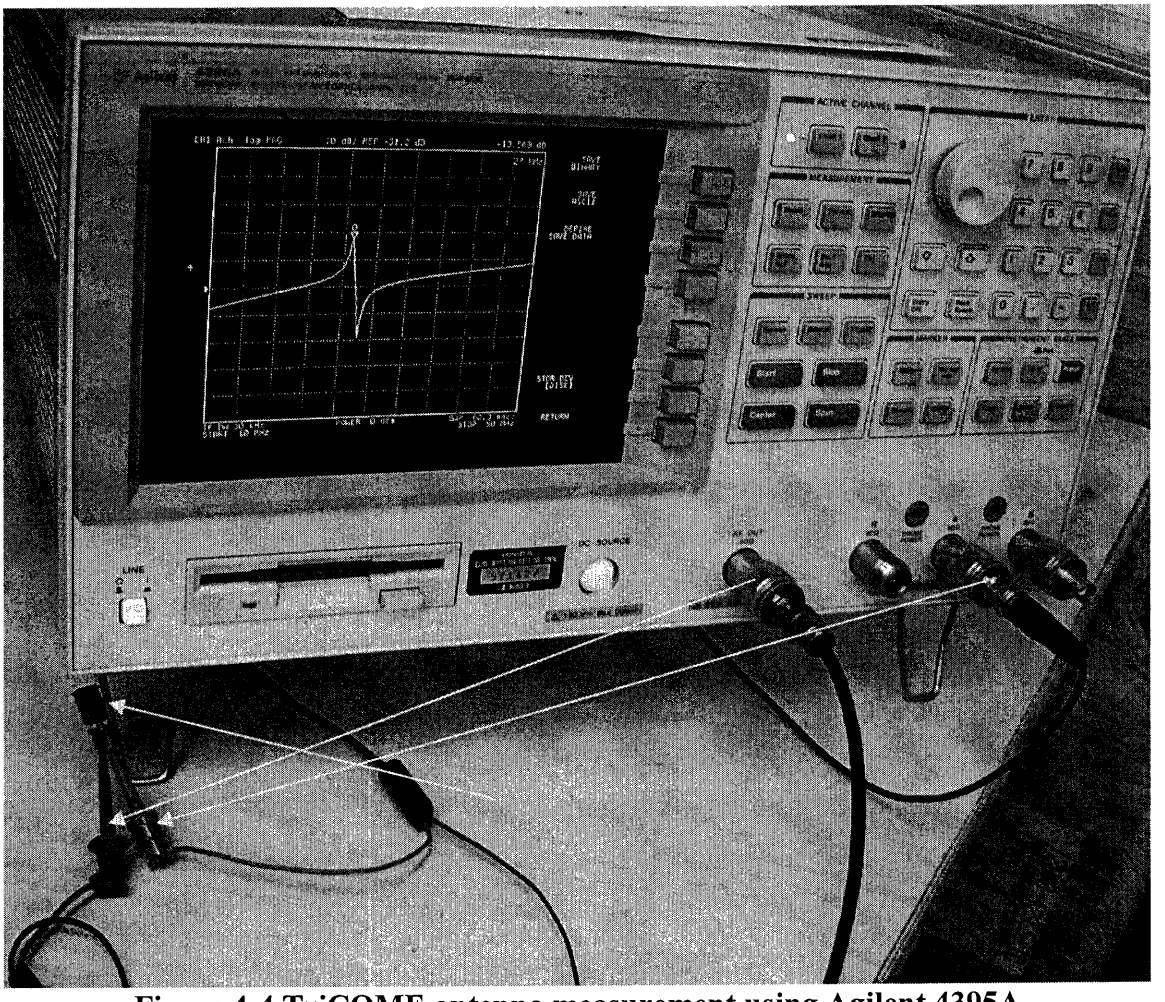


Figure 4-4 TriCOME antenna measurement using Agilent 4395A

The connection is modeled as shown in Figure 4-4. Assuming that the impedance of antenna is Z_{ant}, the voltage at port A is given by

(4-5)

$$V_A = \frac{R_2}{R_1 + Z_{ant} + R_2} V_1$$

R1 and R2 are 50 Ω. V1 is the voltage source provided by RF OUT; V_A is the voltage measured at port A. The RF output power is set to 0 dBm. When RF OUT is connected directly to port A, the measured RF power is 0 dBm, nearly constant over frequency up to 50 MHz, i.e. the analyzer output is $2V_A$.

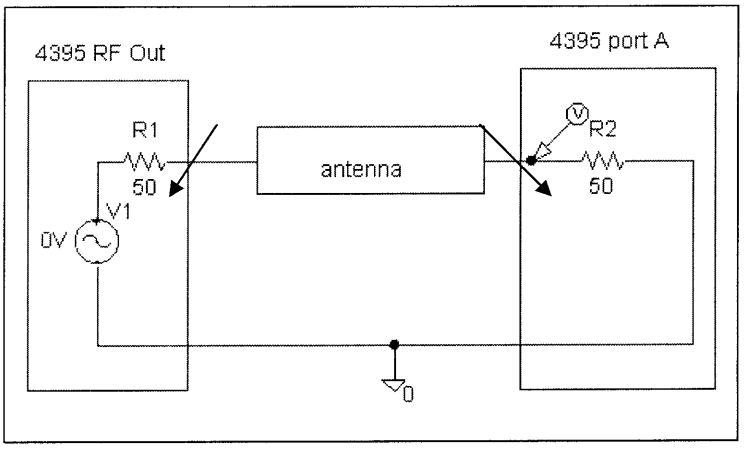


Figure 4-4 The simplified setup for antenna measurement using Agilent 4395A

As shown in Figure 4-5, the antenna impedance is capacitive at low frequency ($Z_{ant} \approx \frac{1}{j\omega C}$), and has 2 resonant peaks near 30 MHz. The antenna was tuned to 27 MHz by moving the antenna near to the grounded chassis of the instrument. Away from the resonant peak, the magnitude of V_A can be approximated by

(4-6)

$$2|V_A| = 2\left|\frac{R_2/Z_{ant}}{2R_2/Z_{ant}+1}\right||V_1| \cong 2\left|\frac{R_2}{Z_{ant}}\right||V_1| = 2\omega R_2 C|V_1|, \text{ if } R_2/Z_{ant} << 1$$

Since the magnitude increases proportional to frequency below resonance, the antenna appears to have a series capacitor. Using any point well below resonance in Figure 4-5, the series capacitance can be calculated using

(4-7)

$$C_s = \tfrac{1}{2}10^{\frac{A(dB)}{20}}\frac{1}{R_2\omega},$$

where A(dB) is the measurement reported by the analyzer. At 8.75 MHz, the measured signal is about –40 dB, so C_s = 1.82 pF.

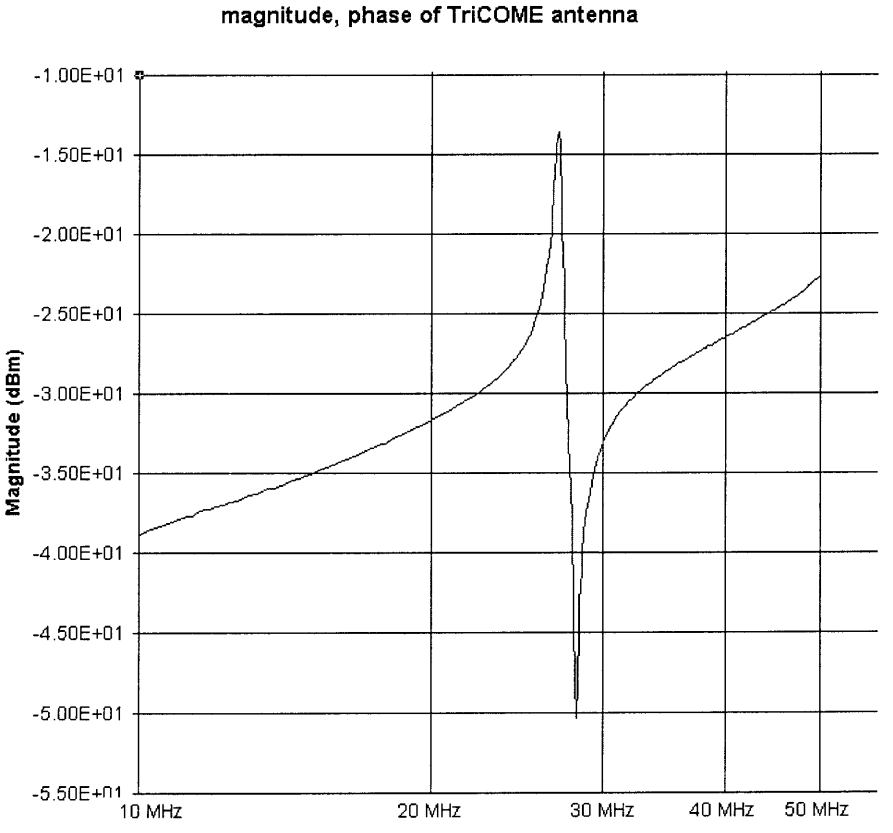


Figure 4-5 Measured magnitude vs. frequency for TriCOME antenna

Near resonance, the approximation $Z_{ant} \approx \frac{1}{j\omega C}$ is not applicable, since series capacitance does not dominate. Considering the structure of the antenna (approximately 30 turns of wire wound around a plastic core), the resonant behavior was approximated by a lumped model, an inductor, L_a, in series with its intrinsic resistor, R_s, then parallel with its parasitic capacitor, C_p. These three components are in series with the series capacitor, C_s. Adding this model to Figure 4-4 yields Figure 4-6.

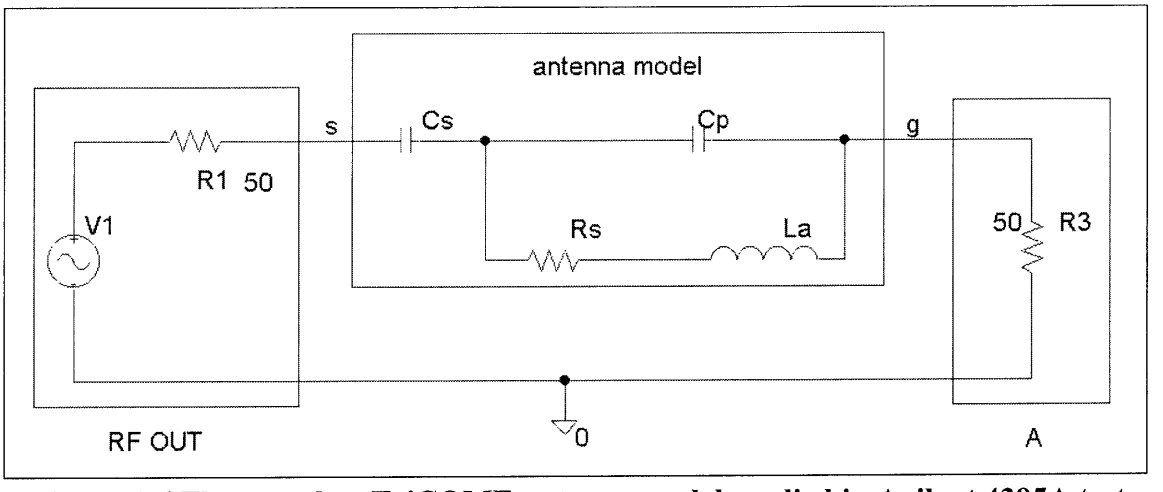


Figure 4-6 The complete TriCOME antenna model applied in Agilent 4395A test setup

To better understand the antenna behavior, the series RL network can be converted to an equivalent parallel RL network. The equivalent relationship can be expressed by [9]

(4-8)

$$R_P = R_S(1+Q^2) \cong Q^2 R_S \text{ , Q} >> 1$$

The transfer function from V_1 to V_a can be written

(4-9)

$$H(\omega) \cong \frac{R_1}{R_1 + R_2 + \frac{1}{j\omega C_S} + \frac{1}{j\omega C_P + \frac{1}{j\omega L_a} + \frac{1}{R_P}}},$$

using the approximation of parallel equivalence.

When L_a resonates with C_p, the transfer function has minimum value, corresponding to the valley in Figure 4-5. The model predicts this minimum is $R_1 / (R_1 + R_2 + R_P + 1/j\omega C_S) \cong R_1 / R_P$.

Eq. (4-9) can be also approximated as

(4-10)

$$H(\omega) \cong \frac{R_1 \cdot j\omega C_S \cdot (1 - \omega^2 L_a C_p)}{2R_1 \cdot j\omega C_S \cdot (1 - \omega^2 L_a C_p) + (1 - \omega^2 L_a (C_p + C_S))}$$

When L_a resonates with the sum of C_p and C_s, the impedance of both C_p and L_a is much less than R_p and the transfer function reaches its maximum of about ½. C_p and L_a can be calculated from

(4-11)

$$C_P = \frac{C_S}{\left(\frac{\omega_P^2}{\omega_{PS}^2}\right) - 1}, \quad L_a = \frac{1}{\omega_P^2 C_P}$$

, where $\omega_P = \frac{1}{\sqrt{L_a C_P}}$ and $\omega_{PS} = \frac{1}{\sqrt{L_a (C_P + C_S)}}$

The value of L_a determined from Eq. (4-11) is reasonably close to the value of 6 μH calculated using the model of infinite solenoid [30] [11].

The quality factor of the inductor, $Q = \frac{\omega L}{R_S}$, determines the magnitude and bandwidth of the peaking at ω_P and ω_{PS}. Once C_s, C_p, and L_a were determined using Eq. (4-7) and (4-11), R_S was determined by adjusting its value to match the peak of the response in Figure 4-5. This value is reasonably close to the theoretical value of Rs calculated using the resonance frequency and the bandwidth.

The parameter values of the TriCOME antenna, after tuning the ω_{PS} peak to 27.0 MHz, are summarized in Table 4-1.

Table 4-1 The calculated parameters for the TriCOME antenna model

Cs	1.81 pF
Cp	18.4 pF
La	1.71 uH
Rs	4.27 ohm

Based on the above model and parameters, a circuit simulation of impedance was compared to an impedance measurement mode using an Anritsu MS4623B Vector Network Measurement System, as shown in Figure 4-7 and Figure 4-8. The two waveforms have the same shape but their peak and valley are shifted in frequency because the C_p parameter is very sensitive to the proximity of the ground plane. Figure 4-7 is based on data in which the peak was tuned to 27 MHz, while the measurement using Anritsu VNA was not tuned. Away from resonance, the measured impedance has noise which makes the phase bounce between ±90°. Otherwise, the phase and magnitude of the measured and modeled antenna impedance are the same.

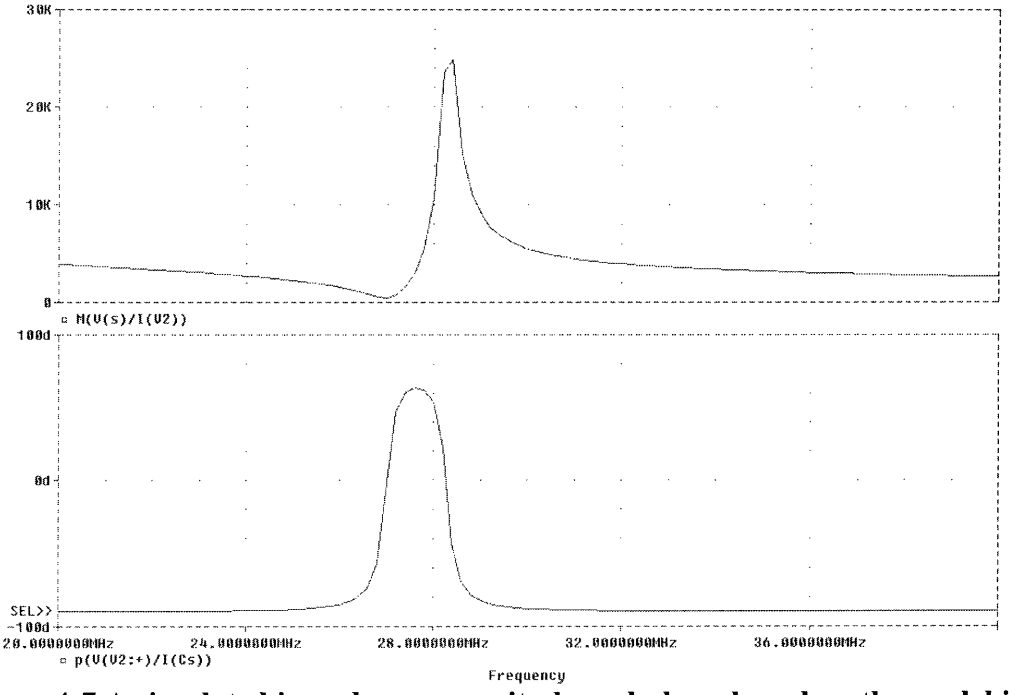


Figure 4-7 A simulated impedance magnitude and phase based on the model in Figure 4-6

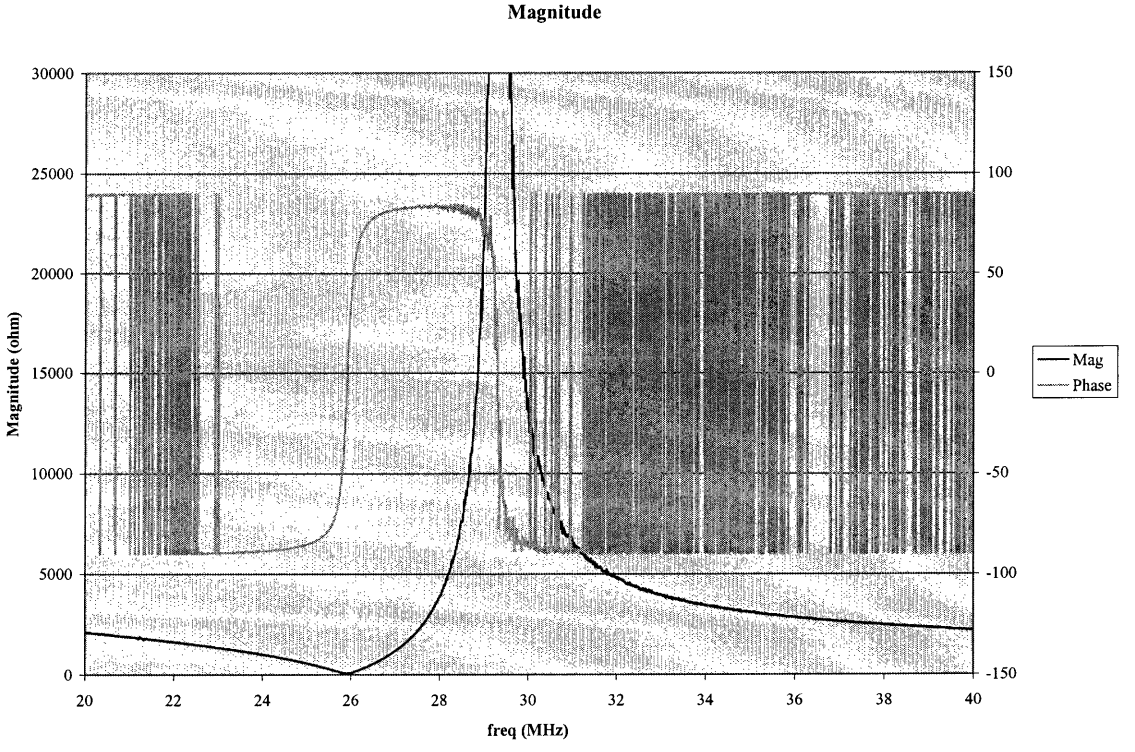
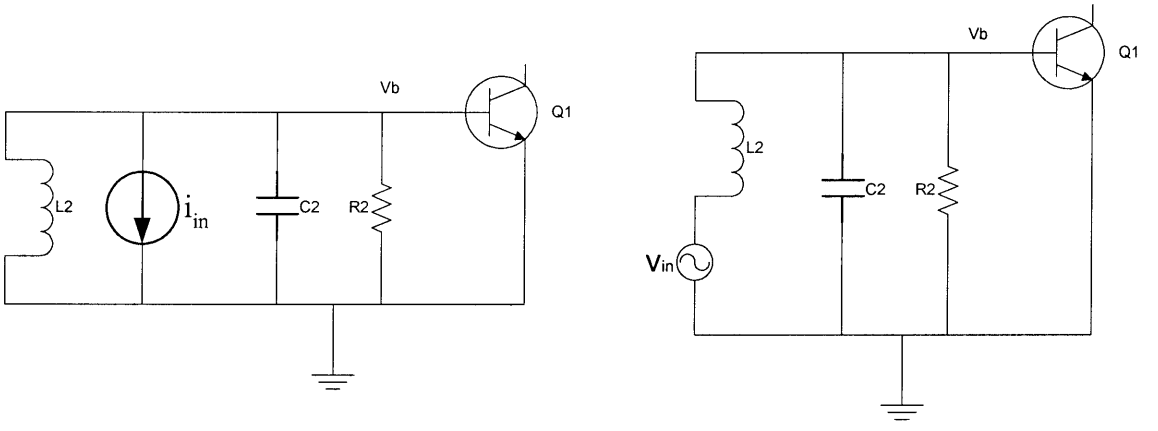


Figure 4-8 The magnitude and phase of TriCOME antenna measured from R&S network analyzer

4.4 Receiver SNR Calculation for Parallel Tuning in the Common-Emitter Configuration

A BJT was selected to amplify the very weak, coupled voltage signal v_b from parallel tuning, as shown in Figure 4-9. The received, i.e. induced signal, is modeled either as a Norton current or Thevenin voltage.



(a) (b)

Figure 4-9 Parallel tuning with BJT common-emitter configuration: (a) model using induced current; (b) model using induced voltage.

From Eq. (4-1), we can determine that

(4-12)

$$i_{in} = -\frac{M}{L_2} i_1 = -k\sqrt{\frac{L_1}{L_2}} i_1$$

$$i_{in} = -k\sqrt{\frac{L_1}{L_2}} i_1 \cdot j\omega L_2 = -k\sqrt{\frac{L_2}{L_1}} v_1 ,$$

where i_1 and v_1 are the transmitter current and voltage, respectively. When L_2 and C_2 resonate at the transmission carrier frequency, the current of the self inductance is cancelled by the current going of the capacitor, which has amplitude of Q times i_{in}. The induced current flows through the resistor R_2, which is the parallel combination of the

equivalent parallel resistor of the inductor and input resistance of the amplifier. Therefore, the input voltage at node b is given by

$$v_b = i_{in} R_2 = -k\sqrt{\frac{L_1}{L_2}} i_1 R_2 \tag{4-13}$$

Using Eq. (4-4), v_b can be written

$$v_b = -k\sqrt{\frac{L_1}{L_2}} \frac{v_1}{j\omega_0 L_1} R_2 = \frac{Q v_{in}}{j}, \tag{4-14}$$

where $Q \equiv R_2 /(\omega_0 L_2)$.

Hence, the base voltage is Q times the induced voltage. Q depends on R_2 and L_2, and R_2 is assumed dominated by r_π.

From transmitter simulations, the RMS voltage across the planar antenna, v_1, is ~140 mV, the inductance of the planar antenna L_1 is 200 nH and k is expected to be about $1x10^{-6}$ at 1m distance. Referring to the antenna model analysis in section 4.3, L_2 is about 1.7 uH. The input signal can be calculated using Eq. (4-15), and Q is 35 for $R_2 \cong r_\pi = 10k\Omega$.

$$| v_b | = Q | v_{in} | \approx 14.3uV \text{ rms} \tag{4-15}$$

Q1 must be biased properly so that it operates in the forward-active region. Its small-signal equivalent circuit at resonance is shown in Figure 4-10, in which C_π and C_μ are assumed to be included in C_2, which is cancelled by L_2.

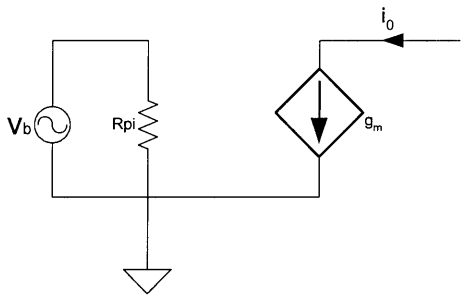


Figure 4-10 Small-Signal equivalent circuit of the pre-amplifier input, at resonance.

By applying g_m equation, Eq. (4-14) and Eq. (4-12), the output current i_o can be represented by

$$i_0 = g_m v_b = \frac{\beta}{R_\pi} \cdot \frac{R_\pi}{j\omega_0 L_2} \cdot v_{in} = \frac{\beta}{j\omega_0 L_2} v_{in} = k \frac{\beta}{j\omega_0 \sqrt{L_1 L_2}} v_1 \tag{4-16}$$

Surprisingly, the amplitude of the output current is proportional to β and v_1, and inversely proportional to $\sqrt{L_1 L_2}$. It has no direct dependence on the transconductance g_m and r_π. The calculation is only accurate given that $r_\pi << R_p$, where R_p is the equivalent resistance of the antenna. Also, adequate biasing current is required to ensure that Q1 operates in the forward-active region and has adequate f_T. Although the receiver is not constrained by power consumption, output noise current is reduced when bias current is reduced.

The Zetex NPN silicon planar RF transistor BFS17H was selected for this work and the collector bias current is 200 uA. The transconductance is

$$g_m = \frac{I_c}{V_{th}} = \frac{200\mu A}{26mV} \approx 8mA/V, \tag{4-17}$$

so $i_o \cong 14\mu V \cdot 8mA/V = 115nA$ rms. Typical characteristics are shown in Figure 4-11. The figure shows that 200 MHz is the cut-off frequency for I_C = 200 μA, which indicates

that the current gain at 27 MHz is about 8. Current gain vs. unity gain frequency was simulated using the manufacturer SPICE model and shown in Figure 4-12. The current gain at 27 MHz is 14.

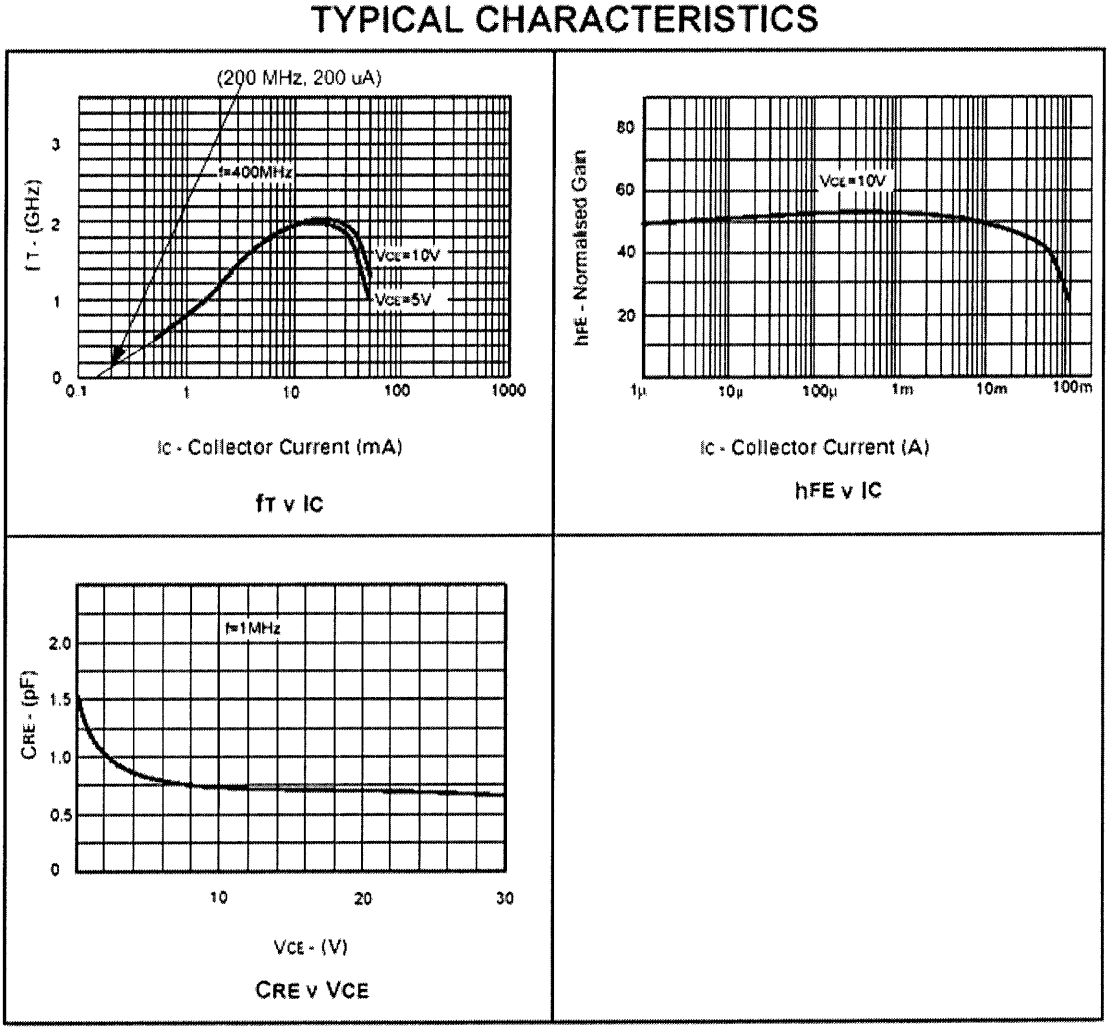


Figure 4-11 Typical characteristics of BFS17H (from [32]).

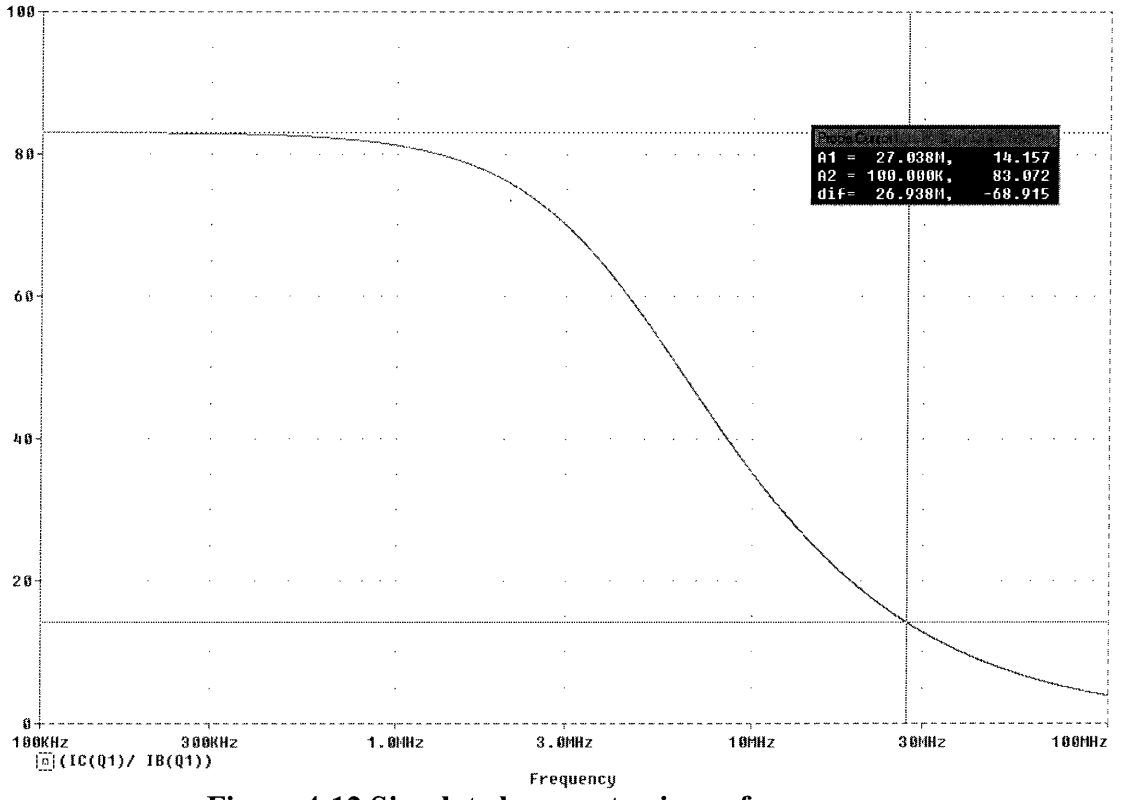


Figure 4-12 Simulated current gain vs. frequency.

The equivalent circuit model for noise is shown in Figure 4-13. Since R_p is neglected, the base is open circuited at resonance; the emitter is virtual ground. The output current i_o consists mainly of shot noise and can be written

(4-18)

$$\frac{\overline{i_o^2}}{\Delta f} = \overline{i_c^2} + \beta^2 \overline{i_b^2} = 2qI_c + \beta^2 2qI_B = 2qI_c(\beta + 1) \cong 2qI_c\beta$$

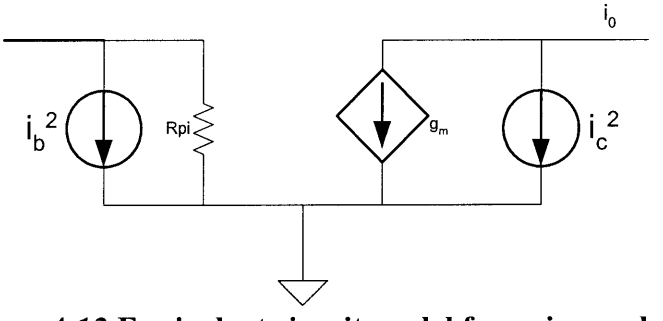


Figure 4-13 Equivalent circuit model for noise analysis

Finally, the signal noise ratio (SNR) is given by

(4-19)

$$(SNR)^2 = \frac{|i_o|^2}{\overline{i_o^2}} = \frac{\left(k\dfrac{\beta}{\omega_0\sqrt{L_1L_2}}|v_1|\right)^2}{2qI_c\beta\cdot\Delta f} = \frac{k^2|v_1|^2}{4\pi\cdot kT\cdot f_{BW}^2 L_1},$$

where v_1 is the rms voltage on the transmitter, k in the denominator is Boltzmann's constant and k in the nominator is the coupling factor. The SNR results from simulation and calculation using $k=1x10^{-6}$, $v_1=140$ mV, $f_{BW}=500$ kHz and $L_1=200$ nH are 4.7 and 5.1 respectively, which are in good agreement.

4.5 Pre-Amplifier, First Stage Design

Due to the very weak coupling ($k=10^{-6}$) between transmitter and receiver, the signal coupled to the receiving antenna is very small. It is comparable to the noise of most operational amplifiers on the market, so a custom amplifier is required. The first stage of the amplifier should be a high-Q band-pass filter where the bandwidth is set by the bandwidth of the FSK modulated signal at transmitter, in order to minimize noise.

The design is based on the common-emitter configuration, for which SNR is given in section 4.4. In this section, output impedance is considered and shown to be greatly affected by the feedback capacitance C_u.

The circuit is analyzed based on the model shown in Figure 4-9, for which the output impedance is

(4-20)

$$Z_o = \frac{1+Y_\pi/Y_\mu}{g_m+Y_\pi},$$

where Y_π is the admittance of paralleled L_2, C_2, r_π, and Y_μ is the feedback capacitance (collector-base capacitance), about 1pF. The calculated magnitude of Z_o is about 132 ohm. Using the simulation model in Figure 4-14, the magnitude of Z_o is 73 ohm.

The output impedance of the first stage is too small to drive a load resistor or a transresistance stage which is likely to have an input impedance near 1000 ohm. Most of the signal will be lost. Therefore, a cascoded first stage is chosen.

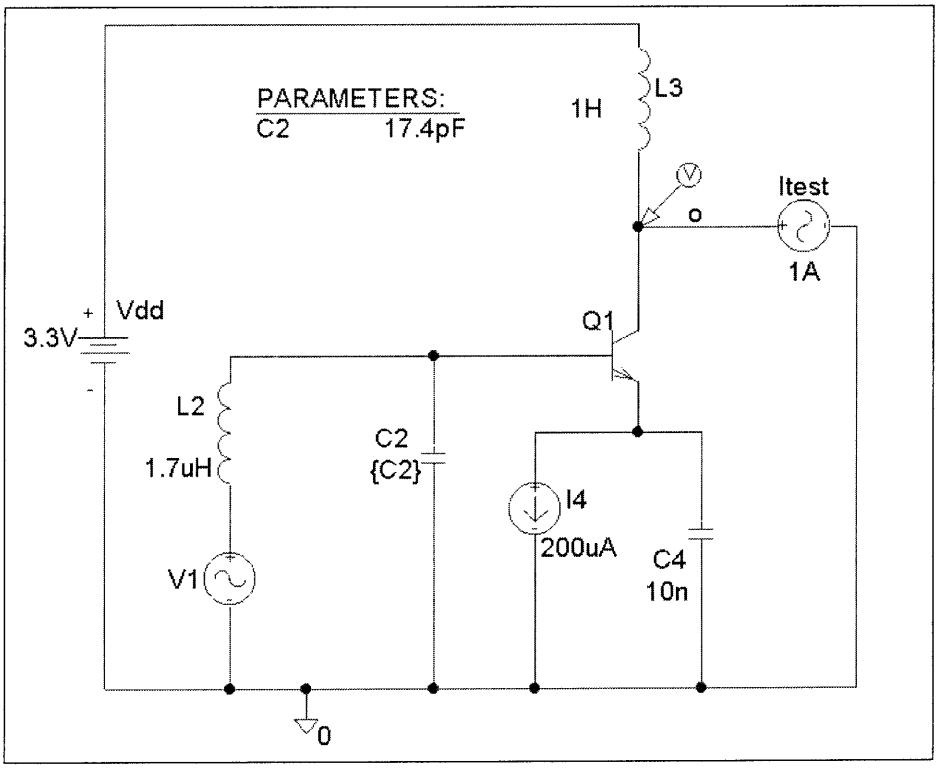


Figure 4-14 Simulation model for impedance analysis of the parallel-tuned, common-emitter configuration. I4, C4 and L3 provide proper biasing, incremental ground for the emitter, and incremental open for the collector.

SNR of the cascoded configuration was simulated using the circuit shown in Figure 4-15. SNR should not be affected by the cascading, since the transconductance of the cascode configuration is same as the transconductance of Q1. The noise also does not change. The simulation verifies that SNR is not affected by the cascode.

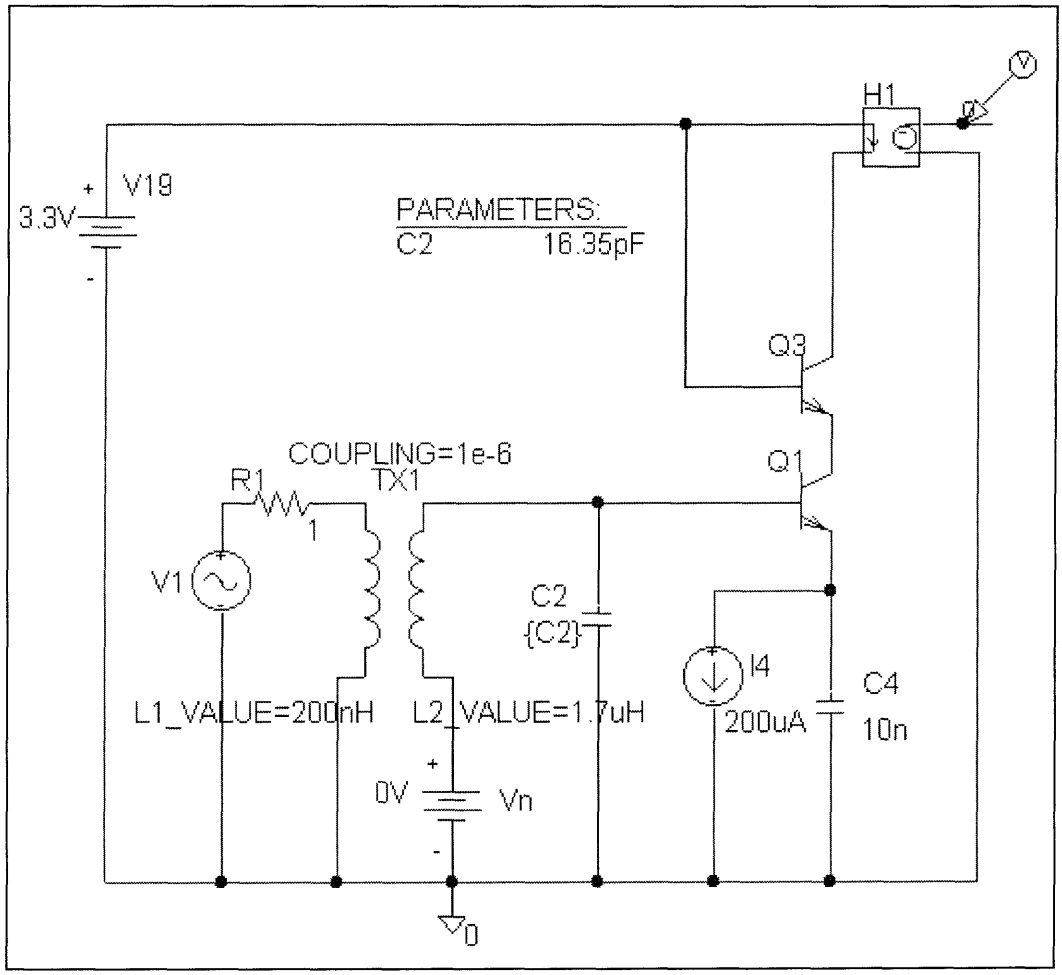


Figure 4-15 Simulation test circuit for SNR analysis at the parallel-tuned, common-emitter configuration. H1 acts as an ideal transresistance amplifer for analysis of output noise.

The simulated output impedance is 3.7 kΩ, roughly β times greater than for no cascode, which is adequate to drive a second-stage transresistance amplifier.

In summary, the cascode configuration greatly improves the output impedance while having negligible effect on SNR. The cascode design is somewhat more difficult to bias and is ideally suited for an IC implementation.

In Figure 4-16, the TriCOME antenna model is used with the cascoded pre-amplifier and current-mirror biasing. L7 must be a large value such that it is a short circuit for DC, but open at the FSK frequency. The high impedance of L7 at the FSK

frequency ensures that it has no impact on the antenna signal going into the amplifying stage. Additional details of the bias circuit are discussed in section 4.5.1. An ideal transresistance and the ideal current source were used for preliminary simulation of noise and output impedance.

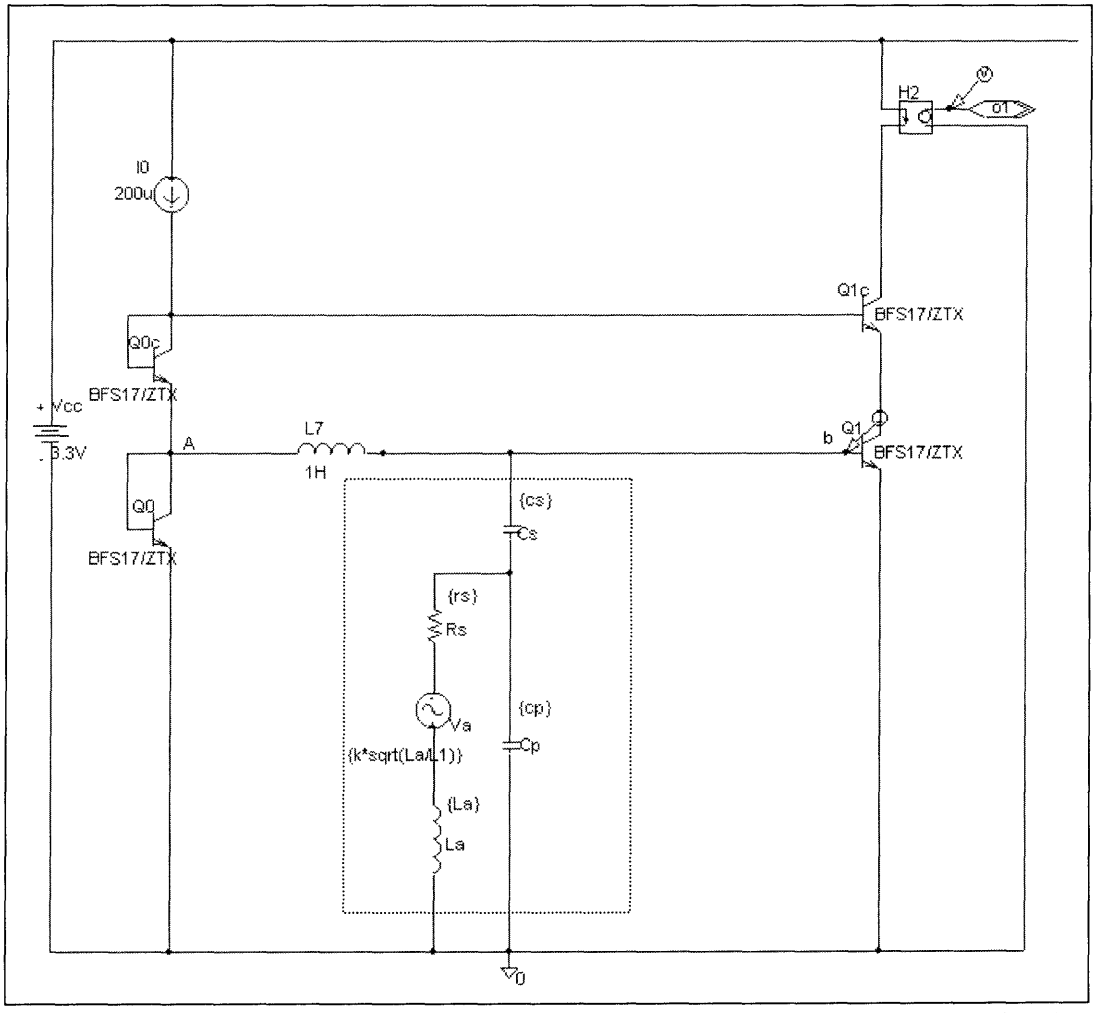


Figure 4-16 Simplified parallel-tuning cascode configuration with TriCOME antenna model and current-mirror biasing.

The existence of C_s in the TriCOME antenna model complicates the analysis, but this model can be converted to an equivalent parallel model for the frequencies near

resonance, as illustrated in Figure 4-17. To make the conversion, quality factor is used often. These definitions are made:

$$Q_2 = \frac{\omega L_a}{R_s} = 67; \tag{4-21}$$

$$Q_3 = R_\pi \omega C_b = 6.1; \tag{4-22}$$

$$Q_4 = \frac{1}{R_{\pi\_s} \omega C_b} = 18.4, \tag{4-23}$$

where C_b is represented by Cpi_u based on the model in Figure 4-16.

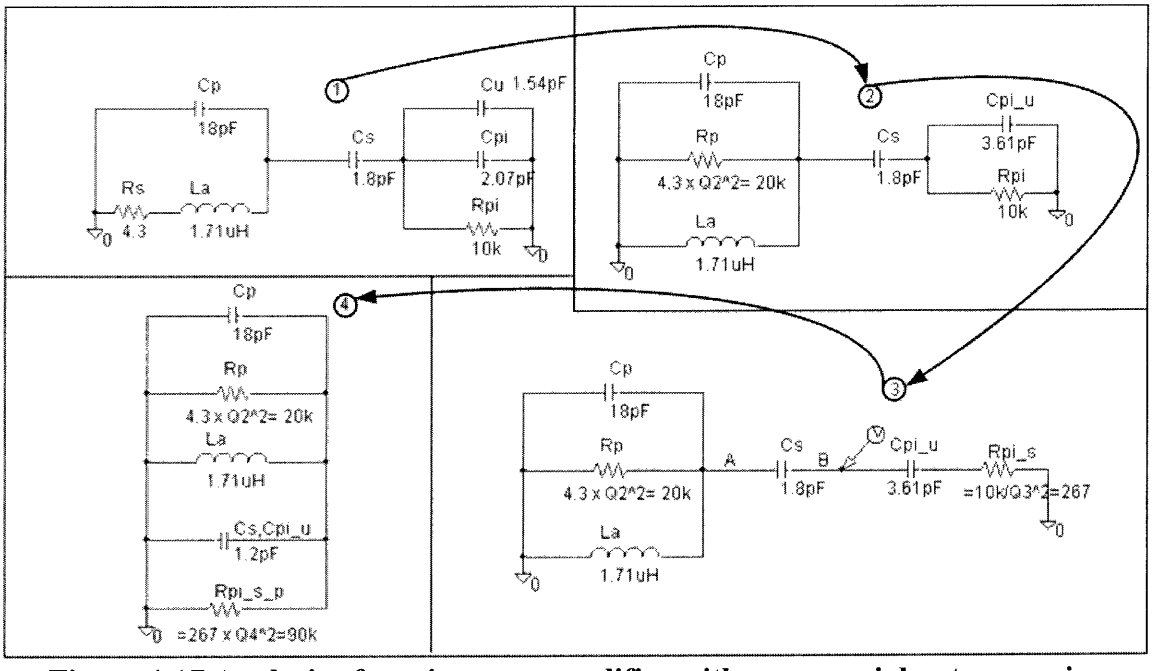


Figure 4-17 Analysis of receiver pre-amplifier with commercial antenna using equivalent impedance conversion: (1) The original impedance consists of antenna model and the related components from the cascode. (2) Converted tricome parallel antenna model and simplified Q1 components. (3) Converted series Q1 components. (4) Converted parallel model.

Following the conversion, the quality factor is easily calculated to be

$$Q = \frac{R_p \parallel R_{pi\_s\_p}}{\omega L_a} \cong 57 , \tag{4-24}$$

i.e. the quality factor is approximately determined by the properties of the commercial antenna, not the pre-amplifier. Q is higher than calculated when r_π was assumed to dominate the calculation, and determines a bandwidth of f0/Q 474 kHz, close to the desired bandwidth. However, the voltage $v_{IN}Q$ is attenuated by C_s and C_{π_μ}, ~1/3. Thus, the base voltage is equal to the induced voltage multiplied by Q times 1/3, which is about 7.8 uV rms. The simulation shows 6.4 uV for the input voltage; SNR is about 3, i.e. 9 dB.

The output impedance was checked again. It is approximately 4 k , about same as the parallel-tuned, common-emitter.

The bandwidth was also examined by simulation and hand-calculation. Based on the quality factor in Eq. (4-24) and the carrier frequency of 27 MHz, the bandwidth is 474 kHz, which higher than the data sheet. The simulation shows 450 kHz in agreement.

Given that the antenna is very sensitive to the ground, it is likely that the ground changes the loop-to-loop capacitance, C_p. When the ground is moved nearer to the antenna, the capacitance increases and the peak response shifts to lower frequency. Thus, the distance between ground and the antenna or the size of ground pad can be used to tune the peak frequency.

4.5.1 Biasing Circuit

Transistors Q0, Q0c, Q1 and Q1c form a cascoded current mirror. The bias transistors are diode-connected, so the transistors operate in the forward-active region

[10]. The current mirror does not depend on the exact i-v characteristics, but Q0 and Q1 should be well matched. All transistors have the same base-emitter voltage since their collector current is approximately the same.

In practice, discrete BJTs are less well-matched than discrete resistors. The effect of mismatch is described by equation (4.163) in [10],

(4-25)

$$\frac{\Delta I_c}{I_c} = \left(\frac{1}{1+\frac{g_m R}{\alpha_F}} \right) \frac{\Delta I_s}{I_s} + \frac{\frac{g_m R}{\alpha_F}}{1+\frac{g_m R}{\alpha_F}} \left(-\frac{\Delta R}{R} + \frac{\Delta \alpha_F}{\alpha_F} \right)$$

The mismatch is mainly determined by transistor I_s mismatch (ΔI_s) when $g_m R$ is $<< 1$, while the second term (ΔR and $\Delta \alpha_F$) are dominant when $g_m R$ is $>> 1$, i.e.

(4-26)

$$\frac{I_c R}{V_{th}} >> 1$$

Therefore, to improve matching, resistors were added at the emitters of Q0 and Q1. The drawback of the method is a trade-off of output swing. Considering this, the two resistors were designed to be 400 Ω and $I_c R$ is about four times V_{th}.

The resistor increases the input resistance of Q1 (R_{in} $r_\pi[1+g_m R_e]$), so the voltage $v_{IN}Q$ attenuated by C_s and C_{π_μ} is less, i.e. the base voltage is higher than when $R_{in} = r_\pi$, 10.6 μV. On the other hand, G_m is lowed down by $[1+g_m R_e]$. Finally, the increment ratio of the base signal is less than the decrement ratio of G_m and the output amplitude is lower. SNR ends up with 2.4, i.e. 7.7 dB.

Referring to Figure 4-16, a large RF capacitor was added to the base/collectors of Q0c, the base of Q1c, and another to Vcc to ensure that they act as virtual grounds. (see Figure 4-21)

The simplest reference current source is a resistor, but it has a nearly 100% supply dependence since $I_{ref} = (V_{cc}-V_{BE}) / R \quad V_{cc} / R$. To minimize the impact of variation in the power supply, an n-channel JFET 2N5457 was selected to generate the reference current supplied by the ideal current source in Figure 4-16. The JFET drain current is given by

(4-27)

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_p})^2,$$

where I_{DSS} is the drain current when $V_{GS}=0$ and V_P is the pinch-off current, which is negative for an n-channel JFET. For the source-degenerated JFET shown in Figure 4-18, V_{GS} is controlled by

(4-28)

$$V_{GS} = -I_D R_{17},$$

so I_D is set by the value of R_{17}. Thus, a 4.7-kΩ resistor was chosen to work with JFET 2N5457 to output a 200 μA reference current. The reference circuit is supply-independent, but does depend on the JFET characteristics.

Figure 4-21 shows the final bias circuit, including emitter degeneration resistors, R0e and R1e, and JFET current source, J2 and R4.

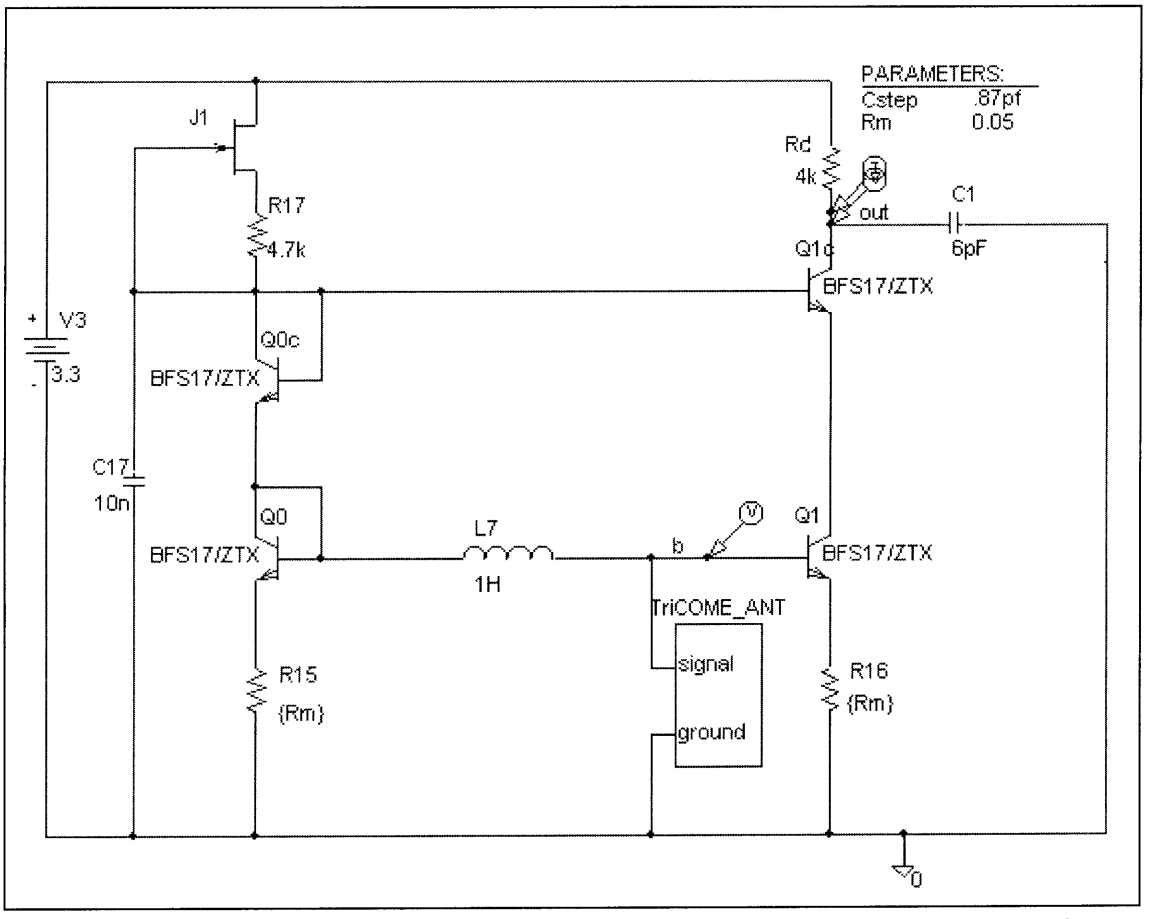


Figure 4-18 A voltage-output approach using load resistor Rc. The load capacitance is estimated to be 6 pF.

4.6 Pre-Amplifier, Second Stage Design

Referring to Figure 4-16, the first stage provides 20 nA rms from the Q1c collector. Although the out-of-band noise is minimal, the signal is too small to be measured by oscilloscope or drive a FSK demodulator. Further amplification can be achieved by simply connecting a load resistor to the Q1c collector, but output impedance would be large. Such a circuit is shown in Figure 4-18, where the estimated load capacitance is 6 pF. The load resistor can be represented by

(4-29)

$$R_{load} = R_c \parallel R_{1st\_out} \parallel R_{2nd\_in}$$

Since R_{1st_out} is about 4 kΩ, the maximum output signal is about 20 nA • 4 kΩ = 80 μV rms. Worst still, R_{load} and C1 form a low-pass filter with a bandwidth of just $\frac{1}{2\pi RC} \cong 6MHz$.

A better choice is the transimpedance amplifier, shown in Figure 4-19. The addition of L1 allows cancellation of the bandwidth limiting capacitance, and input resistance is just R_2/A_{v2}, which can be made much smaller than the 1st stage output resistance, even though the gain R_2 is high. A high-value RF capacitor was used to couple node s and node b to isolate bias levels in the 1st and 2nd stages.

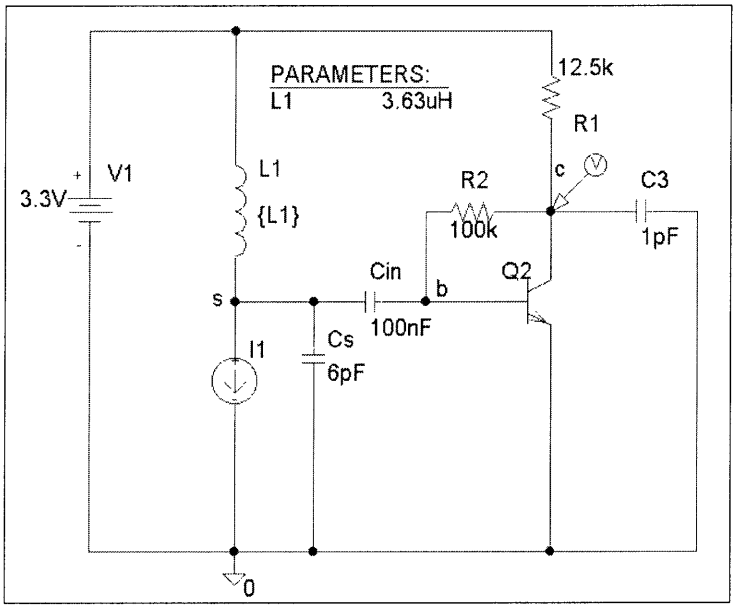


Figure 4-19 A simple transimpedance amplifier. I1 represents the input signal , for example, from the 1st stage of the pre-amplifier

R_f (R_2 in Figure 4-19) sets close-loop gain, and also provides the bias current for Q2. With I_c set to 200 μA and β=80, base current is about 2.5 μA, and the voltage drop across R_2 is 250 mV. Bias stability and signal swing would be compromised if this were allowed to be larger.

Miller-effect must also be considered in this design since the base-collector capacitor, C_μ, is amplified by the open-loop voltage gain A_{v2}, about 100 in this design. If the Miller multiplied capacitor is too large, L1 must be made unreasonably small to achieve cancellation at resonance. Also A_{v2} is not particularly stable, so cancellation would not be stable.

A cascode approach is employed to eliminate the miller effect. (Figure 4-20) The cascode approach has slightly reduced the output swing, but eliminates the Miller effect and provides a higher output impedance.

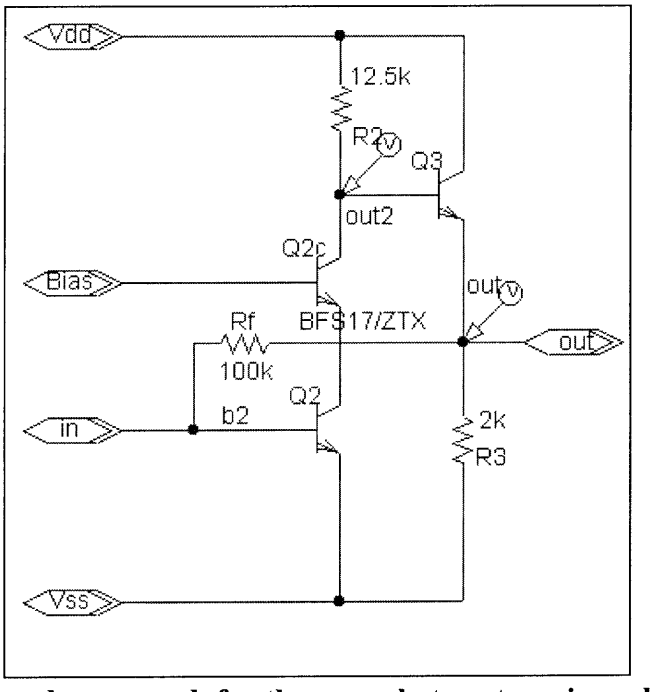


Figure 4-20 Cascode approach for the second-stage transimpedance amplifier

Finally, a feedback-biased emitter follower output stage is designed to provide a 50 output impedance, as shown in Figure 4-20. The amplifier input resistance is $r_\pi \| (R_f / A_{v_2}) \cong 1k\Omega$ and the input capacitance is (C_π + 2C_μ) 6 pF. The input capacitance is device dependent, but stable, and is cancelled by L1 in Figure 4-19. Since

R_{in2} ¼ R_{out1}, 80% of the received signal is driven across R_f to create an output of about $20nA \cdot 80\% \cdot 100k\Omega = 1.6mA$ when k=10^{-6}.

The bandwidth of the second stage should be wider than the first in order to pass all the information from the first stage. Simulation of Figure 4-19 shows that the bandwidth is 2.8 MHz, safely wider than the first stage, which is 450 kHz. The simulated gain is 88 kΩ, little less than 100 kΩ, primarily due to loss to r_π.

4.7 Pre-Amplifier Complete Design

The complete receiver pre-amplifier is shown in Figure 4-21. Considering the unknown parasitic capacitance and the variation of the devices, L8 is made somewhat smaller than necessary to achieve perfect resonance, and a small C7 is added for fine tuning. This capacitor is fabricating using 2 stiff wires that are twisted together. Another tuning capacitor, CT, is placed in Figure 4-21 to represent the adjustable ground pad that is used to tune antenna.

The circuit was simulated to verify its overall SNR and bandwidth. The SNR for k=10^{-6} is 26 dB while the bandwidth is 450 kHz. The output voltage will be > 1 mV. Some critical performance parameters are listed in Table 4-2 for comparison.

Table 4-2 Comparison of selective parameters' hand-calculation and simulation

	Hand Analysis	Calculated	Simulated
v_b rms at Q1	2/3 of $Q \cdot v_{induced}$	15.6 uV	10.8 uV
i_c rms (Q1c)	$G_m \cdot v_b$	31 nA	37 nA
i_{in} rms (HS2)	i_c	31 nA	118 nA, including the current flowing into C_π and C_μ
A_{v2} Transimpedance gain	R_f •80%	80 k	88 k
v(out) rms	i_{in} • A_{v2}	2.4 mV	1.7 mV

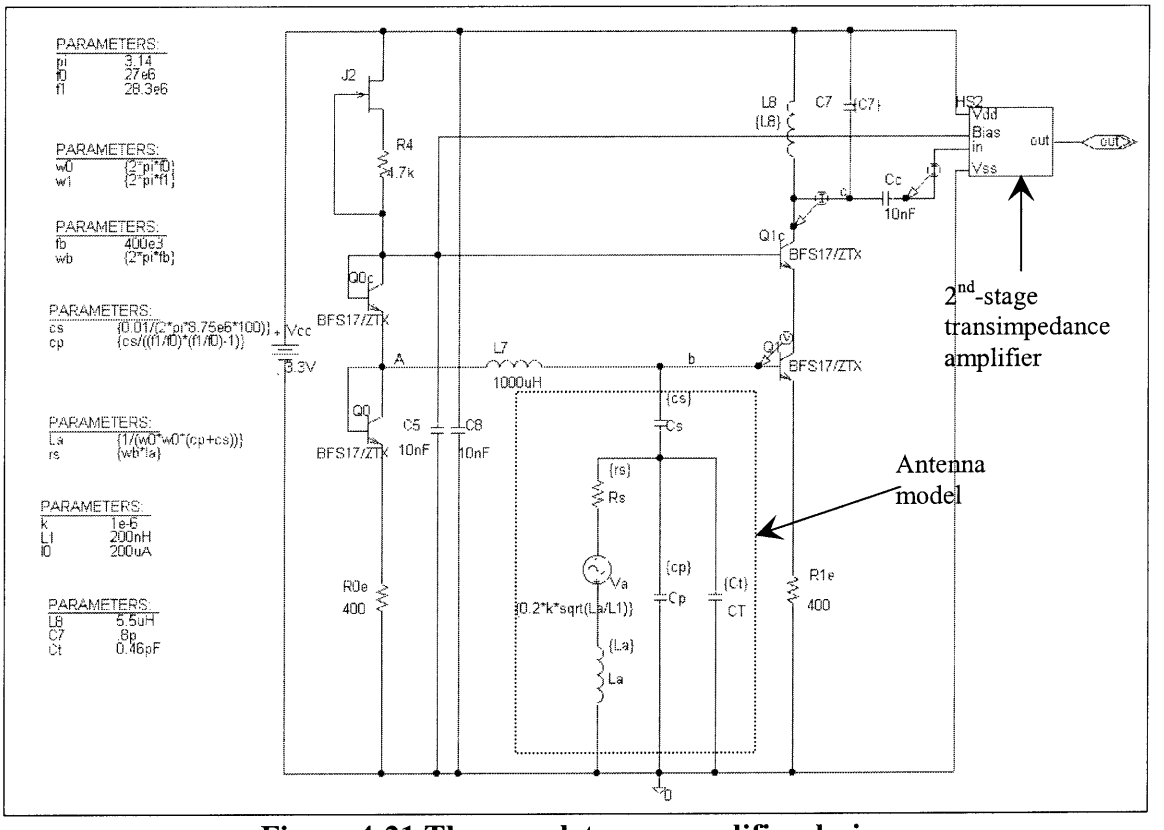


Figure 4-21 The complete pre-amplifier design

4.8 Pre-amplifier Test Results

In this test, the feasibility of pre-amplifier is explored. Test setup is shown in Figure 4-22. Grounding is important, and all unused copper was connected to ground. A potentiometer was used to adjust the reference current. Bias voltage was measured to make sure DC condition. The measured data is shown with the simulated data in Figure 4-23 and they are agreed each other. Tuning was done by adjusting output frequency from the function generator. After tuning, the signal reaches the maximum at 27 MHz by given input. Figure 4-24 shows the pre-amplifier output when the input signal is 27 MHz sine wave, Vpp = 10 mV. The measured gain is less than 40. Considering the input

current loss due to the quality factor of the inductor and R_{pi}, the gain is supposed to be about 160. The measured result is only ¼ and further measurement will be continued.

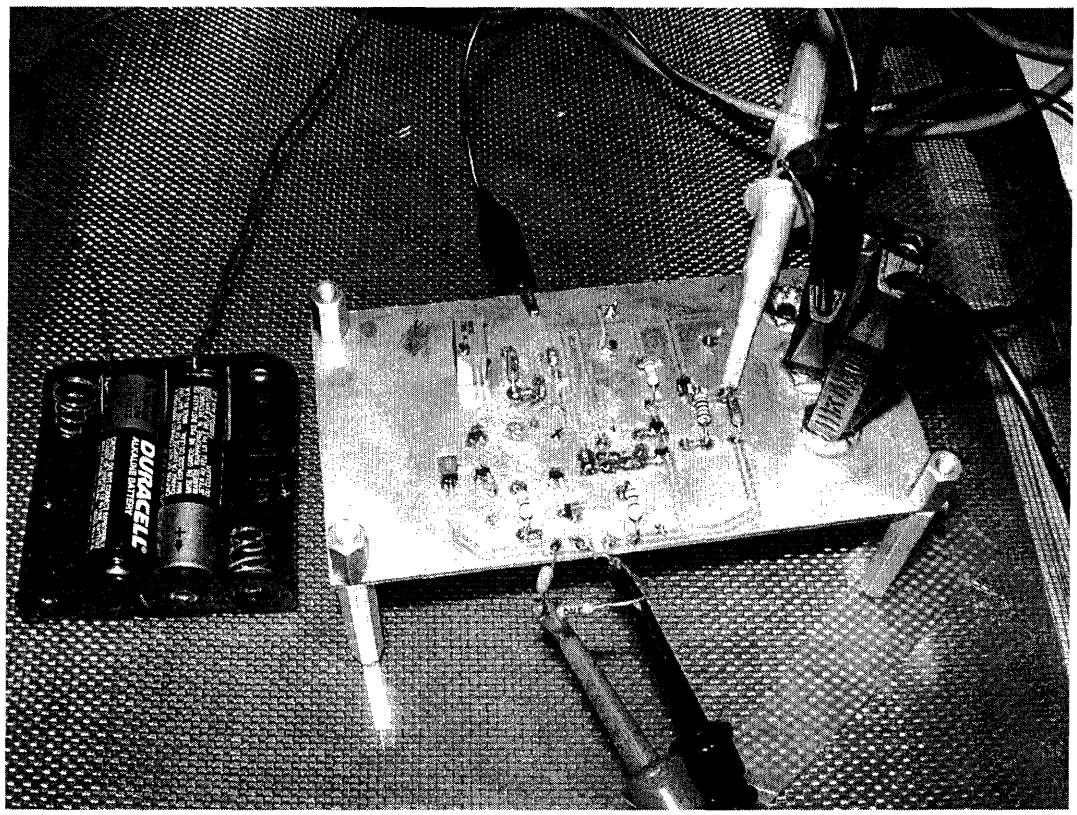


Figure 4-22 Test setup for pre-amplifier test

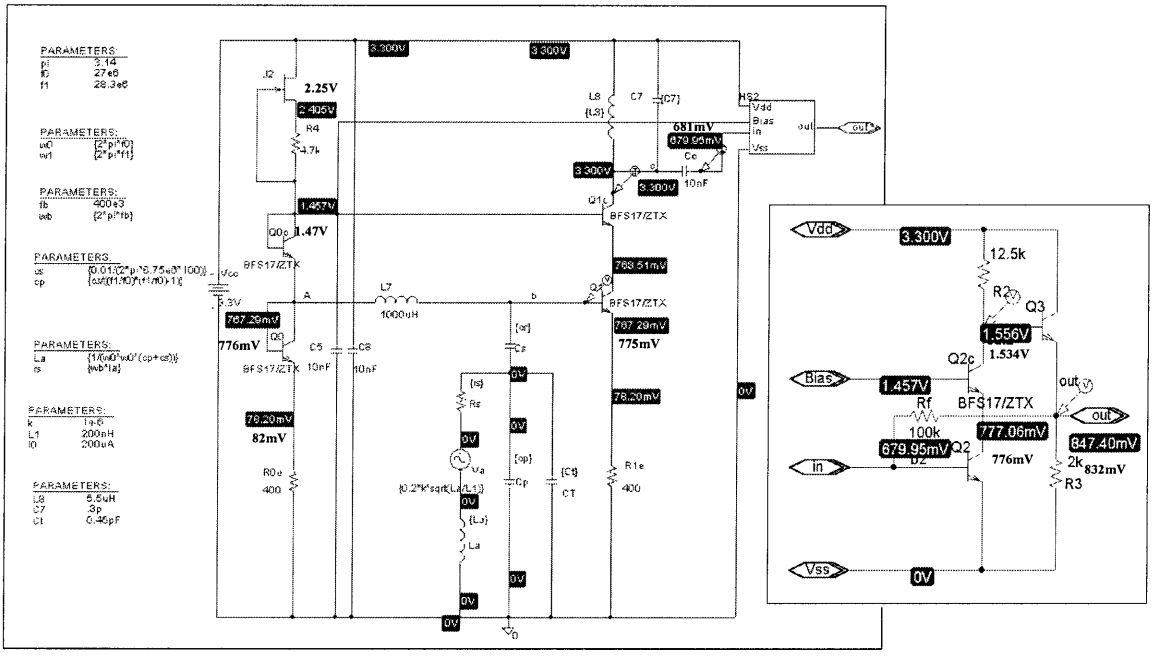


Figure 4-23 Bias point from measurement and simulation

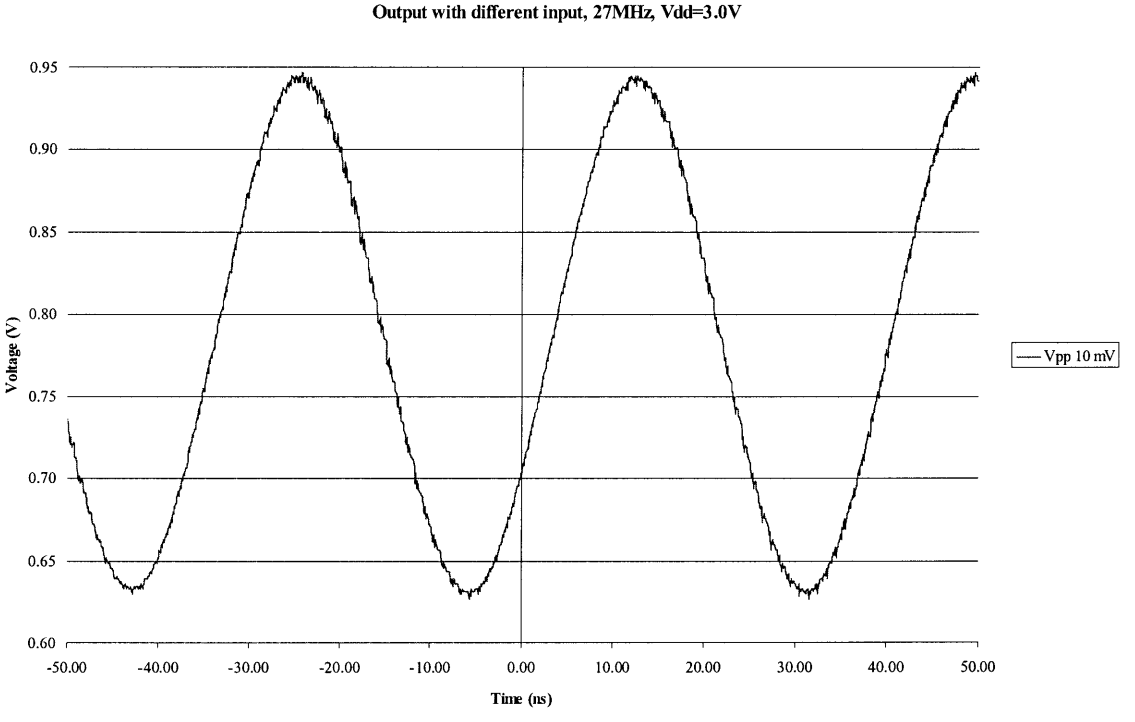


Figure 4-24 Pre-amplifier output when applying Vpp=10 mV, 27 MHz sine wave

5 Conclusion and Future Work

The main purpose of this work has been to explore the feasibility of transmission of sensor data over a distance about 1 meter using robust and low-power electronics suitable for a high-temperature environment. Loop antenna and frequency-shift keying (FSK) have been chosen for the telemetry system in view of their potential for reliable and low-power communication, and a high-temperature wireless telemetry circuit has been designed based on a negative-resistance oscillator which uses a tunnel diode. The project also employs a variable MOSFET capacitor in SOI IC technology. A pre-amplifier was designed to pick up the weak signal using a commercial, room-temperature antenna. The pre-amplifier has been designed to optimize SNR and provide enough gain to make the signal viewable in oscilloscope.

The following aspects of the communication link could be optimized in future work.

The channel and gate resistance of the MOS capacitor should be carefully considered. As discussed in Chapter 2 and Chapter 3, channel resistance reduces the Q, reduces the effective value of MOS capacitance, and reduces the adjustment range of the capacitor. To optimize the MOS capacitor design, the ratio of channel width to channel length should be adequately large.

In the buffer design, both the PMOS and NMOS transistor sizes impact oscillation settling time. The size of PMOS and NMOS should be designed for comparable drive strength.

In the I/O pad design of the SOI IC, the ports for the transmitter (transmitterIn/VCOIn and RFgate) should be digital pads since the transmitter circuit

uses digital power, and this will simplify testing and eliminate conflicts with ESD protection circuitry. The transmitterIn (VCOIn) should be a digitalIn pad, and RFgate may also use the digitalIn pad so that the transmitter circuit can function when analog power is disabled.

In the PCB design, the ground connections should be very carefully considered. The fabrication quality is critical to obtaining maximum performance.

Similar to the commercial 27-MHz antenna, a multi-turn loop antenna should be considered in the future transmitter design. The purpose is to improve transmission efficiency.

The high-temperature PCB material and the high-temperature components must be further explored, used and tested under different high-temperature conditions. The off-chip components should be reduced if possible. On-chip tuning capacitors would be highly desirable. On-chip capacitors could potentially be tuned using laser trimming or discrete fuses.

With enough space on the SOI chip, an on-chip receiver could be considered, and would enable bi-directional communication so sensors could be provisioned or act as relay stations for increased transmission distance. In the automotive engine application, an on-chip transceiver (transmitter and receiver) will permit sensing and actuating.

The work in this thesis establishes an approach for high-temperature sensor interfacing, but tests have thus far been conducted at room temperature. Thus, measurement at high temperature should be done and documented. Also the sigma-delta ADC and decimation filter should be integrated with the communication link.

Ultimately, the whole project would be converted to SiC technology, fabricated and tested at high temperature up to 500 C.

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