Wireless Interface Circuit For High-temperature Applications Using SOI MOS Varactor

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Outline

- Introduction
- Digital Telemetry
- High-temperature Transmitter Design
- Transmitter Measurement and Results
- Receiver Pre-Amplifier Design and Test Results
- Conclusions and future work
- Acknowledgements

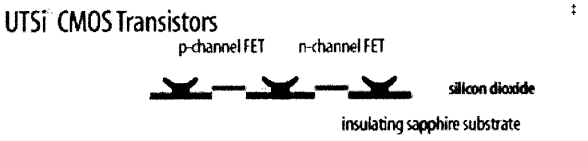
Introduction

Motivation

- Critical to harsh environment systems
- Applications
  - Automotive electronic systems
  - Aircraft industry and space programs
  - Geothermal and well logging

SOI Technology

- Reduces leakage current by isolating devices using dielectric materials
- Peregrine UTSi® SOS technology was chosen in this project to work up to 300°C



‡: www.peregrine-semi.com

Objectives

- Design a high-temperature FSK transmitter with a tunnel diode and a planar loop antenna
- Test FSK transmitter with varactor
- Test FSK transmitter with SOI MOSFET varactor
- Design and test a receiver pre-amplifier to detect a very weak signal at 27 MHz

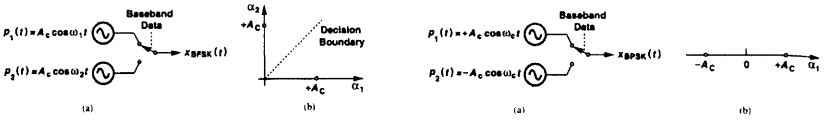
Digital Telemetry

Digital Telemetry

- Carrier frequency
  - ISM band 27.12 MHz ± 163 kHz
- Antenna design
  - Inductively-coupled planar loop antenna implemented on PCB
- Modulation technique
  - ASK, PSK and FSK

BFSK vs. BPSK

- BFSK vs. BPSK

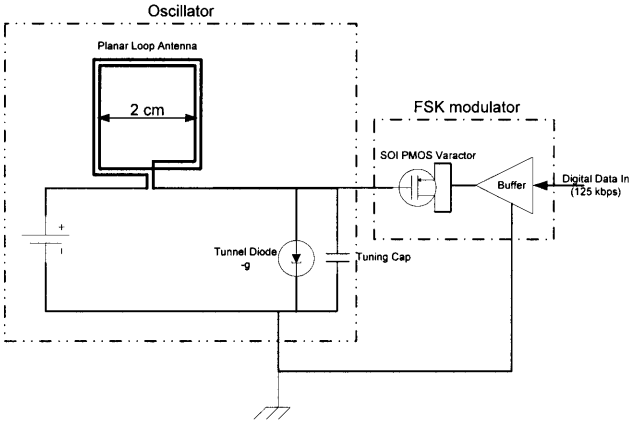


	BFSK	BPSK
BER	$P_{e,BFSK} = Q\left(\sqrt{\frac{E_b}{N_0}}\right)$	$P_{e,BPSK} = Q\left(\sqrt{\frac{2E_b}{N_0}}\right)$
Spectral Efficiency	$BW=2f_b + \Delta f$	$BW=2f_b$
Power Efficiency	Good	Poor

where
E_b is bit energy,
N_0 is noise/bit,
f_b is bit rate,
$\Delta f = f1 - f0$

High-temperature Transmitter Design

Transmitter Architecture



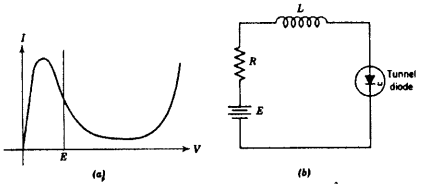
Tunnel Diode Oscillator

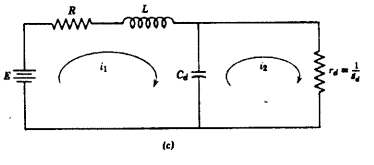
- Bias point
  - Negative resistance region
- Start-up condition

$$\frac{R_1}{R_1^2+\omega^2 L_1^2} < g_d$$

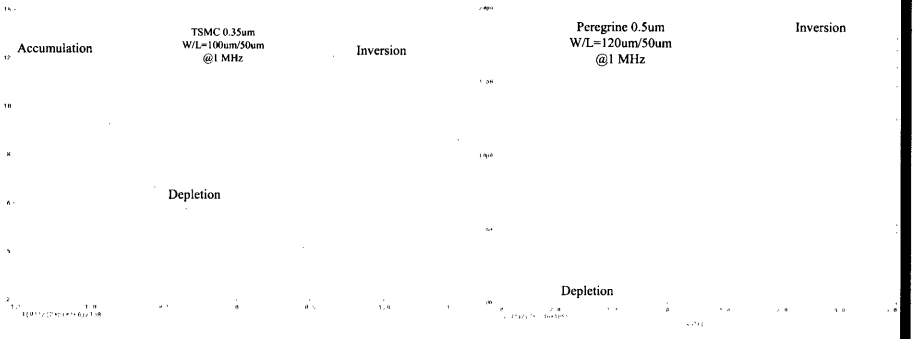
- Oscillation frequency

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L(C_1+C_{td})} - \frac{R_1^2}{L_1^2}}$$





MOSFET Capacitors in Si and SOI

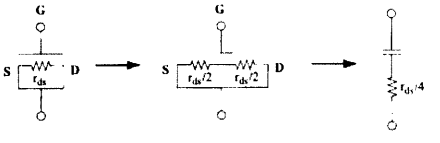


	Si	SOI
Accumulation	$C_{accumulation} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	-
Depletion	$C_{depletion} = C_{ox} + C_d = \frac{\varepsilon_{ox}}{t_{ox}} + \frac{\varepsilon_{Si}}{d}$	$C_{depletion} = C_{ox} + C_d = \frac{\varepsilon_{ox}}{t_{ox}} + \frac{\varepsilon_{Si}}{d}$
Inversion	$C_{inversion} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	$C_{inversion} = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Q in MOSFET Capacitors

Q depends on the channel resistance: $r_{ds} \approx \left[\mu C_{ox} \frac{W}{L} [(V_{GS} - V_T)] \right]^{-1}$

Lumped model for MOSFET capacitors

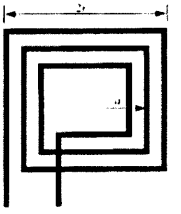


Design Approach: Increase W/L ratio to decrease r_{ds}, increase Q

Planar Spiral Loop Antenna

The inductance was studied and three expressions are used as reference in this project

Expression	Value	From
$L \approx \frac{45\mu_0 n^2 a^2}{22r - 14a}$	237 nH	*The Design of CMOS Radio-Frequency Integrated Circuits* by Thomas H. Lee
$L_{mW} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}$	198 nH	*Simple Accurate Expressions for Planar Spiral Inductances* by Mohan, S.S. etc.
$L = 0.0241 an^{\frac{5}{3}} \log \frac{8a}{c} (\mu H)$	305 nH	*Printed Circuits: Their Design and Application* by Dukes, J.M.C.



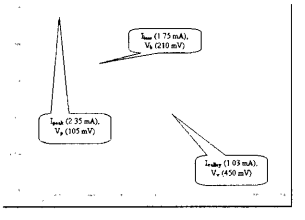
where
n is the number of turns,
a is the mean radius,
d_{avg} is the mean diameter,
2r is the outmost diameter,
ρ is the fill ratio, given by $\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$

c is the radical depth of winding
$c = \frac{1}{2}(d_{out} - d_{in})$

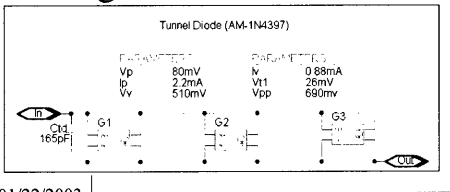
Tunnel Diode

- Germanium tunnel diode 1N4397 from American Microsemiconductor Inc.

V(f) at I_{peak}	690 mV
I_{peak} Max.	2.2 mA
I_{peak} Tolerance	0.22 mA
V_p at I_{peak}	80 mV
V_v at I_{valley}	510 mV
I_{peak} / I_{valley}	2.5
I(f) Max.	4.5 mA
r(s) Max.	2 ohm
C(t) Max.	200 pF
T(operating) Max.	200 °C



- A 3-region model was used



$$I_1 = I_p e^{-\frac{V_{pp}}{V_{t1}}} e^{\left(\frac{V(\%IN+,\%IN-)}{V_{t1}} - 1\right)}$$

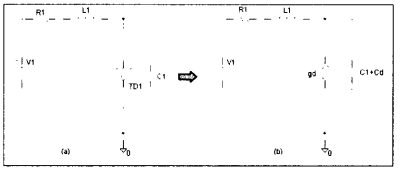
$$I_2 = I_p V(\%IN+,\%IN-) e^{\left(\left(1 - \frac{V(\%IN+,\%IN-)}{V_p}\right) * 0.8\right)}$$

$$I_3 = I_v \frac{V(\%IN+,\%IN-)}{V_V} e^{(V(\%IN+,\%IN-) - V_V)}$$

Tunnel Diode Oscillator

Parameters

Description	Equation	Value
g_d	$-g_d = \frac{\Delta i}{\Delta v}$	7 mA/V
L1	$L_{mW} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho}$	200 nH
Ctd	-	170 nH



Operating Conditions

Conditions	Equation	Value
DC bias	$R_1 < \frac{1}{g_d}$	R1 < 140 ohm
Start-up	$\frac{R_1}{R_1^2 + \omega^2 L_1^2} < g_d$	Yes
Resonance frequency	$f = \frac{1}{2\pi}\sqrt{\frac{1}{L(C_1 + C_{td})} - \frac{R_1^2}{L_1^2}}$	27.31 MHz

FSK-Modulated Transmitter

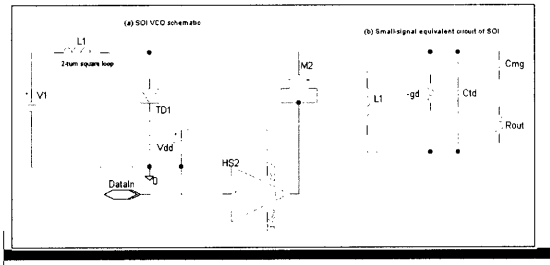
- SOI PL transistor is used

$$C_{inversion} = W \cdot L \cdot C_{ox} = W \cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{depletion} = L(C_{gs0} + C_{gd0})$$

- $f_{high} - f_{low} >= 2\ f_b$

t_{ox}	10.5 nm	
W	120 um	
L	50 um	
C_{gs0}, C_{gd0}	3.6×10^{-10} F/m	
	Calculation	**Simulation**
$C_{inversion}$	19.98 pF	19.72 pF
$C_{depletion}$	36 fF	87 fF



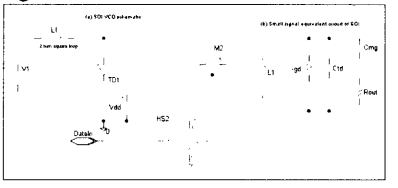
Channel Resistance

- R_{out} includes the channel resistance from PMOS and output resistance from the buffer
- The buffer resistance was designed very small by increasing W/L ratio
- The channel resistance R_{mg} is dominant to impact the circuit

$$Y = \frac{1}{j\omega L_1} - g_d + j\omega C_{id} + \frac{1}{R_{out} + \frac{1}{j\omega C_{mg}}}$$

$$\mathrm{Im}\{Y\} \cong \frac{1}{j\omega L_1} + j\omega C_{id} + j\omega C_{mg}, \text{ if } \omega^2 R_2^2 C_{mg}^2 << 1$$

$$\mathrm{Im}\{Y\} \cong \frac{1}{j\omega L_1} + j\omega C_{id} + \frac{j\omega C_{mg}}{3}, \text{ when W/L=120/50=2.4, f=27MHz}$$



Buffer Design

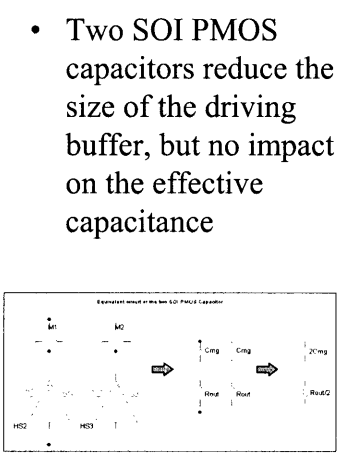
- Objectives
  - Fast transition for both PMOS and NMOS
  - Low output impedance for PMOS
- Transition time must << (125 kbps)$^{-1}$

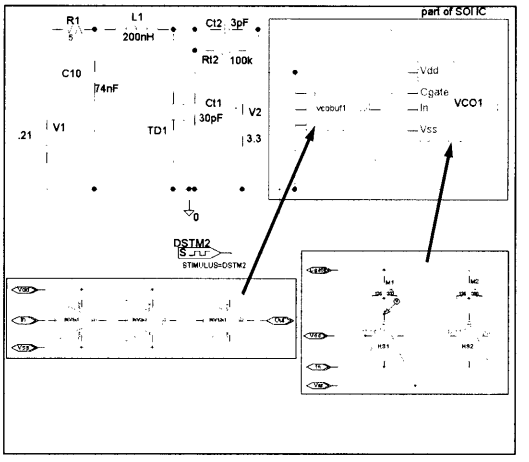
$$\tau_P = \frac{C}{\left(\frac{W}{L} u_p C_{ox} \left(|V_{gs}| - |V_{TP}|\right)\right)}$$

- Four-stage non-inverter buffer design

Complete Transmitter Design

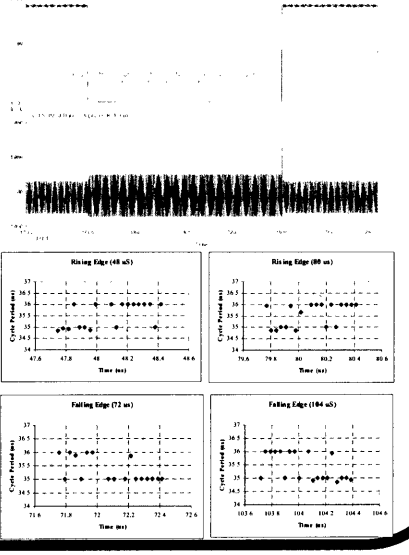
- Two SOI PMOS capacitors reduce the size of the driving buffer, but no impact on the effective capacitance





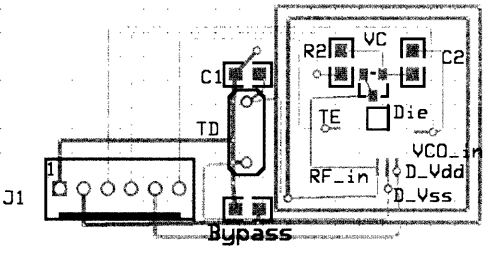
Simulation of Transition Time

- Falling edge takes longer on settling the buffer output
- Both falling and rising edge have clear roll-off
- The roll-off at falling edge results from small size of buffer NMOS
- The roll-off at rising edge results from channel resistance
- Transition time << 10% of bit period (0.8μs)



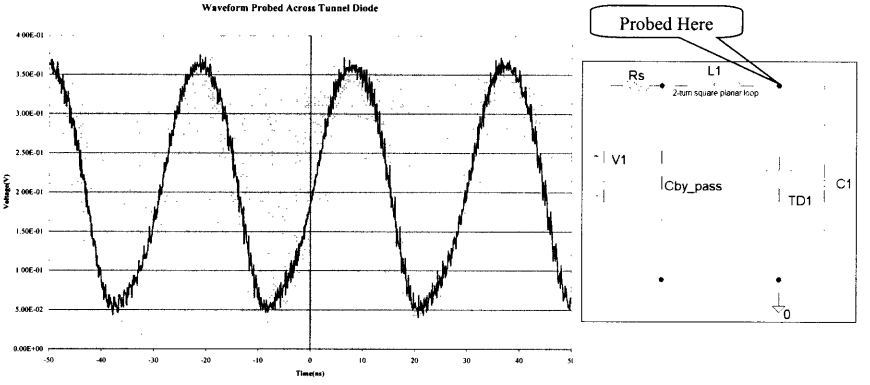
Transmitter PCB Design

- PCB can be used with either SOI die or PN varactor
- SMT components were used to reduce the parasitic effect
- The space inside 2-turn loop was utilized to reduce the size
- The unused copper was removed to reduce eddy current



Transmitter Measurements and Results

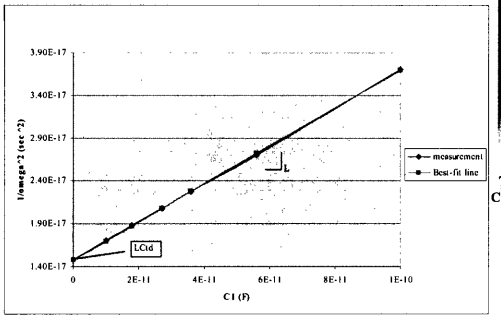
Tunnel Diode Oscillator Measurement

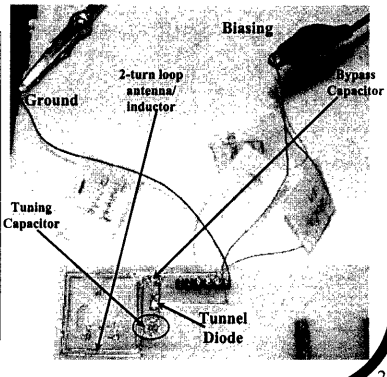


- The measurement was done by HP54615B Oscilloscope
- The voltage oscillated around the bias point, 0.21V
- The peak-to-peak voltage is 320mV

Tunnel Diode Oscillator Test Result

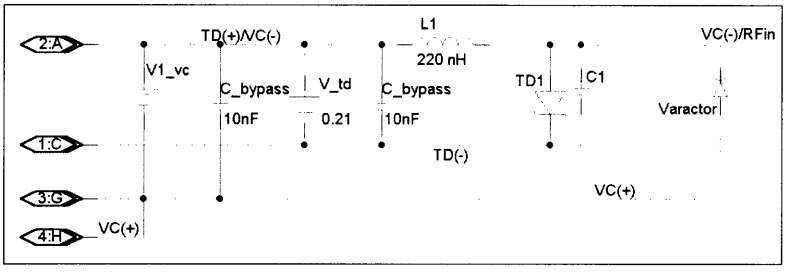
- Linearity $L_1(C_1 + C_{td}) = \frac{1}{\omega_x^2} \Rightarrow \frac{1}{\omega_x^2} = L_1 C_1 + L_1 C_{td}$
- The inductance of 2-turn 2-cm square loop antenna is 218 nH
- The junction capacitance of tunnel diode is 68 pF





Measurement of FSK Transmitter using Si PN Varactor

- Verify the feasibility of FSK modulator concept and PCB design



Frequency Spacing vs. Capacitance Difference

- The relationship between frequency spacing and capacitance difference @ 27 MHz

$$\frac{df}{dc} = -\frac{f}{2C} = -78kHz / pF$$

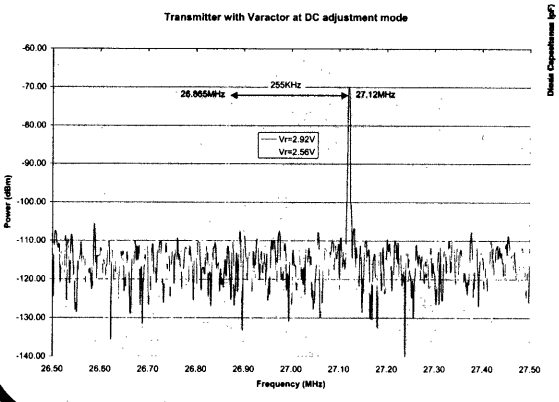
- Bit rate 125 kbps and FSK modulator requires

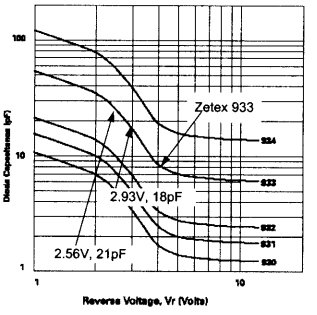
$$\Delta f \geq 2f_b, 250kHz$$

- 3pF capacitance difference are required to provide 250 kHz

Measurement Results

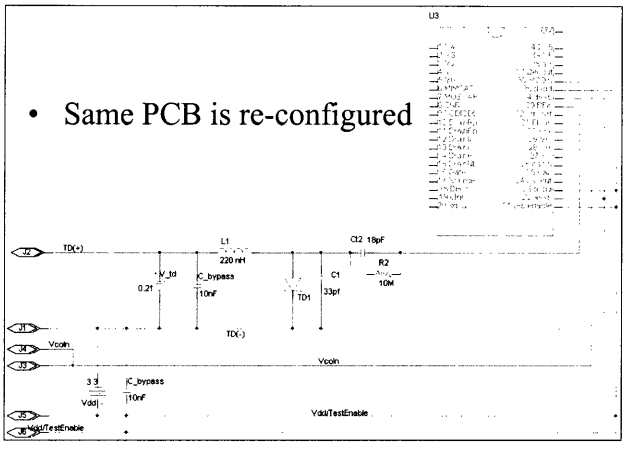
The characteristics of Zetex 933 varactor





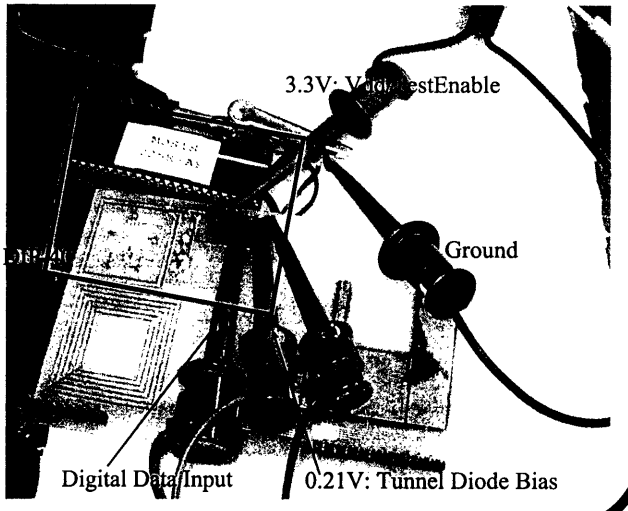
Schematic of FSK Transmitter using SOI IC

- Same PCB is re-configured



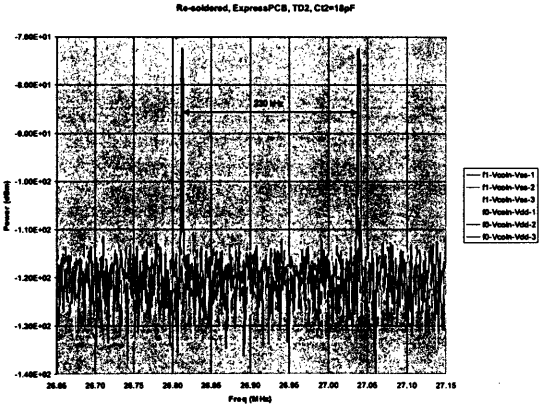
Measurement Setup

- Twisted pairs of wires / shielded wires are used

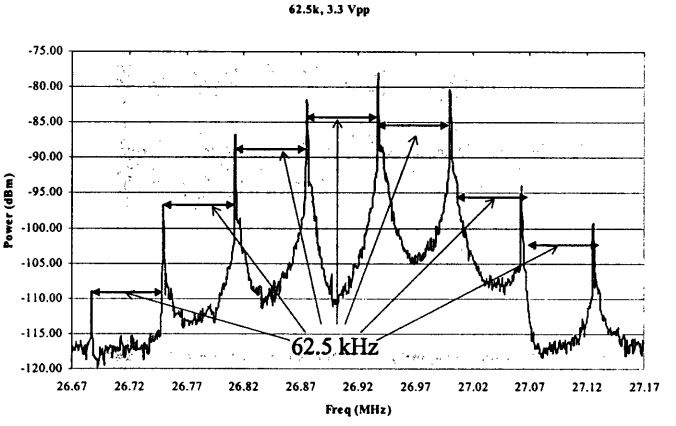


Measurement Results – DC input

- The circuit was tuned to 27.04MHz when the digital input is low
- PMOS capacitance from simulation is 7.5pF @ 27 MHz
- The calculated frequency spacing 410 kHz vs. the measured, 230kHz

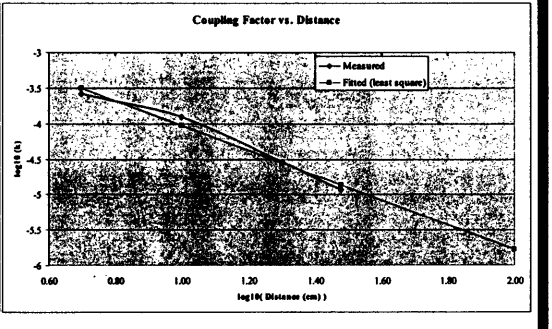


Measurement Results – 125 kbps Input 62.5 kHz Modulation Signal

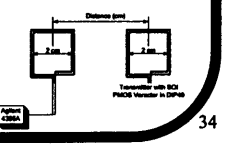


Coupling Factor

Distance (cm)	Measured Power @ 4395A (dBm)	Induced Voltage (μV, rms)	Calculated k
		$10^{\frac{power(dBm)}{10}} \cdot R \cdot 1m W$	$\frac{v_2}{v_1}\sqrt{\frac{L_1}{L_2}}$
5	-71.4	60.0	2.6×10^{-4}
10	-77.9	28.5	1.2×10^{-4}
20	-90.5	6.7	2.9×10^{-5}
30	-98.4	2.7	1.2×10^{-5}



- The coupling factor degrades exponentially with distance

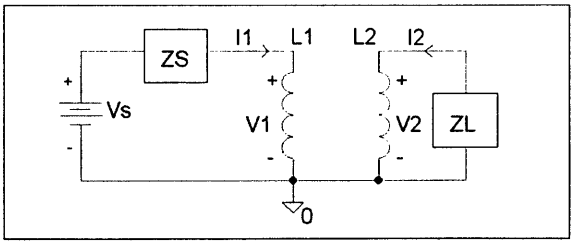


Receiver Pre-Amplifier Design and Test Results

Coupling Impact

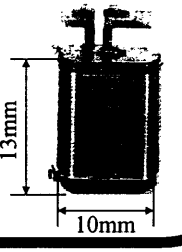
- GMI project targets 1-m distance
- The coupling co-efficient k is $1x10^{-6}$
- No impedance impact between transmitter and receiver

$$Z_1 = \frac{V_1}{I_1} = j\omega L_1 + \frac{\omega^2 k^2 L_1 L_2}{j\omega L_2 + Z_L}$$
$$\cong j\omega L_1, \text{ if } k = 1x10^{-6}$$

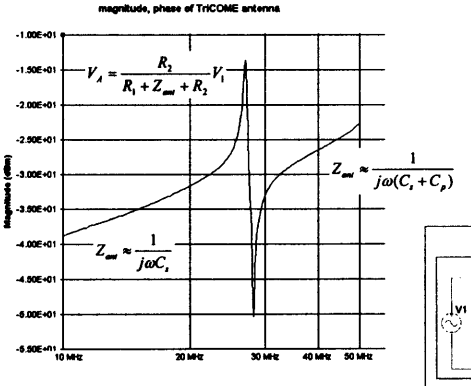


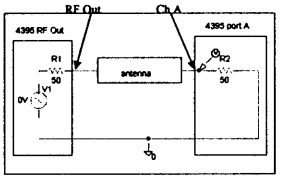
Receiver Antenna

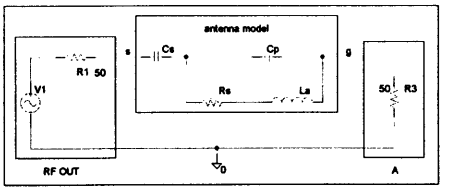
- A commercial ISM 27MHz antenna was selected in receiver design
- A model derived from measurement of its characteristics by
  - Using Anritsu MS4623B Vector Network Measurement System
  - Using Agilent 4395A Network Analyzer



Antenna Model – Agilent 4395A







Antenna Model – Agilent 4395A (Cont')

- The transfer function

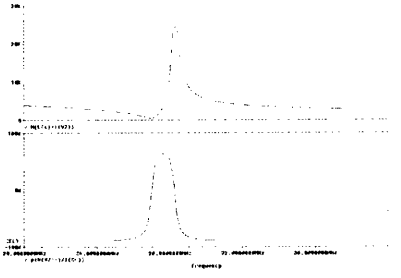
$$H(\omega) \cong \frac{R_1}{R_1 + R_2 + \frac{1}{j\omega C_S} + \frac{1}{j\omega C_P + \frac{1}{j\omega L_a} + \frac{1}{R_P}}}$$

- When L_a resonates with C_p, $H(\omega)$ is minimum $H(\omega) \cong \frac{R_1}{R_P}$
- When L_a resonates with C_p and C_s, $H(\omega)$ is maximum $H(\omega) \cong \frac{1}{2}$

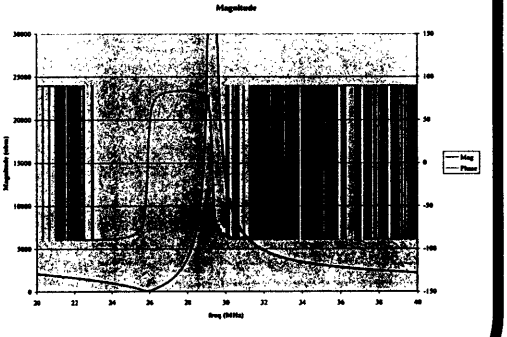
Cs	1.81 pF
Cp	18.4 pF
La	1.71 uH
Rs	4.27 ohm

The Simulated Impedance vs. The Measured Impedance

Impedance simulated from the estimated model

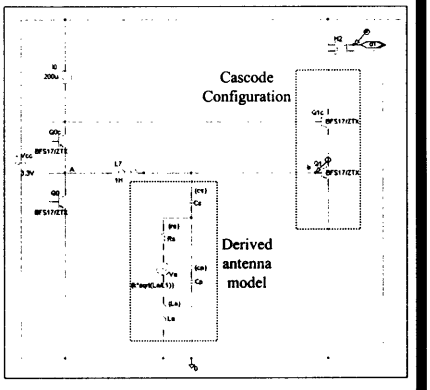


Impedance measured from Anritsu MS4623B VNA



First-stage, Pre-Amplifier Design

- Cascode configuration improves the output impedance
- The derived antenna model and Zetex BFS17N were applied



SNR and Output Impedance

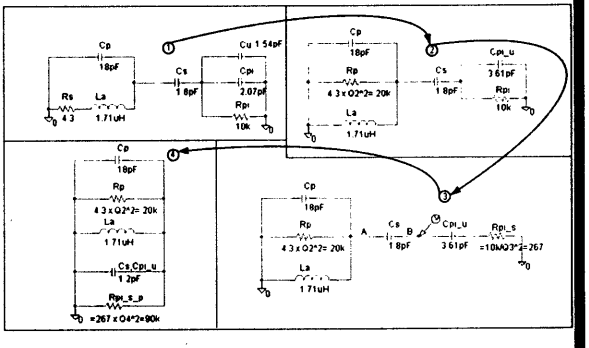
- Q ≈57

$$Q = \frac{R_p \parallel R_{pi\_s\_p}}{\omega L_a}$$

- SNR ≈3

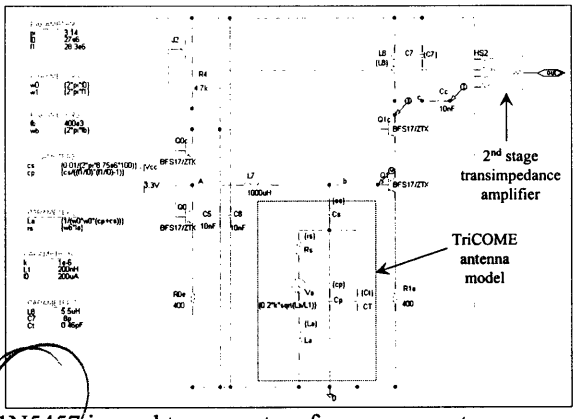
$$(SNR)^2 = \frac{|i_a|^2}{i_n^2} = \frac{\left(k\frac{\beta}{\omega_0\sqrt{L_1 L_2}}|v_i|\right)^2}{2qI_c\beta\cdot\Delta f} = \frac{K^2|v_i|^2}{4\pi\cdot kT\cdot f_{\omega}^2 L_1}$$

- R_{out} 4.7 kohm



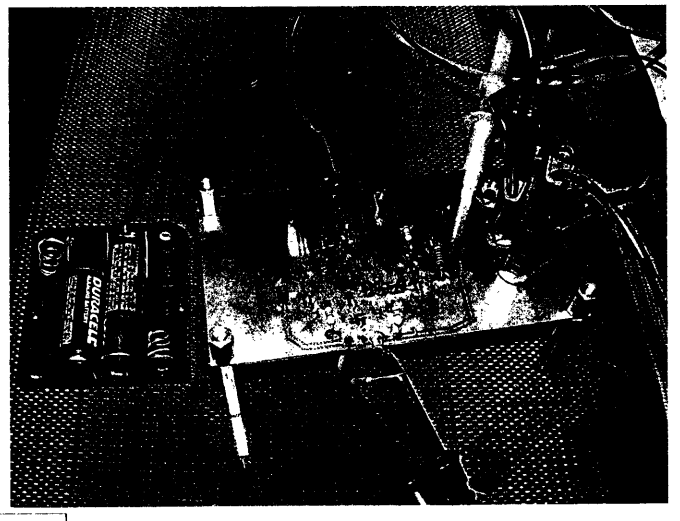
- Bandwidth 450 kHz

Receiver Pre-Amplifier Schematic

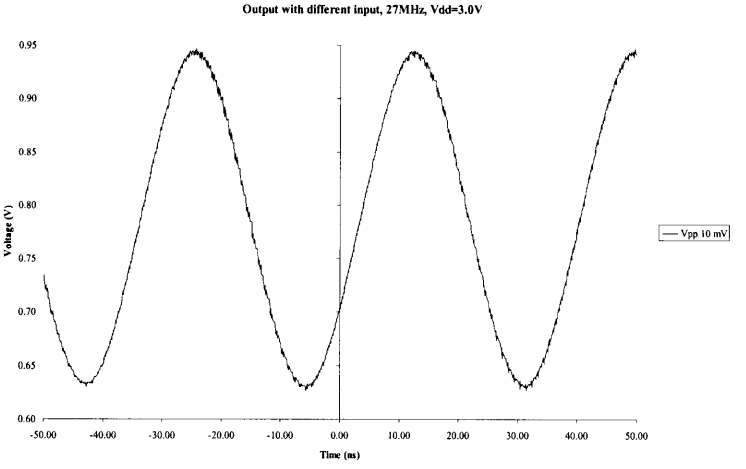


- JFET 1N5457 is used to generate reference current
- Emitter resistors are used to better match for current-mirror
- L8 is used smaller and C7 is used to tune the 2nd-stage

Receiver Pre-Amplifier Test Setup



Tuning and Gain



Conclusions

- The high-temperature transmitter was designed, fabricated and tested
- The inductance of 2-turn, 2-cm square loop antenna was measured
- The parameters of tunnel diode was measured
- The FSK scheme was tested with Si PN varactor and SOI PMOS varactor
- The coupling factor as a function of distance was measured
- The receiver pre-amplifier was designed and fabricated and further measurement will be continued by a senior project

Future Work

- Channel and gate resistance should be minimized
- The size of PMOS and NMOS should be comparable
- The pad for PMOS gate could be digital input pad to reduce the connection when testing transmitter alone
- Ground connection in PCB should be well considered
- A multi-turn loop antenna is worth to try to increase its radiation efficiency
- High-temperature PCB material and discrete components should be explored, or convert them to on-chip devices
- High-temperature transmitter test should be done
- The integration of A/D converter, decimation filter and transmitter should be done
- The entire work should be converted to SiC technology for higher temperature

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