**PROBLEM 5**

An 8-bit analog-to-digital converter (ADC) uses a 5 V reference voltage. What is the accuracy of the converter?

(A) 3.9 mV
(B) 9.8 mV
(C) 20 mV
(D) 250 mV

**SOLUTION 5**

The accuracy of a converter is one-half the value of the least significant bit (LSB). (Sometimes the value of the LSB is called the resolution of the converter and this substitutes for the accuracy. The use of terms is not standard.) The value of the LSB is given by

$$V_{\text{LSB}} = 2^{-n} V_{\text{fs}}$$

The term $n$ is the number of bits in the converter, in this case 8. The full-scale voltage is the reference voltage. Substituting gives

$$V_{\text{LSB}} = 2^{-n} V_{\text{fs}} = (2)^{-8}(5\text{ V}) = 1.95\times10^{-2}\text{ V}$$

One-half of this value is

$$\text{accuracy} = \frac{1}{2}V_{\text{LSB}} = \left(\frac{1}{2}\right)\left(1.95\times10^{-2}\text{ V}\right)$$
$$= 9.75\times10^{-3}\text{ V} \quad (9.8\text{ mV})$$

**The answer is B.**

**PROBLEM 6**

An 8-bit analog-to-digital converter (ADC) has a reference voltage of 10 V. What is the value of the most significant bit (MSB)?

(A) $3.90 \times 10^{-3}$ V
(B) $256 \times 10^{-3}$ V
(C) 5.00 V
(D) 10.0 V

**SOLUTION 6**

The value of the most significant bit in a binary number with $n$-bits is given by

$$V_{\text{MSB}} = \frac{1}{2}V_{\text{fs}} = \left(\frac{1}{2}\right)(10\text{ V}) = 5.00\text{ V}$$

**The answer is C.**

**PROBLEM 7**

A 10-bit digital-to-analog converter (DAC) uses a 5.12 V reference. What is the output voltage for a binary input code of 1011011001?

(A) $5.00 \times 10^{-3}$ V
(B) $723 \times 10^{-3}$ V
(C) $729 \times 10^{-3}$ V
(D) 3.64 V

**SOLUTION 7**

The converter determines the output by assigning an analog value to the code that is obtained in steps. The value of the least significant bit (LSB) determines the minimum size of the steps. The minimum size for a 10-bit converter with a 5.12 V reference is

$$V_{\text{LSB}} = 2^{-n} V_{\text{fs}} = (2)^{-10}(5.12\text{ V}) = 5\text{ mV}$$

The binary coded input is the number of these minimum steps to take. The number corresponding to the binary code is

$$1011011001_2 = (1)(2)^9 + (0)(2)^8 + (1)(2)^7 + (1)(2)^6$$
$$+ (0)(2)^5 + (1)(2)^4 + (1)(2)^3$$
$$+ (0)(2)^2 + (0)(2)^1 + (1)(2)^0$$
$$= 729_{10}$$

Thus, 729 steps of 5 mV are taken to convert this input signal. The output voltage is

$$V_{\text{out}} = (729)(5\text{ mV}) = 3645\text{ mV} \quad (3.64\text{ V})$$

Note that the output voltage of any DAC can be represented as

$$V_{\text{out}} = \left(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}\right)V_{\text{fs}} \quad b_i \in \{0, 1\}$$

The full-scale (or reference) voltage is given by $V_{\text{fs}}$. The total number of bits is represented by $n$. The value of the bits, $b_i$, is either 0 or 1. The 2s are the weighting factors.

**The answer is D.**

# Diode Circuits

**PROBLEM 4**

The manufacturing data for a discrete silicon diode shows a reverse saturation current of 1 nA and an experimentally determined coefficient, $\eta$, of 2. The diode is forward biased at 0.7 V. What is the expected current as the diode just becomes forward biased?

(A) $10^{-9}$ mA
(B) 0.7 mA
(C) 1.8 mA
(D) 24 mA

**SOLUTION 4**

The governing equation for practical diodes is

$$I = I_s\left(e^{\frac{V}{\eta V_T}} - 1\right)$$

(The minus 1 term is insignificant and often neglected.)

Substitute the given information and the known value of the thermal voltage at a room temperature of 0.026 V (see Prob. 3).

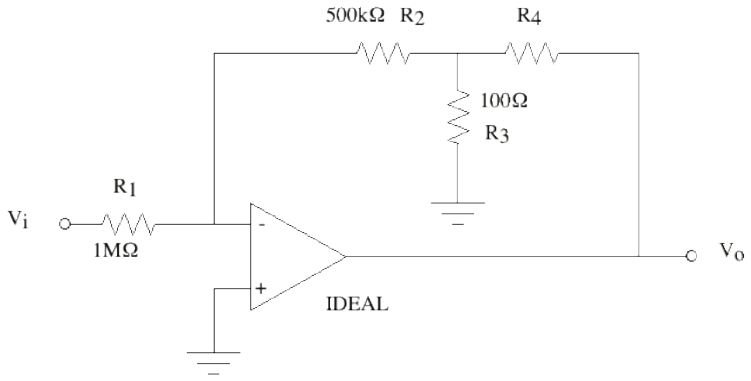
$$I = \left(1\times10^{-9}\text{ A}\right)\left(e^{\frac{0.7\text{ V}}{(2)(0.026\text{ V})}} - 1\right) = 7.02\times10^{-4}\text{ A}\ \ (0.7\text{ mA})$$

**The answer is B.**

## Operational Amplifiers

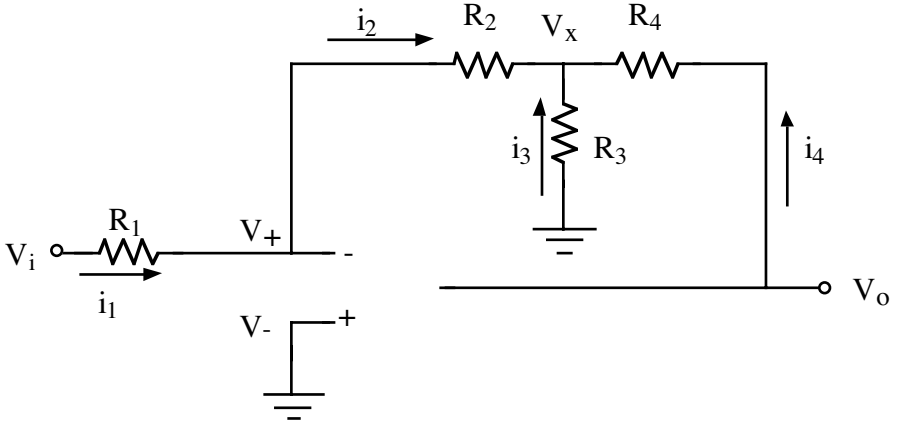
2. Determine the voltage gain $V_o/V_i$ in the circuit shown below. Assume the operational amplifier is ideal. You may use R4=24kΩ.

$V_o/V_i$ = _____ ANSWER: -120.5




ANSWER:

There are multiple ways to solve the problem. The key is that by KCL and the virtual short assumption the voltage at the junction of R2, R3 and R4 is actually known. Once this is known Vo can be readily calculated using KCL.




Using the virtual short assumption, since $v_{in-}$ is grounded $v_{in+}$ is also at ground potential, i.e., $v_{in-} = 0$

Since $v_{in-} = 0$, the input current through R1 is given by $i_1=v_i/R_1$.

Using KCL at the – input of the op amp and recognizing that no current can flow into the op amp we have that $v_x=-i_2R_2$ where $i_2=i_1$ and $v_x$ is the voltage at the node formed by $R_2$, $R_3$ and $R_4$.

If we know $v_x$ we can write $i_3=-v_x/R_3$ and $i_4=(v_x-v_o)/R_4$ . Using Kirchhoff's current law at this

node we have $i_2 + i_3 + i_4 = 0$ which gives

$$\frac{v_x - v_o}{R_4} = \frac{-v_x}{R_2} + \frac{-v_x}{R_3} \qquad (1)$$

Substituting for the actual circuit values gives

$$\frac{v_x - v_o}{24{,}000\Omega} = \frac{-v_x}{500{,}000\Omega} + \frac{-v_x}{100\Omega}$$

We know $v_x$ in terms of $v_i$ from the input node where $\frac{v_i - v_+}{R_1} = \frac{v_+ - v_x}{R_2}$

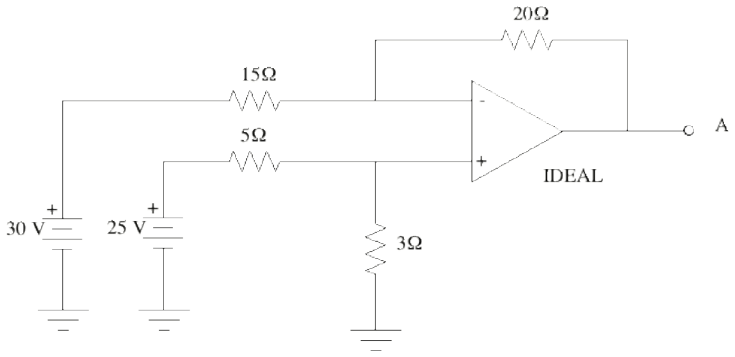
And, using the given circuit values becomes $\frac{v_i - 0}{1{,}000{,}000\Omega} = \frac{0 - v_x}{500{,}000\Omega}$

which can be solved to give $v_x = -\frac{v_i}{2}$. Substituting this value into equation (1) gives

$$-\frac{v_i}{48{,}000} + \frac{-v_o}{24{,}000\Omega} = +\frac{v_i}{1{,}000{,}000} + \frac{v_i}{200}$$

Combining terms gives $\frac{-v_o}{24{,}000\Omega} = \frac{v_i}{199.13}$ or $\frac{v_o}{v_i} = -\frac{24{,}000}{199.13} = -120.52$

4. For the difference amplifier circuit shown, determine the output voltage at terminal A.




(A) - 18.13 V
(B) -6.07 V
(C) 6.07 V
(D) 15.45 V

**Solution:**

By voltage division,

$$v_{in+} = 25V\left(\frac{3\Omega}{5\Omega + 3\Omega}\right) = 9.375V$$

By the virtual short circuit between the input terminals, $v_{in-} = 9.375$ V
Using **Ohm's** law, the current through the 15 Ω resistor is

$$I_{15} = \left(\frac{30V - 9.375V}{15\Omega}\right) = 1.375A$$

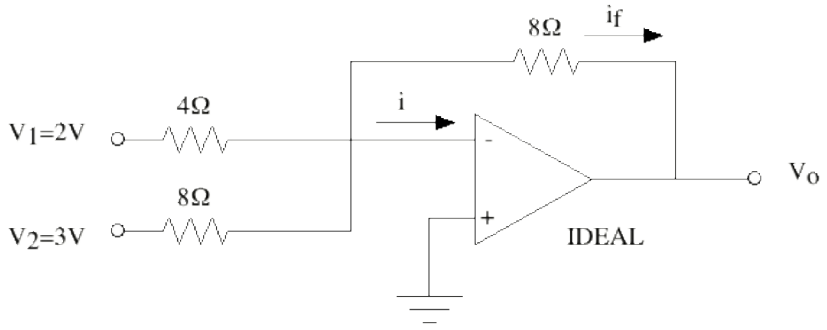
The input impedance is infinite; therefore, $I_{in-}=0$ and $I_{15}=I_{20}$.

Use Kirchoff's voltage law to find the output voltage at A.

$v_A=v_{in-} - 20I_{20} = 9.375$ V - (20Ω)(1.375 A) = -18.125 V

Answer is A.

Problems 2 and 3 refer to the following figure.




2. What is the current, i?

(A) -0.88 A
(B) -0.25 A
(C) 0 A
(D) 0.25 A

**Solution** 2:

The input current in an op amp is so small that it is assumed to be zero.

Answer is C.

3. What is the output voltage, $v_o$?

(A) -7 V
(B) -6 V
(C) -1 V
(D) 6 V

**Solution 3:**

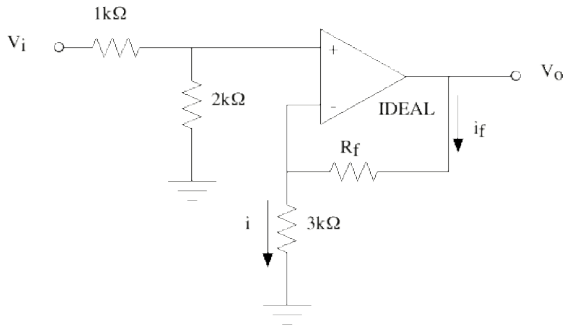
This op amp circuit is a summing amplifier. Since i=0,

$$i_f = \frac{v_1}{R_1} + \frac{v_2}{R_2} = \frac{3\text{ V}}{8\ \Omega} + \frac{2\text{ V}}{4\ \Omega} = 0.875\text{ A}$$

$v_o = -i_f R_f = -(0.875\text{ A})(8\ \Omega) = -7\text{ V}$

Answer is A.

4. For the ideal op amp shown, what should be the value of resistor $R_f$ to obtain a gain of 5?




(A) 12.0 kΩ
(B) 19.5 kΩ
(C) 22.5 kΩ
(D) 27.0 kΩ

**Solution:**

By voltage division, $v_{in+} = v_i\left(\frac{2k\Omega}{3k\Omega}\right) = \frac{2}{3}v_i$

By the virtual short circuit, $v_{in-} = v_{in+} = \frac{2}{3}v_i$

$$i = \frac{v_{in-}}{3k\Omega} = \frac{\frac{2}{3}v_i}{3k\Omega}$$

Since the op amp draws no current, $i_f$=i

$$\frac{v_o - v_{in-}}{R_f} = \frac{\frac{2}{3}v_i}{3k\Omega}$$

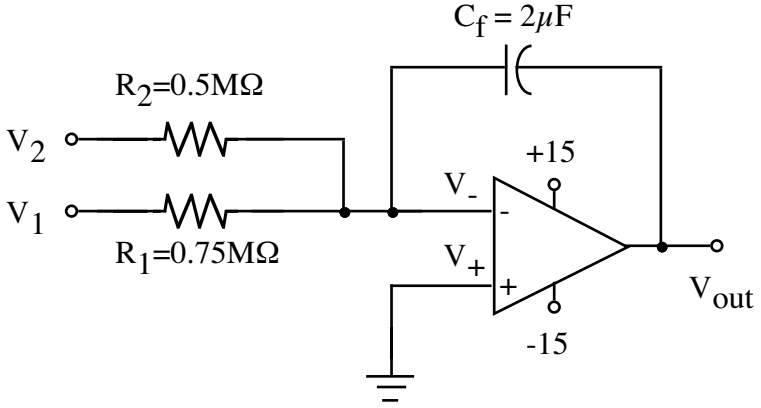
But, $v_o = 5v_i$.

$$\frac{5v_i - \frac{2}{3}v_i}{R_f} = \frac{\frac{2}{3}v_i}{3k\Omega}$$

$$\frac{\frac{13}{3}}{R_f} = \frac{\frac{2}{3}}{3k\Omega}$$

$R_f$=19.5 kΩ, Answer is B.

14. For the circuit shown below, $V_1 = 10\sin(200t)$ and $V_2 = 15\sin(200t)$. What is $V_{out}$? The op amp is ideal with infinite gain.




ANSWER:

Any problem with a capacitor (or inductor) in it and sinusoidal voltages immediately indicates that $V_1$ and $V_2$ should be represented as phasors, and $C_f$ should be replaced by an impedance. This circuit is most easily solved using the virtual short assumption ($V_+=V_-$), and using KCL at the inverting input. Since $V_+$ is grounded $V_-=0$.

$$\frac{V_2 - 0}{R_2} + \frac{V_1 - 0}{R_1} - \frac{0 - V_{out}}{1/j\omega C} = 0.$$

Rationalizing this expression gives $+\frac{V_2}{R_2} + \frac{V_1}{R_i} + j\omega C V_{out} = 0$.

Solving for $V_{out}$ gives $V_{out} = -\frac{V_2}{j\omega C R_2} - \frac{V_1}{j\omega C R_i}$

It is important to recognize that all sine functions should always be converted to cosines for proper phase in the phasor expressions, i.e. $\sin(200t) = \cos(200t - 90°) \leftrightarrow 1\angle -90° = -j$

Using the circuit parameters given,

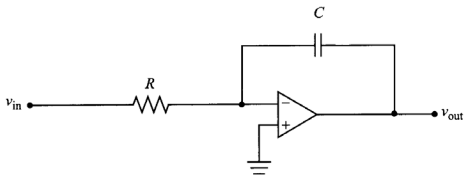
$$V_{out} = -\frac{-j15}{(200)(2\times 10^{-6})(0.5\times 10^{6})} - \frac{-j10}{(200)(2\times 10^{-6})(0.75\times 10^{6})}$$

$$= \frac{15}{200} + \frac{10}{300} = \frac{3}{40} + \frac{1}{30}$$

The answer is then $V_{out}(t) = \left(\frac{3}{40} + \frac{1}{30}\right)\cos(200t)$

**PROBLEM 13**

Consider the operational amplifier circuit shown. What is the function of the circuit?




(A) amplification
(B) differentiation
(C) integration
(D) multiplication

**SOLUTION 13**

Assuming an ideal op amp, KCL can be written at the inverting terminal as

$$\frac{0\text{ V}-v_{in}}{R}+i_C=0$$

$$\frac{0\text{ V}-v_{in}}{R}+C\left(\frac{d(0\text{ V}-v_{out})}{dt}\right)=0$$

Rearranging for an expression of the output voltage gives

$$C\left(\frac{d(0\text{ V}-v_{out})}{dt}\right)=-\frac{0\text{ V}-v_{in}}{R}=\frac{v_{in}}{R}$$

$$-C\left(\frac{dv_{out}}{dt}\right)=\frac{v_{in}}{R}$$

$$dv_{out}=\left(-\frac{1}{RC}\right)v_{in}dt$$

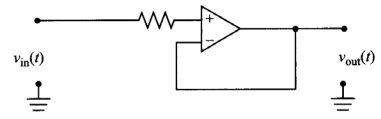
$$v_{out}=\left(-\frac{1}{RC}\right)\int v_{in}dt$$

The op amp circuit is designed to accomplish integration.

**The answer is C.**

**PROBLEM 11**

Operational amplifiers can be used to isolate sections of instrumentation to avoid undesirable interactions between circuits. One such circuit is as follows. What is the common name for the circuit shown?




(A) differential amplifier
(B) noninverting amplifer
(C) simple amplifier
(D) voltage follower

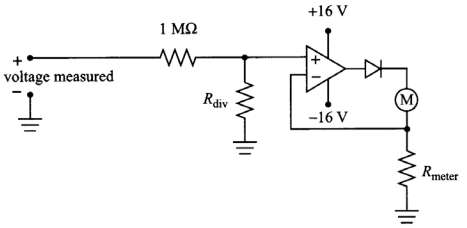
**SOLUTION 11**

The op amp shown is configured such that the input is amplified and fed directly to the negative terminal of the amplifier. This, in effect, causes the output to follow the input, hence the name *voltage follower*. (The configuration is used to buffer the input circuitry from that connected to the output. That is, the impedance of the input is not seen by the output circuitry. In fact, ideally, the output impedance is zero.)

**The answer is D.**

## PROBLEM 7

An electronic voltmeter using a d'Arsonval meter display is shown. The full-scale meter current is 0.1 mA. The voltmeter reads 250 $V_{rms}$. To ensure linear operation, the op amp input and output are restrained to operate a minimum of 3 V from the rail voltages (power supply voltages).




**7.1** What approximate value of divider resistance, $R_{div}$, is necessary to ensure linear operation?

(A) 40 kΩ
(B) 50 kΩ
(C) 55 kΩ
(D) 1000 kΩ

## SOLUTION 7

**7.1** The op amp will respond to the instantaneous values of the voltage. The relationship between the peak voltage and the root-mean-square voltage for a sinusoidal voltage is

$$|V_{peak}| = \sqrt{2}V_{rms} = 1.414V_{rms}$$
$$|V_{peak}| = (\sqrt{2})(250\text{ V}) = 353.55\text{ V}$$

The op amp is not able to follow the input voltage more than 13 V (positive or negative). Choose to make the op amp input peak voltage of 13 V (which is 3 V less than the power supply voltage needed to ensure linear operation) correspond to the peak voltage (both positive and negative) of 353.55 V, that is, 250 $V_{rms}$. The voltage divider shown attached to the positive terminal accomplishes the adjustment if the value of $R_{div}$ is

$$(353.55\text{ V})\left(\frac{R_{div}}{R_{div}+1\times10^6\ \Omega}\right) = 13\text{ V}$$
$$(353.55\text{ V})R_{div} = (13\text{ V})(R_{div}+1\times10^6\ \Omega)$$
$$= (13\text{ V})(R_{div}+13\times10^6\text{ V}\cdot\Omega)$$
$$(353.55\text{ V})R_{div} - (13\text{ V})R_{div} = 13\times10^6\text{ V}\cdot\Omega$$
$$R_{div}(353.55\text{ V} - 13\text{ V}) = 13\times10^6\text{ V}\cdot\Omega$$
$$R_{div} = \frac{13\times10^6\text{ V}\cdot\Omega}{340.55\text{ V}}$$
$$= 3.8\times10^6\ \Omega\ \ (40\text{ k}\Omega)$$

**The answer is A.**

**7.2** What approximate value of meter resistance, $R_{meter}$, is required if the op amp uses the entire linear voltage range?

(A) 52 Ω
(B) 82 Ω
(C) $41\times10^3$ Ω
(D) $102\times10^3$ Ω

**7.2** The full-scale meter current is given as 0.1 mA. Given that the meter is a d'Arsonval meter, this is the average current. (DC meters, such as the d'Arsonval, respond to the average current through them, hence their inability to measure AC currents without rectification.) The current output of the op amp is half-wave rectified by the indicated diode. The average value of a full-wave rectified signal is $2/\pi$ of the peak value. For half-wave rectification, which has a period twice that of full-wave rectification, the average value is $1/\pi$ of the peak value. Thus,

$$I_{meter,peak} = (0.1\text{ mA})\pi = 0.314\text{ mA}$$

0.314 mA is the current through the meter resistor, $R_{meter}$, at which 13 V must be developed at the negative input. This value matches the 13 V at the positive terminal that develops at the peak input voltage of 353.55 V (250 $V_{rms}$). Using Ohm's law on the meter resistor gives

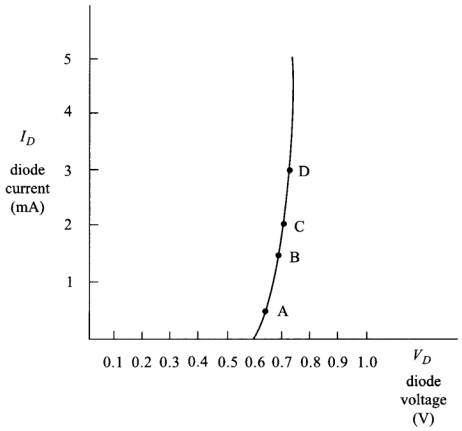
$$V_{meter} = I_{meter}R_{meter}$$
$$R_{meter} = \frac{V_{meter}}{I_{meter}} = \frac{13\text{ V}}{0.314\times10^{-3}\text{ A}}$$
$$= 41{,}400\ \Omega\ \ (41\times10^3\ \Omega)$$

Note that this problem essentially determines the average current flowing through a meter as a function of the rms value of a pure sinusoidal input voltage. Thus, the scale factors for the meter can be determined from the calculated information.

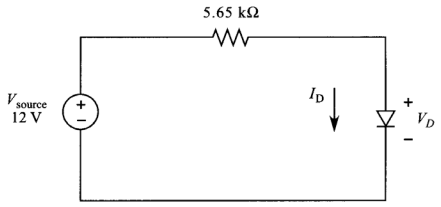
**The answer is C.**

**PROBLEM 8**

Consider the diode operating characteristic shown.




The diode is used in the indicated circuit.




What is the quiescent operating point (Q-point)?

(A) point A
(B) point B
(C) point C
(D) point D

**SOLUTION 8**

Using KVL around the given circuit results in the following equation.

$$V_{source} = I_D R + V_D$$

Substituting the known values gives the load line equation.

$$12\text{ V} = \left(5.65\times10^3\ \Omega\right)I_D + V_D$$

Such an equation can be used to find the load line for the particular circuit. Since two points are required to define a line, let $V_D = 0$ V and $I_D = 0$ A. For $V_D = 0$ V, the resulting point is

$$12\text{ V} = \left(5.65\times10^3\ \Omega\right)I_D + V_D = \left(5.65\times10^3\ \Omega\right)I_D + 0\text{ V}$$

$$I_D = \frac{12\text{ V}}{5.65\times10^3\ \Omega} = 2.12\times10^{-3}\text{ A} = 2.12\text{ mA}$$

This gives a point (0.00, 2.12) on the graph.

For $I_D = 0$ A, the resulting point is

$$12\text{ V} = \left(5.65\times10^3\ \Omega\right)I_D + V_D = \left(5.65\times10^3\ \Omega\right)(0\text{ A}) + V_D$$

$$V_D = 12\text{ V}$$

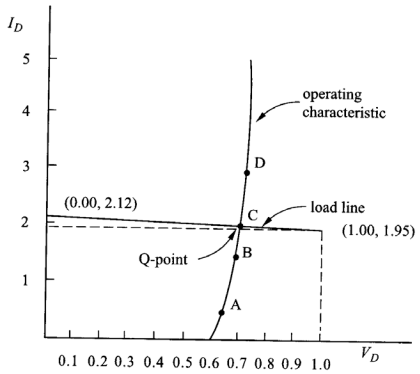
This gives a point (0, 12) that is off the graph. Since any point can be used, let $V_D = 1.0$ V to ensure a point of $I_D$ will be found that will plot on the graph. The resulting point is

$$12\text{ V} = \left(5.65\times10^3\ \Omega\right)I_D + V_D = \left(5.65\times10^3\ \Omega\right)I_D + 1.0\text{ V}$$

$$I_D = \frac{11\text{ V}}{5.65\times10^3\ \Omega} = 1.95\times10^{-3}\text{ A} \quad (1.95\text{ mA})$$

This gives a point (1.00, 1.95) on the graph.

Plotting both these points results in the following.

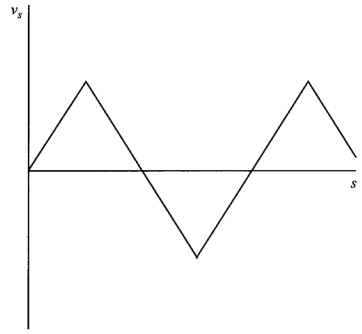



The Q-point is at point C. The point C is (0.7, 2.0), which is a solution to the load line equation.

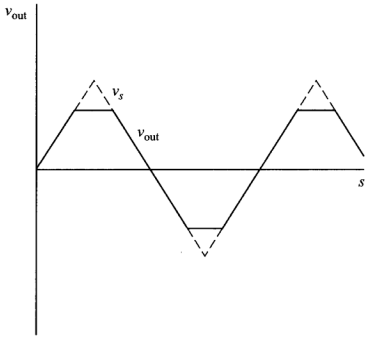
**The answer is C.**

**PROBLEM 9**

A voltage source produces a triangular wave shape as shown.

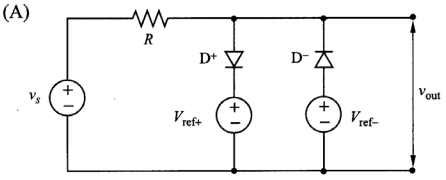



An output wave shape of the indicated form is desired.

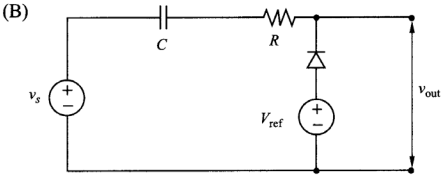



Consider the four circuits shown. Which of the indicated circuits can provide the desired output?

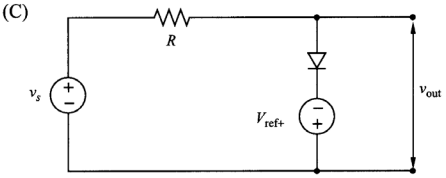
(A)



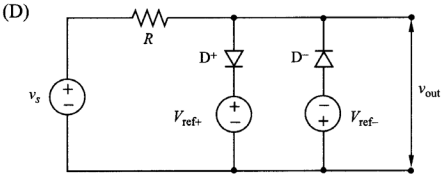

(B)




(C)




(D)




**SOLUTION 9**

A clipping (limiting) circuit that clamps the voltage on both the positive and negative portion of the cycles is needed. Thus, only choices (A) and (D) are possibilities.

Consider both the figures for choices (A) and (D). During the positive half cycle, diode $D^+$ (associated with $V_{ref+}$) conducts once the source voltage is greater than the reference voltage. This means that in a portion of the positive half-cycle, the diode $V_{ref+}$ conducts, thus limiting the voltage drop to the reference value. Diode $D^-$ (associated with $V_{ref-}$) is reverse-biased and does not conduct.

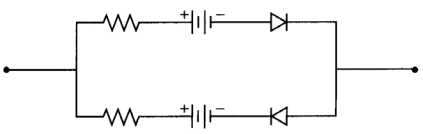
Consider the negative half-cycle. In choice (A), diode $D^-$ conducts almost immediately, thus clamping the output voltage to near zero. In choice (D), diode $D^-$ conducts once the source voltage is less than the reference voltage. Or, one can say that diode $D^-$ conducts when it overcomes $V_{ref-}$. (A symmetrical wave is generated when $|V_{ref+}| = |V_{ref-}|$.)

**The answer is D.**

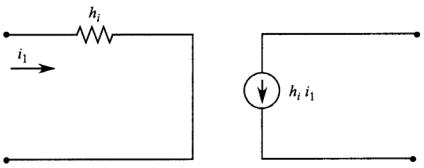
**PROBLEM 10**

Consider the electronic circuit models shown. Note that identifying subscripts have been removed. Which of these models represents a field-effect transistor?

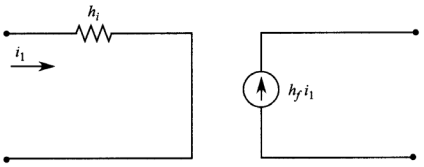
(A)



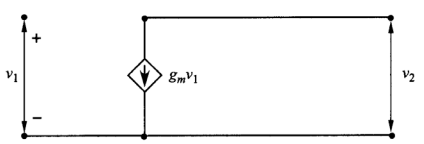
(B)




(C)




(D)




**SOLUTION 10**

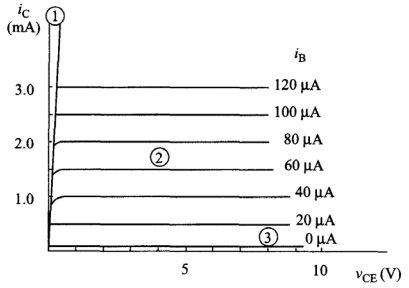
The figure in choice (A) is the piecewise linear model for a diode. The figure in choice (B) is an *h*-parameter, small-signal, simplified equivalent circuit for a common-emitter bipolar junction transistor (BJT). The figure in choice (C) is an *h*-parameter, small-signal, simplified equivalent circuit for a common-collector BJT. The figure in choice (D) is a simplified model of a field-effect transistor. (The simplifications in each model consist of ignoring parameters that are insignificant, for example, extremely small reverse currents or near-infinite parallel resistance.)

**The answer is D.**

# Transistors - BJTs

**PROBLEM 11**

Consider the following figure of the characteristics of a bipolar junction transistor (BJT) configured as a common emitter.




**11.1** The bipolar junction transistor (BJT) whose characteristics are shown is to be used in a TTL (transistor-transistor logic) circuit. What operating region(s) will be utilized?

(A) 1
(B) 2
(C) 3
(D) 1 and 3

**SOLUTION 11**

**11.1** Logic circuits require the transistor to operate as a switch, thereby providing two outputs (logic 0 and logic 1). Logic circuit operation requires the transistor to operate between the saturation region (1) and the cutoff region (3).

**The answer is D.**

**11.2** What region of operation is an *npn* transistor using if $V_{BE} = 0.75$ V and $V_{BC} = -0.70$ V?

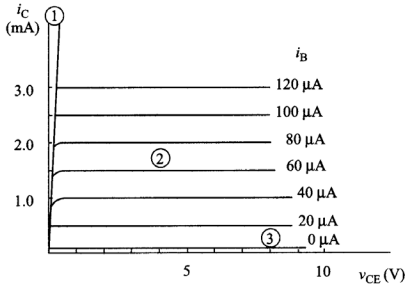
(A) forward-active
(B) saturation
(C) reverse-active
(D) cutoff

**11.2** The given voltages indicate that the base-emitter (pn) junction is forward-biased and the base-collector (pn) junction is reverse-biased. This places the transistor in the forward-active region (or normal-active region) that is used when amplification of the input signal is the main goal.

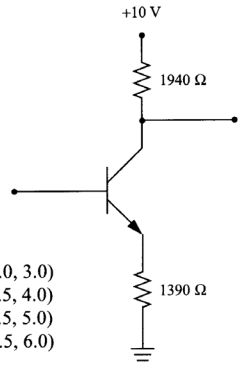
**The answer is A.**

## PROBLEM 11

Consider the following figure of the characteristics of a bipolar junction transistor (BJT) configured as a common emitter.



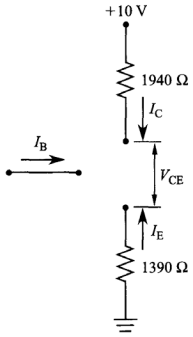

**11.3** A transistor with the characteristics given is used as part of an amplification circuit. The portion of the circuit of interest is shown. What is the circuit's Q-point, in terms of ($I_C$, $V_{CE}$), if the base current is 60 μA?




(A) (1.0, 3.0)
(B) (1.5, 4.0)
(C) (1.5, 5.0)
(D) (2.5, 6.0)

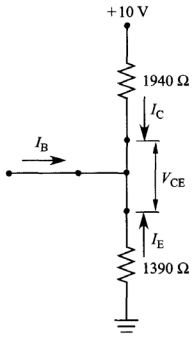
## SOLUTION 11

**11.3** The Q-point is found graphically, in this case, by determining the load line. Redraw the circuit with the transistor open circuited (that is, with $I_C = 0$ V).




Performing KVL in the collector loop, or by inspection, reveals that $V_{CE} = 10$ V. This provides a point (0.0, 10) on the characteristic graph.

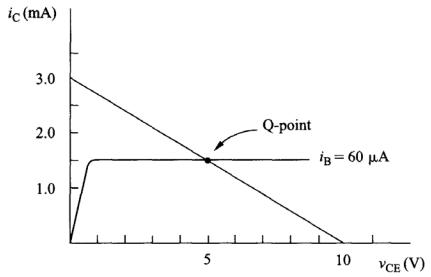
Redraw the circuit with the transistor short-circuited (that is, with $V_{CE} = 0$ V).




The collector current is determined from Ohm's law.

$$I_C = \frac{V_{CC}}{R_C + R_E} = \frac{10\text{ V}}{1940\ \Omega + 1390\ \Omega} = 3.00\times10^{-3}\text{ A}$$

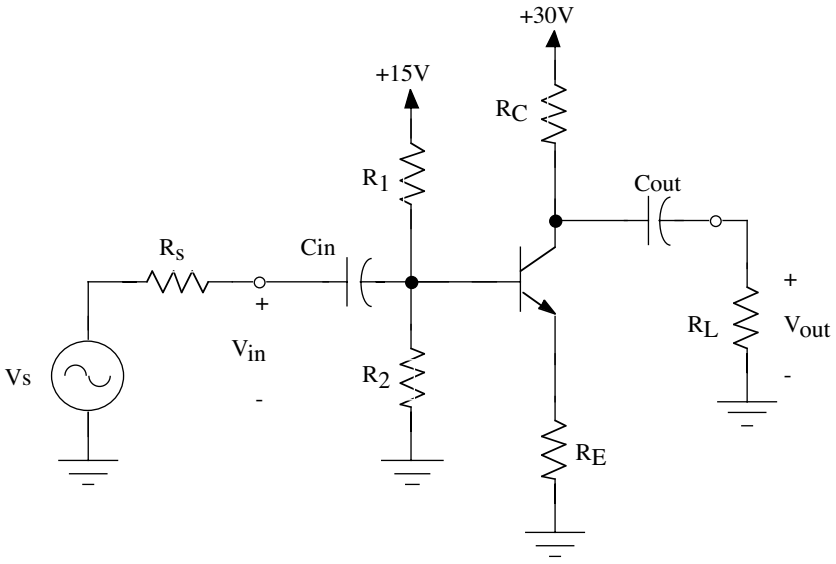
This provides a point (3.0, 0) on the characteristic graph. Plotting both the calculated points and connecting the two gives the load line.




The Q-point is then determined as (1.5, 5).

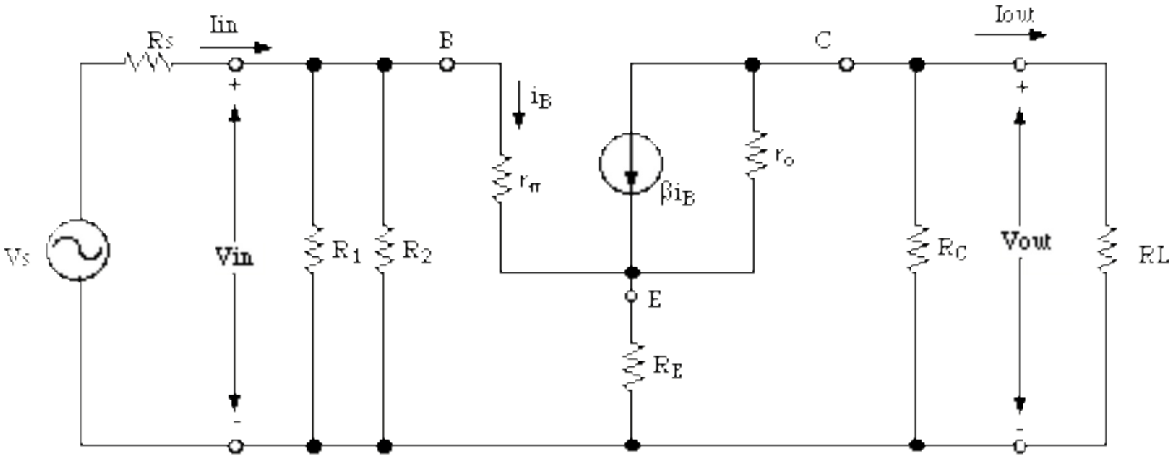
**The answer is C.**

4. SMALL SIGNAL BJT ANALYSIS




Consider the above BJT amplifier where $R_S$=500Ω, $R_1$=10kΩ, $R_2$=10kΩ, $R_E$=2000Ω, $R_L$=10kΩ and Rc=5kΩ. The transistor is characterized by β=100. The amplifier is biased such that $I_{C,Q}$=3.3mA. You may assume that $C_{IN}$ and $C_{OUT}$ have a low impedance at mid-frequency and that $r_o$ is so large it can be neglected.
(a) Draw the small-signal equivalent circuit for this BJT small signal amplifier at mid-frequency. Indicate the values of all small signal parameters in your circuit.
(b) Calculate $R_{in}$ for this amplifier.
(c) What is the voltage gain $A_v$ for this amplifier.

ANSWER:
(a)




All small signal circuit parameters except $r_\pi$ are known. $r_o$ can be neglected. $r_\pi$ can be calculated as $r_\pi = \dfrac{\beta V_T}{I_{C,Q}} = \dfrac{(100)(26mV)}{(3.3mA)} = 788\Omega$

(b) Normally you assume that the bias resistor equivalent resistance $R_B = R_1 \,||\, R_2 = \dfrac{(R_1)(R_2)}{R_1 + R_2} = \dfrac{(10k\Omega)(10k\Omega)}{10k\Omega + 10k\Omega} = 5k\Omega$ is so large that it can be neglected. That was not true in this problem since it is only 5000 ohms. We continue to use the definition of input resistance $R_{in} = \dfrac{V_{in}}{I_{in}}$. The input current is now calculated as $I_{in} = \dfrac{V_{in}}{R_1 \,||\, R_2} + i_B$. The corresponding input voltage can be calculated as $V_{in} = i_B r_\pi + (\beta + 1) i_B R_E = i_B \left(r_\pi + (\beta + 1) R_E\right)$. Solving for $i_B$ gives $i_B = \dfrac{V_{in}}{r_\pi + (\beta + 1) R_E}$ which can be substituted into the expression for $V_{in}$ to give $I_{in} = \dfrac{V_{in}}{R_1 \,||\, R_2} + \dfrac{V_{in}}{r_\pi + (\beta + 1) R_E}$. Using this expression in that for $R_{in}$ gives $R_{in} = \dfrac{V_{in}}{I_{in}} = \dfrac{V_{in}}{\dfrac{V_{in}}{R_1 \,||\, R_2} + \dfrac{V_{in}}{r_\pi + (\beta + 1) R_E}} = \dfrac{1}{\dfrac{1}{R_1 \,||\, R_2} + \dfrac{1}{r_\pi + (\beta + 1) R_E}}$ which can be recognized as

$R_{in} = \left(R_1 \,||\, R_2\right) || \left(r_\pi + (\beta + 1) R_E\right)$.

Numerically this gives $R_{in} = (5k\Omega) \,||\, \left(788 + (100 + 1) 2000\right) = (5k\Omega) \,||\, (202788\Omega) = 4880\Omega$.

(c) Note that $i_B$ is independent of $R_{in}$ and is given by $i_B = \dfrac{V_{in}}{r_\pi + (\beta + 1) R_E}$. The collector current is then $i_C = \beta i_B = \beta \dfrac{V_{in}}{r_\pi + (\beta + 1) R_E} = \dfrac{\beta}{r_\pi + (\beta + 1) R_E} V_{in}$. The output voltage is then $V_{out} = -i_C \left(R_C \,||\, R_L\right) = -\dfrac{\beta}{r_\pi + (\beta + 1) R_E} V_{in} \left(R_C \,||\, R_L\right)$. Solving for the voltage gain gives $\dfrac{V_{out}}{V_{in}} = -\dfrac{\beta \left(R_C \,||\, R_L\right)}{r_\pi + (\beta + 1) R_E}$.

Numerically,

$$\frac{V_{out}}{V_{in}} = -\frac{\beta \left(R_C \,||\, R_L\right)}{r_\pi + (\beta + 1) R_E} = -\frac{100(5000\Omega \,||\, 10000\Omega)}{788\Omega + (100 + 1) 2000\Omega} = -1.64$$

10. An amplifier in the configuration of figure 8.45 has $R_1 = 6K\,\Omega$, $R_2 = 3K\,\Omega$, $R_e = 1K\,\Omega$, $R_s = 1K\,\Omega$, and $R_L = 833\,\Omega$. With $h_{fe} = 500\,\Omega$, $\beta = 50$ and $r_e = 5K\,\Omega$, determine the amplifier voltage gain.

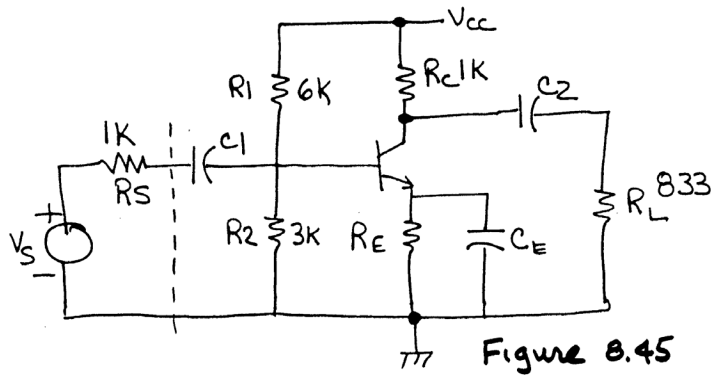
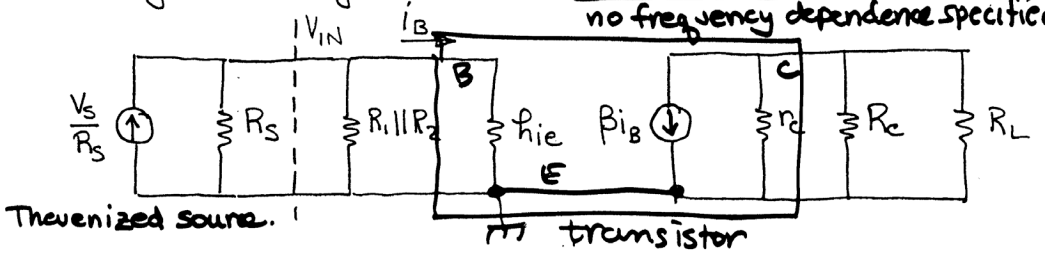



Figure 8.45

Drawing small signal model at mid-band
no frequency dependence specified.



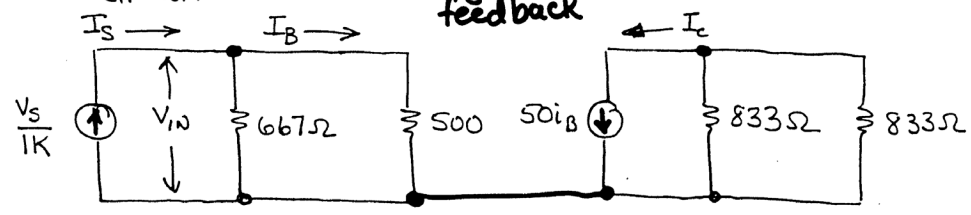

$$R_1 \| R_2 = \frac{(6)(3)}{6+3} = 2k$$

$$R_s = 1k$$

$$R_s \| R_1 \| R_2 = \frac{2 \cdot 1}{2+1} = 667\Omega$$

$$r_c \| R_c = (5000) \| (1000) = \frac{5 \cdot 1}{5+1} = 833\Omega$$

Simplified circuit is then; neglects feedback



Typically have voltage divider with input impedance.

$$V_{IN} = \underbrace{\frac{V_S}{1K}}_{\text{input current}} \underbrace{\frac{667 \times 500}{667 + 500}}_{\text{two resistances in parallel}} = 0.286\ V_S$$

This is amplifier INPUT voltage.

$$I_B = \underbrace{\frac{667}{667 + 500}}_{\text{current divider}} \frac{V_S}{1K} = 5.716 \times 10^{-4}\ V_S$$

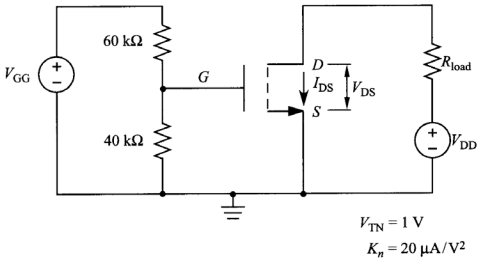
$$V_{OUT} = -(50 I_B)(833 \| 833) = -11.90\ V_S$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-11.90\ V_S}{0.286\ V_S} = -41.6$$

# Transistors - FETS

**PROBLEM 12**

Consider the following figure of a MOSFET.




**12.1** What type of device is the MOSFET?

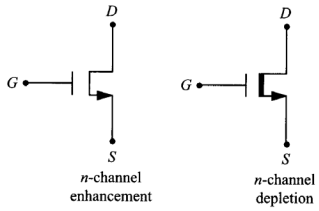
(A) *n*-channel enhancement
(B) *n*-channel depletion
(C) *p*-channel enhancement
(D) *p*-channel depletion

**12.2** What is the gate-source voltage, $V_{GS}$, for the indicated configuration if the gate supply voltage, $V_{GG}$, is 10.0 V?

(A) 0 V
(B) 0.3 V
(C) 0.7 V
(D) 4.0 V

**SOLUTION 12**

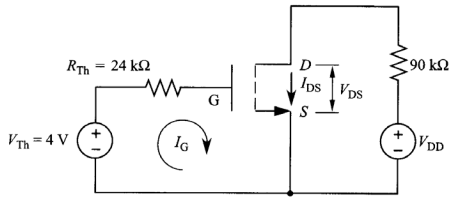
**12.1** The dashed line on the MOSFET indicates an *enhancement* device. Some symbology uses a single connected line for an enhancement device and a thicker line for a depletion device. The thicker line is meant to indicate that a channel is already present. The alternate symbology is shown.




The arrow indicates the direction of conventional current flow. Thus, the current flows from the drain to the source. That is, positive charges flow from the drain to the source, meaning that negative charges flow from the source (the source of the majority charges) to the drain. The channel is composed of these negative charges, that is, this is an *n-channel* device.

**The answer is A.**

**12.2** Obtain the Thevenin equivalent of the gate-source circuit.




Next write the KVL around the gate loop as indicated.

$$V_{Th} - I_G R_{Th} - V_{GS} = 0$$

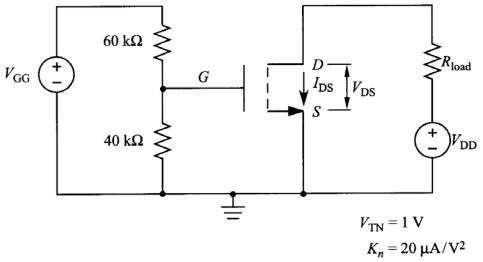
The gate current in a MOSFET is zero amperes. Thus,

$$V_{GS} = V_{Th} = 4.0 \text{ V}$$

**The answer is D.**

**PROBLEM 12**

Consider the following figure of a MOSFET.




**12.3** The drain-source current for a MOSFET in the saturation region is given by

$$I_{DS} = \left(\frac{K_n}{2}\right)\left(V_{GS} - V_{TN}\right)^2$$

The drain supply voltage, $V_{DD}$, is 10 V. MOSFETs are very low-power devices with the drain-source current in the micro-ampere range. What is the Q-point ($I_{DS}$, $V_{DS}$) of the circuit?

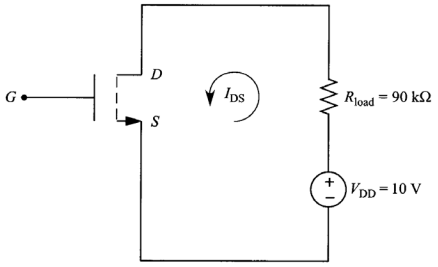
(A) (15, 1.0)
(B) (30, 1.0)
(C) (90, 1.9)
(D) (110, 2.9)

**SOLUTION 12**

**12.3** The drain-source current is determined by the operating conditions of the MOSFET in saturation and is calculated as

$$\begin{aligned} I_{DS} &= \left(\frac{K_n}{2}\right)\left(V_{GS} - V_{TN}\right)^2 \\ &= \left(\frac{20\times10^{-6}\ \frac{\text{A}}{\text{V}^2}}{2}\right)(4.0\ \text{V} - 1\ \text{V})^2 \\ &= 90\times10^{-6}\ \text{A}\ \ (90\ \mu\text{A}) \end{aligned}$$

Using KVL around the output loop gives




$$\begin{aligned} V_{DD} - I_{DS}R_{load} - V_{DS} &= 0 \\ V_{DS} &= V_{DD} - I_{DS}R_{load} \\ &= 10\ \text{V} - \left(90\times10^{-6}\ \text{A}\right)\left(90\times10^{3}\ \Omega\right) \\ &= 1.9\ \text{V} \end{aligned}$$

The Q-point, in microamperes and volts, is (90, 1.9).

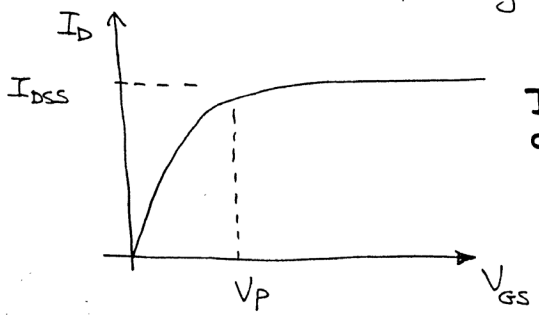
**The answer is C.**

5. An N-channel JFET has $I_{DSS} = 5$ mA and $V_p = 5$ volts. Estimate $I_D$ at $V_{GS} = -3$ volts.

Basic FET equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

watch signs. term should always be negative



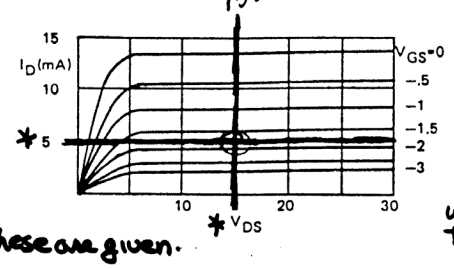

$I_{DSS}$ is saturation current beyond pinchoff.

If $V_{GS}$ is negative, $V_p$ must also be negative

$$I_D = 5\text{mA}\left(1 - \frac{-3}{-5}\right)^2 = 5\text{mA}\left(1 - \frac{3}{5}\right)^2$$

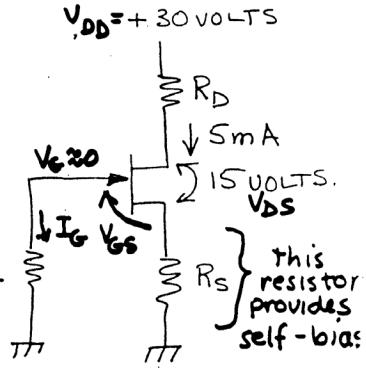
$$= 5\text{mA}\left(\frac{2}{5}\right)^2 = 5\,\frac{4}{25} = \boxed{0.8\text{ mA}}$$

6. An N-channel JFET has the characteristics shown. As a small-signal amplifier, it is to be self-biased at $V_{DS} = 15$ volts, $I_D = 5$ mA with a drain supply of 30 volts. Specify $R_D$ and $R_S$.




*These are given.

15V




$R_G$ is a large resistor (typically $R_G \approx 0.5 M\Omega$) which grounds the gate since $I_G \approx 0$.

Estimate $V_{GS} = -1.8$ volts from graph

Using KVL across $V_{DD}$ to ground. Always use KVL across output circuit.

$$V_{DD} - V_{DS} = I_D (R_D + R_S)$$

$$30 - 15 = I_D (R_D + R_S)$$

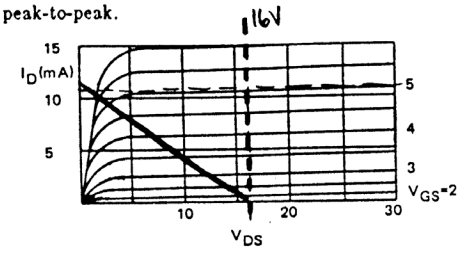
$$R_D + R_S = \frac{15}{I_D} = \frac{15 \text{ VOLTS}}{5 \text{ mA}} = 3k\Omega$$

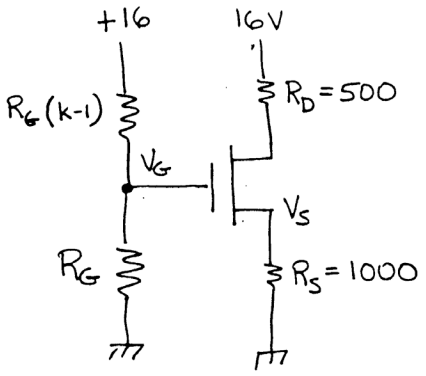
$$I_D R_S = 1.8 \text{ VOLTS} \quad \text{since } V_G \approx 0.$$

$$R_S = \frac{1.8 \text{ VOLTS}}{5 \text{ mA}} = 360\Omega$$

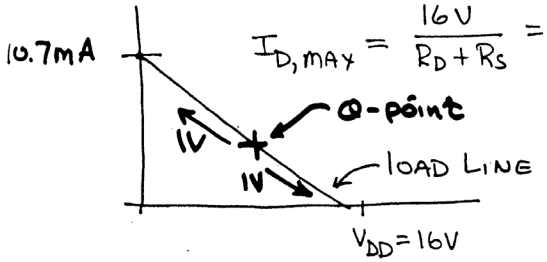
Then $R_D = 3000 - 360 = 2640\Omega$

7. An N-channel enhancement mode MOSFET with the given characteristics is to be operated as a source-follower with $R_D = 500$ ohms, and $R_S = 1000$ ohms, a D.C. supply of 16 volts. Determine a bias circuit which will permit an input voltage swing of at least one volt peak-to-peak.




① **Draw load line**




$$I_{D,MAX} = \frac{16V}{R_D + R_S} = \frac{16V}{500+1000} = 10.7\,mA.$$

Many choices of $V_{GS}$ are possible. Pick $V_{GS}$ = 3 VOLTS
Good range for $V_{GS}$ might be 3 to 4 volts from curves.
for somewhat linear operation.

For $V_{GS}$ = 3 VOLTS, $I_D \approx 2.5\,mA$ from graph.

$$V_S = I_D R_S = (2.5\,mA)(1K\Omega) = 2.5 \text{ volts}$$

$$V_G = V_{GS} + V_S = 3 \text{ VOLTS} + 2.5 \text{ VOLTS} = 5.5 \text{ VOLTS}.$$


No particular reason for I=1mA. Other typical consideration is input impedance.
Pick I = 1mA.

Then $R_{G1} + R_{G2} = \frac{16V}{1mA} = 16k.$

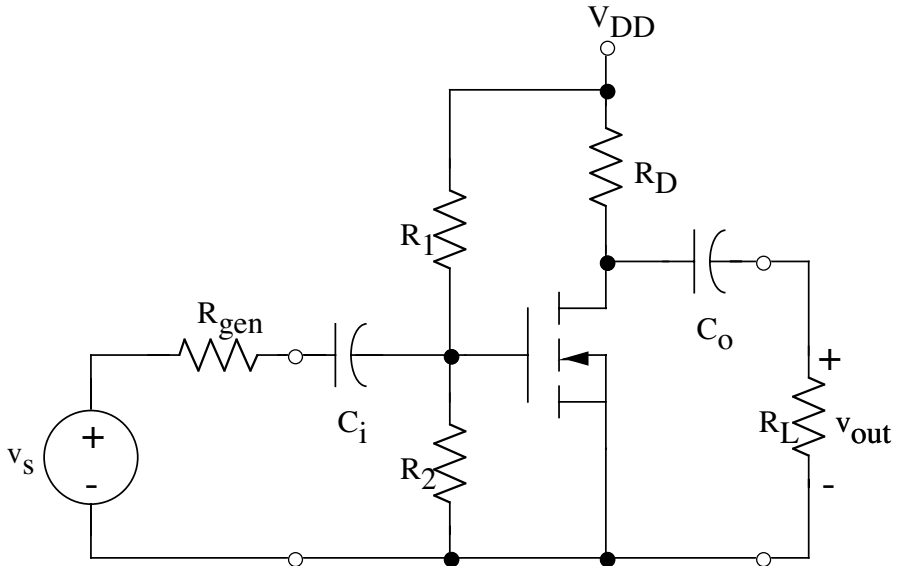
$$R_{G1} = \frac{5.5V}{1mA} = 5.5k$$

$$R_{G2} = 16 - 5.5 = 10.5k$$

LOTS OF OTHER CHOICES ARE POSSIBLE

5. Biasing MOSFETs

For the MOSFET amplifier circuit shown below determine the DC operating point of the transistor, i.e. determine $I_D$, $V_{DS}$, and $V_{GS}$.




The circuit uses the values $R_{gen}$= 10kΩ, $V_{DD}$=18V, $R_1$=3.3MΩ, $R_2$=1.2MΩ, $R_D$=2kΩ, and $R_L$=5kΩ The MOSFET is characterized by K=0.96mA/$V^2$ and $V_T$=2.5 volts.

ANSWER:

There is no voltage at the source as it is connected directly to ground. $V_{GS}$ is determined only by $V_G$ which is set by the $R_1$-$R_2$ voltage divider.

$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{1.2M\Omega}{1.2M\Omega + 3.3M\Omega}(18V) = (0.27)(18V) = 4.8Volts$$

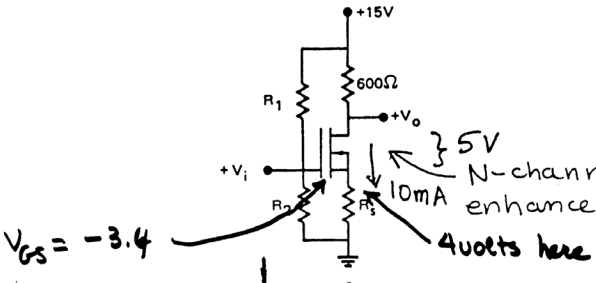
With the transistor parameter K AND $V_{GS}$ we can calculate the drain current as:

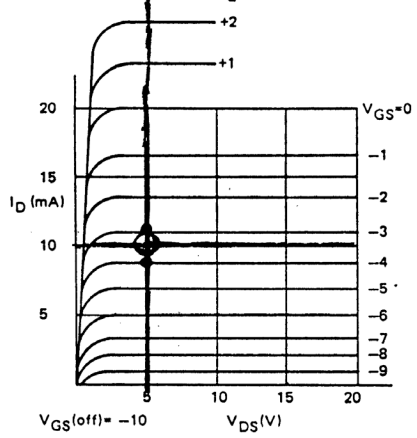
$$I_D = K(V_G - V_T)^2 = 0.96\frac{mA}{V^2}(4.8V - 2.5V)^2 = 5.08mA$$

Once the drain current is known we can apply KVL to the loop from ground through the transistor, through $R_D$, and through the power supply to ground to get:

$$V_{DS} = V_{DD} - I_D R_D = 18 - (5.08mA)(2k\Omega) = 7.84Volts$$

8. Design the bias circuit for the amplifier shown. The desired Q-point is 10 mA and $V_{DS}$ = 5 volts, with an input impedance of 100K Ω. Determine the amplifier gain if the resistance $R_s$ is capacitively bypassed.




Apply KVL to drain-source circuit

$$600 + R_S = \frac{15-5}{10mA} = \frac{10V}{10mA} = 1K$$

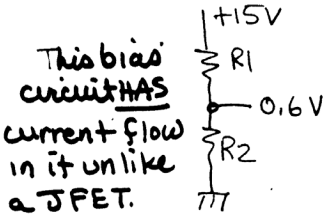
$$R_S = 1000 - 600 = 400\Omega$$

From characteristic curves estimate $V_{GS} = -3.4$ volts.

$$V_S = I_D R_S = (10mA)(400\Omega) = 4V.$$

$$\therefore V_G = 4V - 3.4V = 0.6V$$

Designing the bias circuit




This bias circuit HAS current flow in it unlike a JFET.

$$R_{IN} = \frac{R1\,R2}{R1+R2} = 100k$$

$$0.6 = \frac{R2}{R1+R2}\,15 \quad \text{or} \quad \frac{R2}{R1+R2} = \frac{0.6}{15} = 0.04$$

Substituting

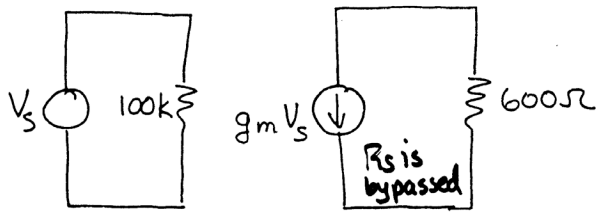
$$R1(.04) = 100k \Rightarrow R1 = 2.5M\Omega$$

$$R2 = .04R1 + .04R2$$

$$.96R_2 = .04R1$$

$$R2 = \frac{.04}{.96}R_1 = \frac{.04}{.96}(2.5M) = 104.2k$$

Small signal gain can be estimated (midband) from the circuit




Estimating $g_m$ from the characteristic curves

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} = \frac{11\,mA-(8.5\,mA)}{-3-(-4)}$$

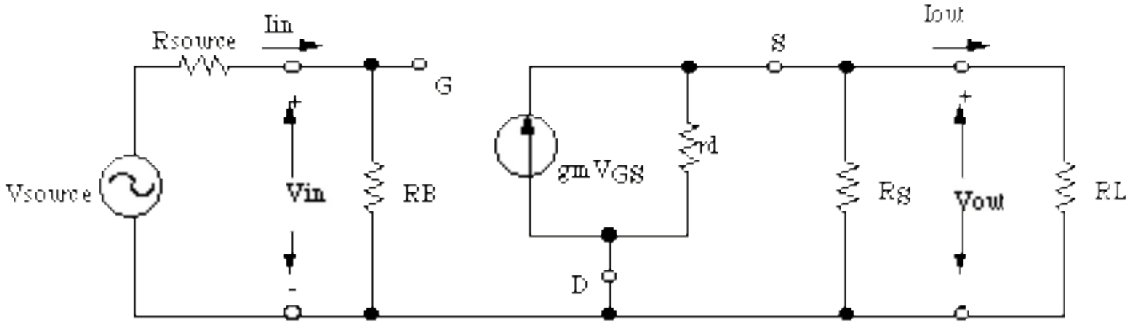
← these are very important

$$g_m = \frac{2.5\,mA}{1\,V} = 2.5\times10^{-3}$$

$$V_{OUT} \approx -\, g_m V_s\,(600)$$ since no input divider

$$\frac{V_{OUT}}{V_{IN}} \approx -\, g_m\, 600 = -\left(2.5\times10^{-3}\right)(600) = -1.5$$

6. Small Signal Amplifier Analysis




Consider the above small signal equivalent circuit for a MOSFET amplifier. The circuit parameters are $R_{SOURCE}$=100Ω, $R_B$=1.5MΩ, $R_S$=330Ω, and $R_L$=100Ω. The transistor's small signal parameters are $g_m$=0.05S and $r_d$=100kΩ.

(a) Determine the small signal voltage gain of this amplifier.

(b) What is the input impedance $R_{in}$ of this amplifier? The output impedance $R_{out}$?

(c) What is the current gain of this amplifier ASSUMING THAT $R_{in}$ =200kohms, $R_{out}$=1000ohms, and $\frac{V_{out}}{V_{in}} = 1$?

Answer:

(a) Rd is so large compared to RS||RL that it can be neglected. Then

$$R_L' = R_S \parallel R_L = \frac{R_S R_L}{R_S + R_L} = \frac{(330\Omega)(100\Omega)}{330\Omega + 100\Omega} = 76.75\Omega$$

In the output circuit $V_{out} = +\left(g_m V_{GS}\right) R_L' = +\left(0.05 V_{GS}\right)(76.75\Omega) = 3.84 V_{GS}$ [1]

Using KVL around the input circuit gives $-V_{in} + V_{GS} + V_{out} = 0$. [2]

Substituting [1] into [2] gives $-V_{in} + \frac{V_{out}}{3.84} + V_{out} = 0$ which can be solved to give the voltage gain $-V_{in} + 1.26 V_{out} = 0$, or $\frac{V_{out}}{V_{in}} = +0.79$

(b) By inspection. $R_{in}=R_B$=1.5MΩ

Using the definition for the output resistance and applying a test voltage source we get

$$R_{out} = \frac{V_T}{I_T} = \frac{V_T}{\frac{V_T}{r_d} + \frac{V_T}{R_S} + g_m V_T} = r_d \parallel R_S \parallel \frac{1}{g_m}$$

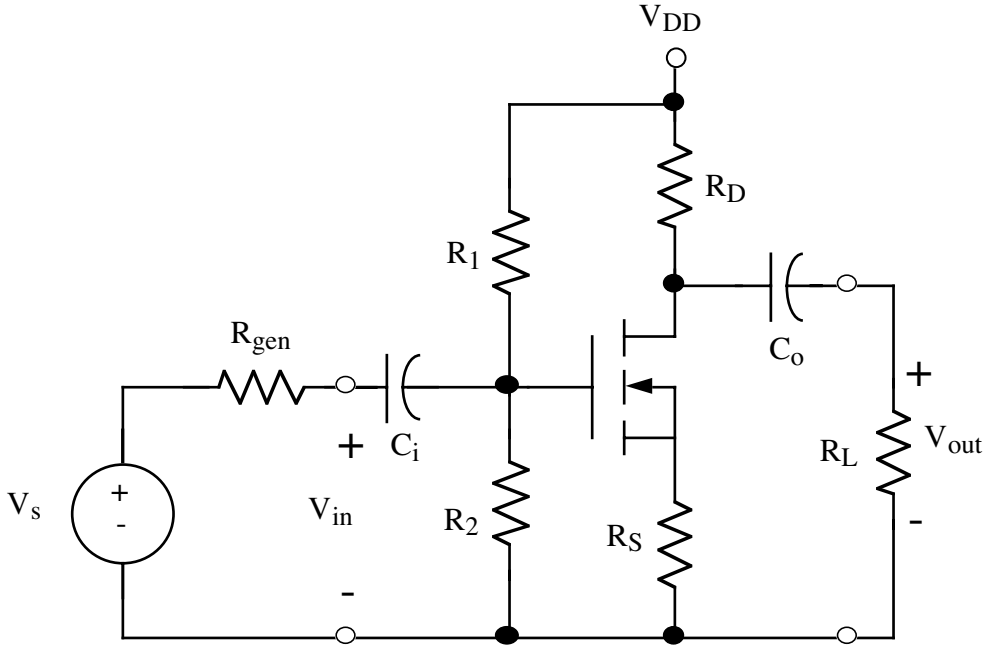
After substituting values we have $R_{out} = r_d \parallel R_S \parallel \frac{1}{g_m} = 100k\Omega \parallel 330\Omega \parallel 20\Omega \cong 18.85\Omega$

(c)

$$A_i = \frac{i_{out}}{i_{in}} = \frac{V_{out}/R_{out}}{V_{in}/R_{in}} = \frac{V_{out}}{V_{in}} \frac{R_{in}}{R_{out}} = (1)\frac{200k\Omega}{1k\Omega} = 200$$

# 3. MOSFETs (AC AMPLIFIER)

The amplifier circuit shown below uses an enhancement mode MOSFET with k=2.7 mA/V$^2$ and $V_T$=2.5 volts operating at $I_{DQ}$=1.2 mA. The circuit parameters are $R_{gen}$=600Ω, $R_K$=1kΩ, $R_L$=10kΩ, $R_1$=1.285MΩ, and $R_2$=237kΩ. You may neglect $r_d$ for the MOSFET.

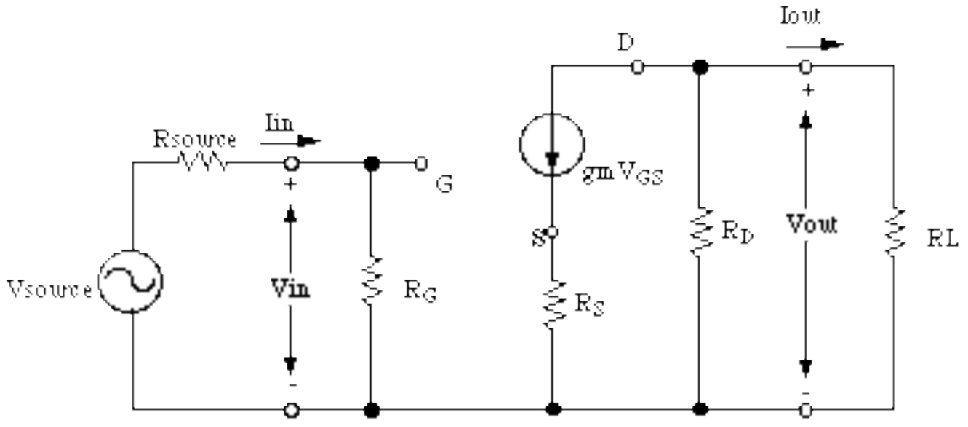



(a) Draw a small signal equivalent circuit for this amplifier indicating the values of all small signal parameters. Note that $R_S$ is NOT bypassed.

(b) Derive an expression for the small signal gain $A_v = \frac{V_{out}}{V_{in}}$ of this amplifier.

ANSWER:

(a) The small signal model is



I combined $R_1$ and $R_2$ into the single bias resistor $R_G$ since both go to ground. All the circuit paramerers are known except for $R_G$ and $g_m$ from the previous circuit diagram. The bias resistor is given by $R_G = \frac{R_1 R_2}{R_1 + R_2} = \frac{(1285k\Omega)(237k\Omega)}{(1285k\Omega) + (237k\Omega)} = 200k\Omega$. $g_m$ can be computed as

$$g_m = 2\sqrt{KI_{DQ}} = 2\sqrt{\left(2.7\frac{ma}{V^2}\right)(1.2mA)} = 0.0036S$$

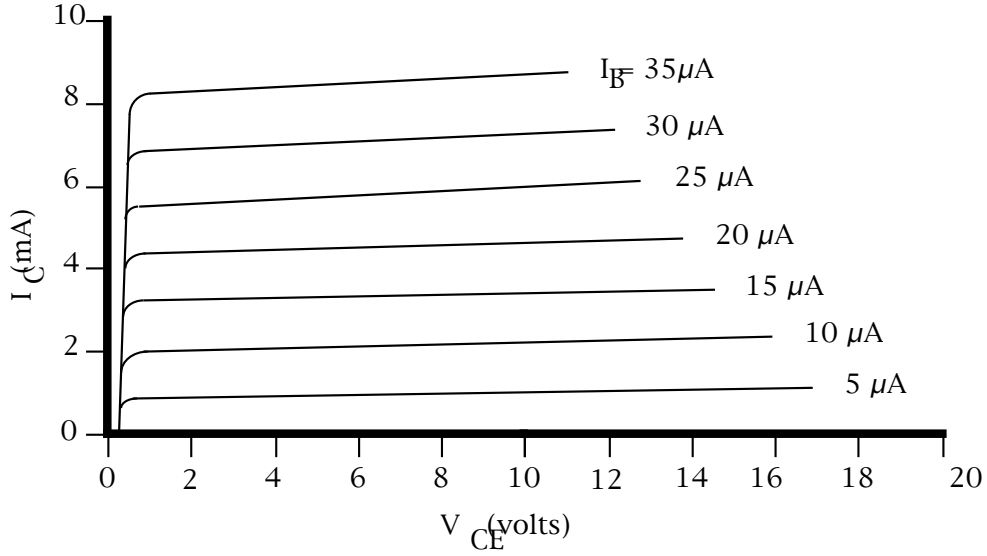
To determine the small voltage gain we first need to determine $V_{GS}$. We can do KVL around the loop defined by $V_{in}$, $V_{GS}$ and $R_S$, i.e., $-V_{in} + V_{GS} + (g_m V_{GS})R_S = 0$. This gives $V_{GS} = \frac{V_{in}}{1 + g_m R_S}$. The output voltage is simply given as $V_{out} = -(g_m V_{GS})(R_D \parallel R_L)$. These two results can be combined to give $V_{out} = -(g_m)\left(\frac{V_{in}}{1 + g_m R_S}\right)(R_D \parallel R_L)$ or

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{1 + g_m R_S}(R_D \parallel R_L).$$

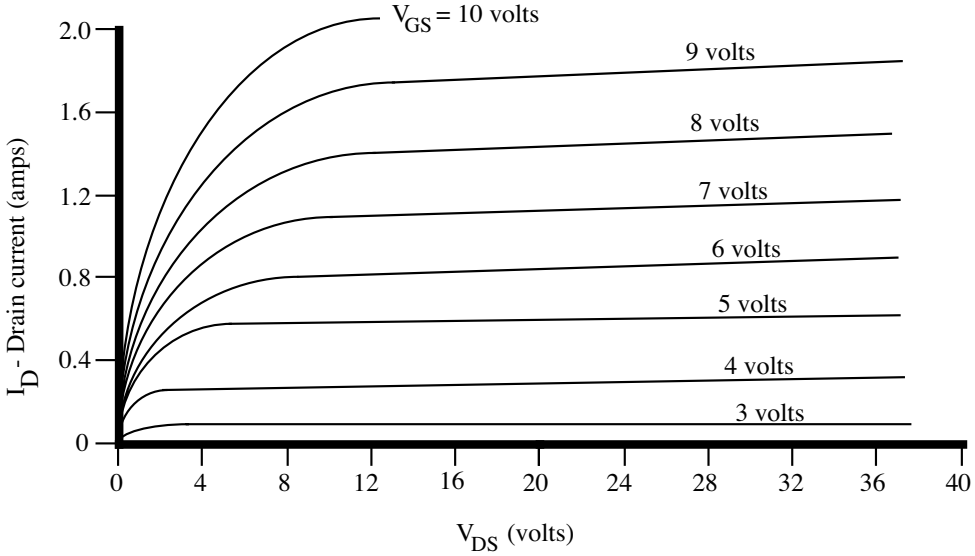
# REFERENCE MATERIAL:

## TRANSISTORS

MEASURED 2N2222 BJT CHARACTERISTICS




MEASURED 2N5447 MOSFET CHARACTERISTICS




MOSFETs

$$I_D = K\left(V_{GS} - V_{TO}\right)^2$$

$$g_m = 2K\left(V_{GS} - V_{TO}\right) = 2\sqrt{KI_{DQ}}$$

BJTs

$V_T$=26mV @ 300° C

$$r_\pi = \frac{\beta V_T}{I_{C,Q}}$$

$$g_m = \frac{\beta}{r_\pi} = \frac{I_{C,Q}}{V_T}$$