II. Final Presentations Slides

[1] Christopher Bertell, Hiep Nguyen, Kathryn Wassink, entitled – ***Machine Vision Interface with Seiko Robot Arm.*** The Technical Faculty Advisor for this project was Professor Gerardo Beni.

[2] Kamal Roumani and Jeremiah Kent, entitled – ***Robust Control Testbed.*** The Technical Faculty Advisor for this project was Professor Jay Farrell.

[3] Naqeeb Ameeri and Ali Seraj, entitled - ***Motion Detection and Object Tracking in Real Time.*** The Technical Faculty Advisor for this project was Professor Bir Bhanu.

[4] Karl Doering, Nadim Addus, Heath Deuel, Steven Gyford, Oscar Servin, Michael Wilson, entitled - ***Wireless Communication Systems Block Analysis and Design.*** The Technical Faculty Advisor for this project was the author, in collaboration with Mr. Dave Devries, Mr. Bob Kelly, and Mr. Daniel Kong of the Maxim Corporation.

The following list shows some of our experience that we would like to share with other course instructors and senior students.

(1) Please pay a particular attention to flags used in these slides, which serve to guide students in the timing and topics of their presentations.
(2) After the experience with using laptop computers and power points earlier in the mid-course presentations, we did not allow that anymore, because students tend to overburden themselves with many graphics and music added to their presentations – their presentations looked more like a made for TV production than actual technical presentations. Occasionally, students changed such presentations without changing their final report, naturally that practice was not allowed in our course. Also, we noted that when one group presents a made for TV presentation, students' concentrations shift completely to outside the classroom. The other groups worried that maybe their technical presentations were not good enough and they lost confidence.
(3) Sometime students using power point tended to show more slides than that they were allowed, a practice not appreciated by the rest of class. By requiring everyone to use the same number of actual "physical" slides (transparencies). Just as any technical presentation requires certain number of pages in a given presentation, *per se.* The entire focus becomes on the substance and actual technical merits of the project and not on the cosmetics.
(4) Furthermore, by asking students to drop their slides in the course instructor's office the night before, they finally go home and come back to present their projects according to the schedule hopefully rested. Otherwise, they want to make changes up to the last minutes before their presentation and that is not a good idea.

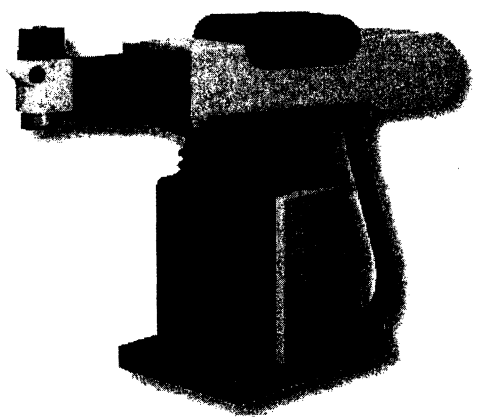
We should note that the final presentation is like a thesis defense setting and should be taken very seriously. This is an important overall educational experience for students.

Regarding the fourth set of slides, by Karl Doering, Nadim Addus, Heath Deuel, Steven Gyford, Oscar Servin, Michael Wilson, this is an ensemble of three projects, and as such there is a slight cross presentation among the three groups. This instructor was extremely lucky to have the best senior student of the class 2001 in the electrical engineering program at UCR, Mr. Karl Doering, interested in this topic. He also played the role of technical manager for the group. The business manager of the group was Mr. Michael Wilson who also served as a daily liaison between the author and all team members, though we had regular weekly meetings. This is how senior design projects should be conducted – a marriage between industry and engineering programs.

EE 175 Senior Design

Professor Mansour Eslami

Machine Vision Interface with Seiko Robot Arm



Christopher Bertell
Hiep Nguyen
Kathryn Wassink

June 8, 2001

Faculty Advisor: Dr. Gerardo Beni
Technical Advisor: Dan Giles

Problem Statement

To integrate a vision system with the Seiko RT3200 Robot Arm, including electronics interfacing between a PC and the robot arm as well as developing vision demos using C++ or Visual Basic with the Vision System.

Design Specification

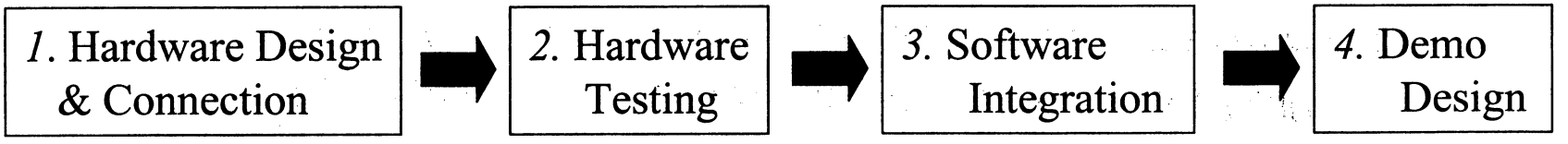
To create a system that will use the camera to find and recognize an object, then send commands to the Robot Arm based on the data.

Preparation

Possible Designs

- Hardware
  - Serial vs. Parallel Cable Connections
  - Camera Mounting Positions
- Software
  - Microsoft Visual vs. Non-Visual Language [VB-RM†]
  - C++ vs. Basic [MSDN‡]

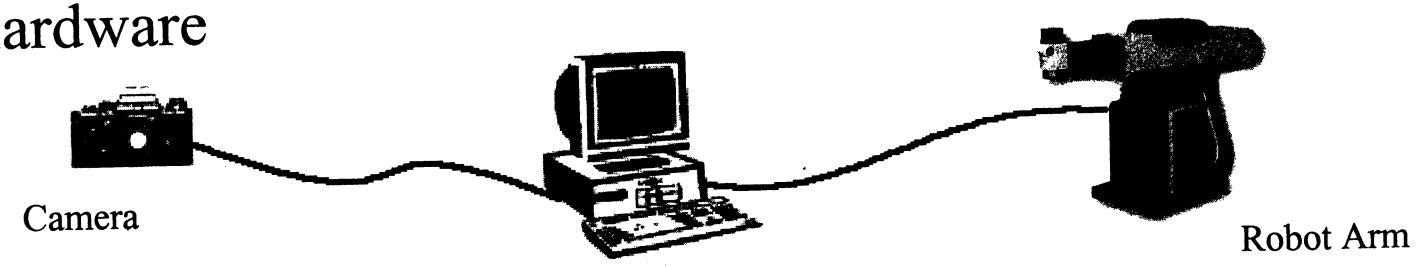
Approach



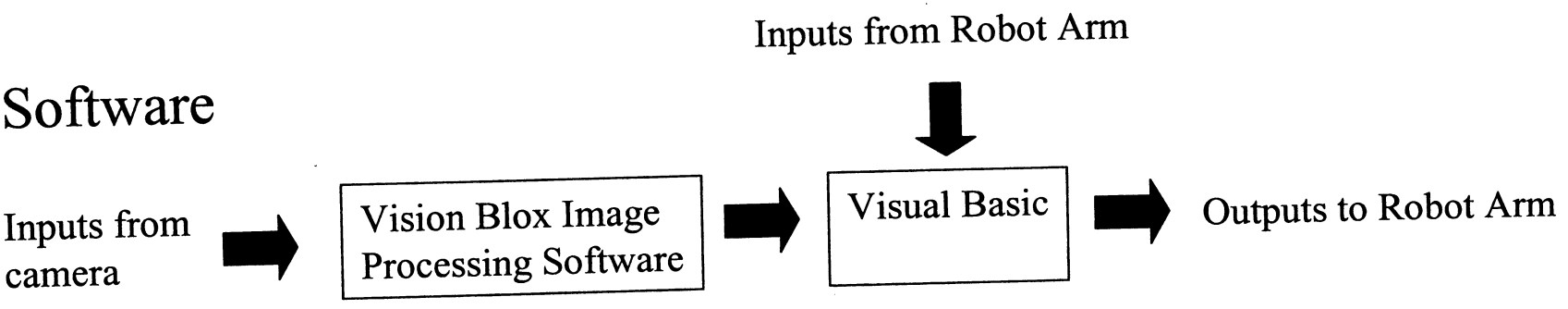
† VB-RM: Vision Blox Reference Manual
‡ MSDN: Microsoft Developer's Network Ocotober '99

The System

Hardware



Software



Test Plan

- Use DARL to confirm output to Seiko arm.
- Use PX5 software to confirm camera operation.
- Use demos to confirm software integration.

Meeting Expectations

- Able to create a machine vision interface
- Able to get a camera input and use it to get a robot output

Design Comparisons

- Simpler than original plan
- Cleaner user interface when final product is done.
- Easier to program for serial communications

Elements of Design

- Increases safety by removing workers from potentially harmful situations.
- Probable shifting of workers from assembly-line positions.
- Possible conflicts between workers and companies.
- Improves our understanding of robotics and image processing.

Cost Analysis

- Marketability

  It would be an upgrade, primarily for companies with older-model robot arms.

- Budget

*Prototype Costs *:*

Parts	$ 3,025
Software	220
Direct Labor 35 hrs @ $25/hr	875
Capital Equipment	4,000

Marketing Analysis $ 12,000

Estimated Costs to Produce 1,000 units:

Parts (at bulk rates)	$ 115,000
Direct Labor (1.5 hrs/unit @ $25/hr)	37,500
Storage (1/sq.ft/month, 100 for 6 months)	600
Advertising Costs:	$ 10,000
Total	$ 153,100

Overhead Cost (85% of above):	$ 130,135
Expected Total Profit	$ 90,000
Grand Total	$ 343,235

Expected Sales ***750 units***

Price Per Unit **$ 499.99**

Administration

- Christopher: Project Leader, Hardware, Control Programming
- Kathryn: Vision Programming, DARL testing
- Hiep: Control Programming, Vision Programming, Hardware

Conclusions

Expansion and Improvements

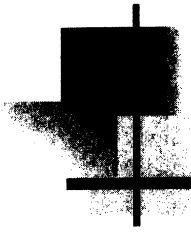
- New end-effector
- Translation function
- New vision functions: edge detection, rotation, color meter
- New Seiko commands: display, jog, changing speed
- Remount the camera

Lessons Learned

- Don't take anything for granted
- It's all right to ask for help
- Sometimes trial and error is the only way to go

‡DARL: **D**-TRAN **A**ssembly **R**obot **L**anguage

EE 175 Senior Design
University of California, Riverside
Electrical Engineering Department

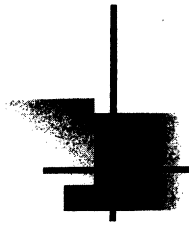


Robust Control Testbed

Kamal Roumani / Jeremiah Kent

June 8, 2001

Professor Mansour Eslami
Project Advisor: Dr. Jay Farrell
Technical Advisor: Dan Giles



Technical Issues

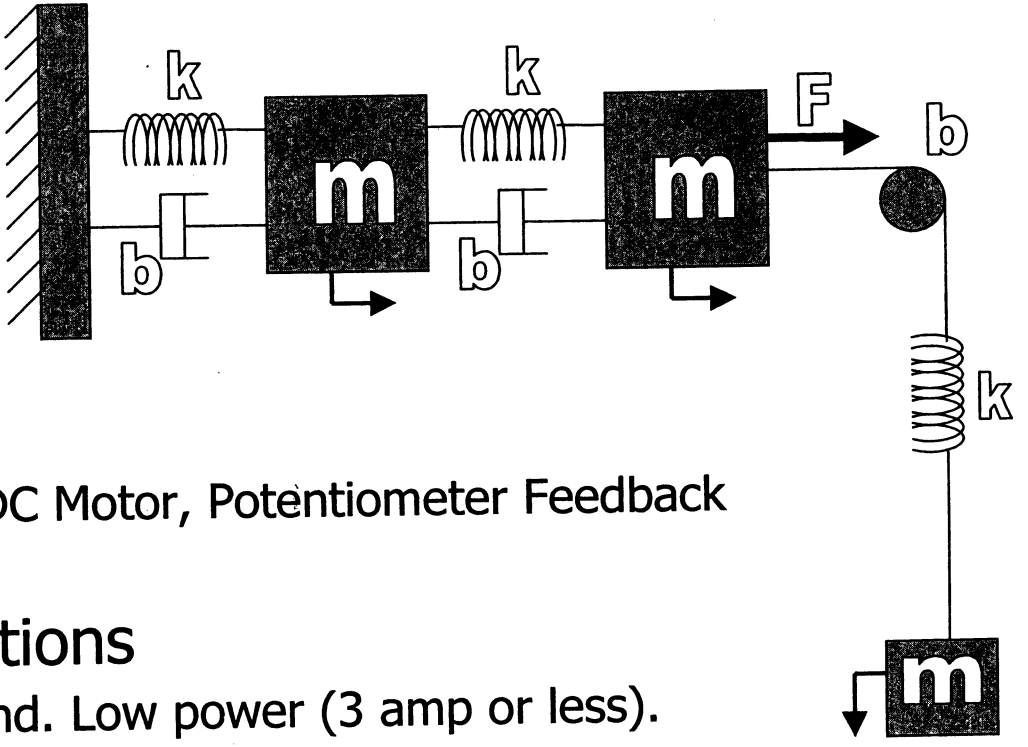
Current System Problems:

- Not Efficiently Used
- Too Complicated
- Limited
- Too Expensive

Design Requirements:

- Experimentally Flexible & Expandable
- Simple Basic Form
- Hands-on Control
- Low cost

Design Specifications



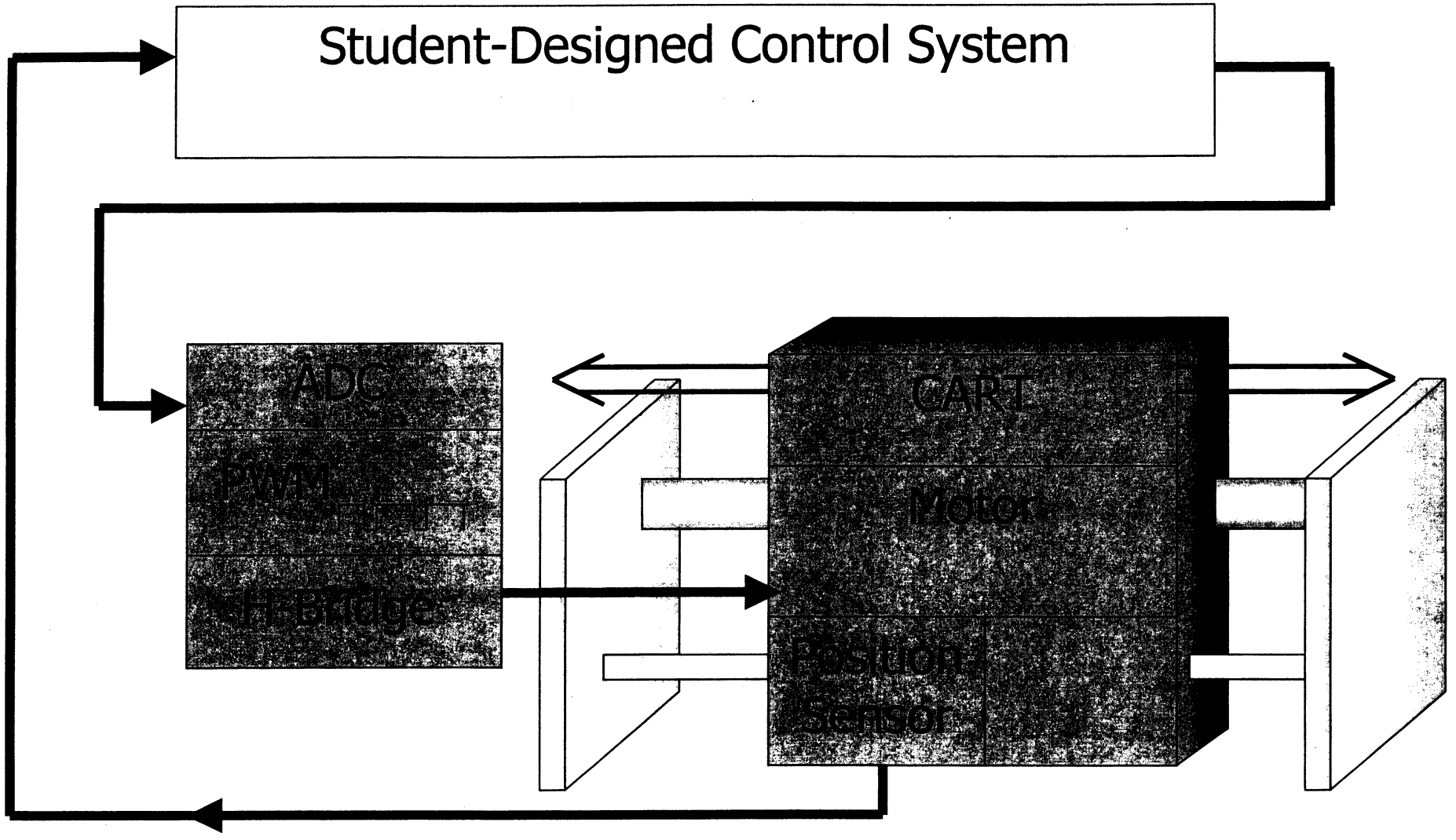
- **Possible Approaches**
- Tortional, Gantry Crane,
- Linear, rotational.

- **Our Design**
- Linear, 1 to 3 DOFs, PWM, DC Motor, Potentiometer Feedback

- **Performance Expectations**
- Transit 1m track in ~1 second. Low power (3 amp or less).

- **Component Specifications**
- Motor – torque > 0.325 N-m ; > 550 rpm
- Power Supply – ±12VDC ; > 1.33 amp

Design Overview



Cost Analysis and Marketability

Cost / Unit

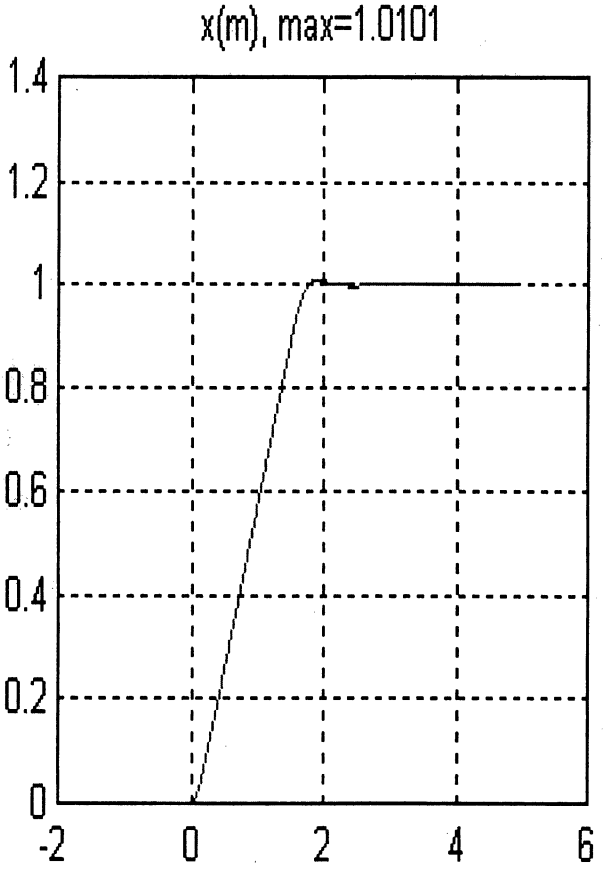
DC motor	$17.50	$15.00
POT	$16.00	$15.00
Bearings	$115.00	$115.00
Gears	$43.00	$40.00
Track	$75.00	$64.00
H-bridge	$5.00	$5.00
Total:	$271.50	$254.00

Budget Analysis

- Prototype Cost $ 10,800.00
- Marketing and Advertising $ 11,000.00
- Production Costs $300,000.00
- Overhead Costs $270,000.00
- Expected Profit $100,000.00
- Grand Total $690,000.00
- Expected Sales 400 units
- Price / Unit $ 1,749.00

Critical Evaluation

- Due to the motor's internal gearing the damping of the system was significantly higher than originally expected, giving transit times of about 1.5 seconds.
- Ideally a motor with less internal friction would produce a more interesting system to control.
- Our prototype has only one degree of freedom. A production model would have up to 3 degrees of freedom and capabilities for digital control and feedback.

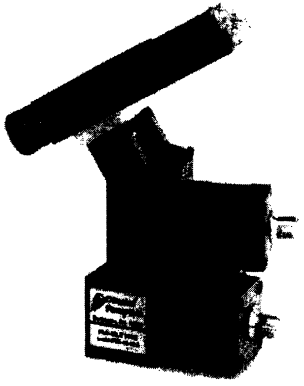


Lessons Learned

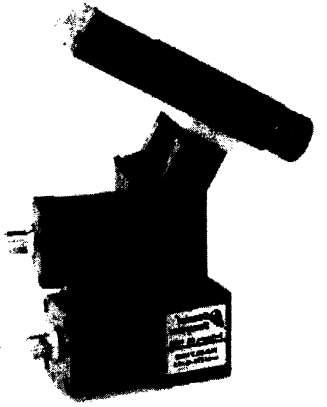
- Modeling a system before implementing it can be a Good Thing
- The entire system should work before the first part is purchased.
- No two problems can be solved the same way; be independent thinker and do not use the "rubber stamp" approach (in the spirit of Professor T.J. Higgins)
- THANKS

  to Dr. Eslami and Dr. Farrell, as well as to Dan Giles and Mike Fournier

Final Presentation of Senior Design Project for
Winter/Spring 2001
Professor Mansour Eslami



The University of California at Riverside
College of Engineering
Department of Electrical Engineering



Motion Detection and Object Tracking in Real Time

Prepared by: Naqeeb Ameeri & Ali Seraj

Technical Faculty Advisor: Professor Bir Bhanu

This project is supported by the Visualization and Intelligent Systems Laboratory at the University of California Riverside

Problem Statement: To implement a motion detection and tracking system in real time.

Applicable Solutions:

- Sensor Based system using infrared motion sensors and a micro-controller
- Transmitter/Receiver based system

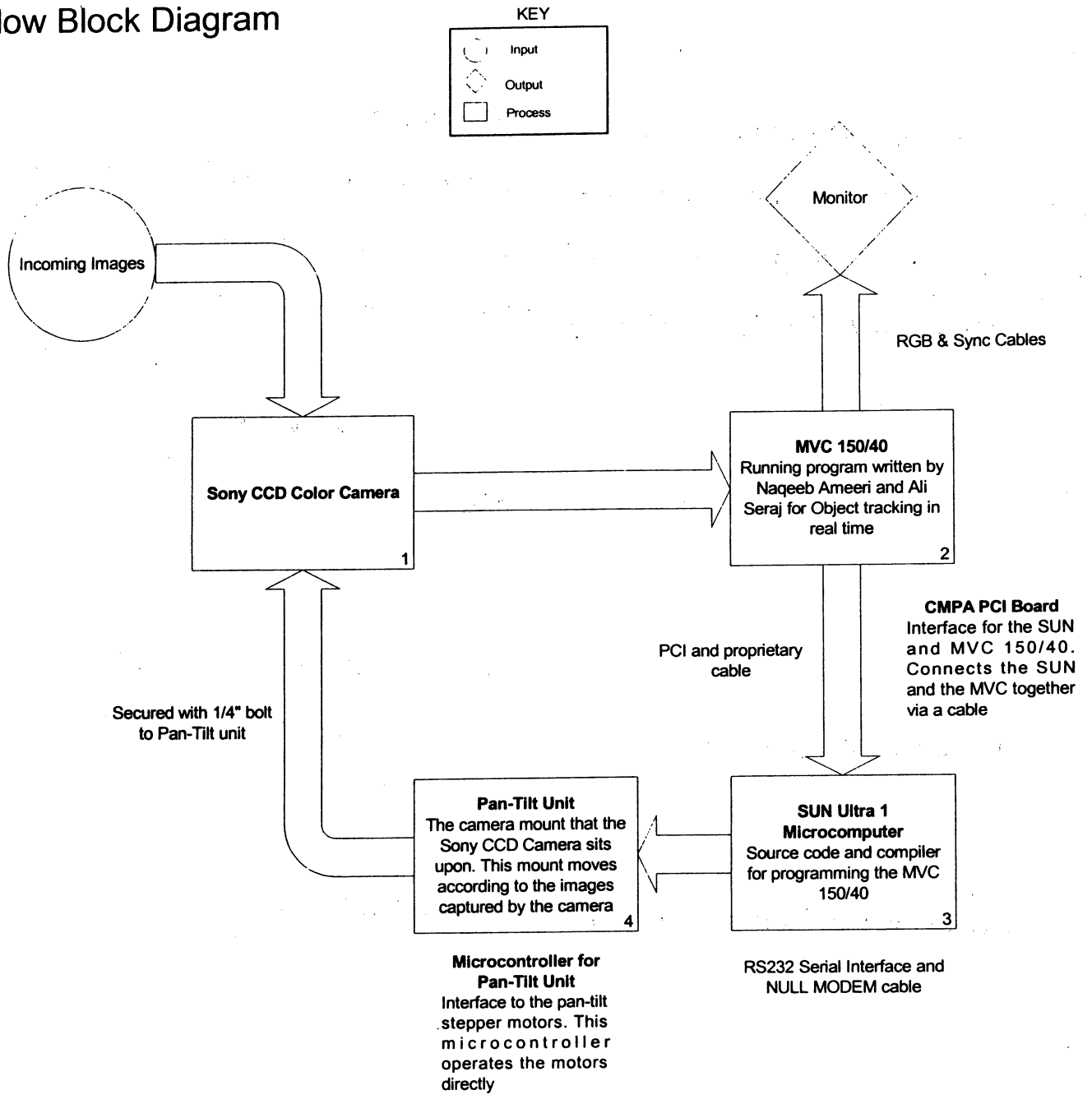
Design Solution

Image Processor based system

- **Applications:**

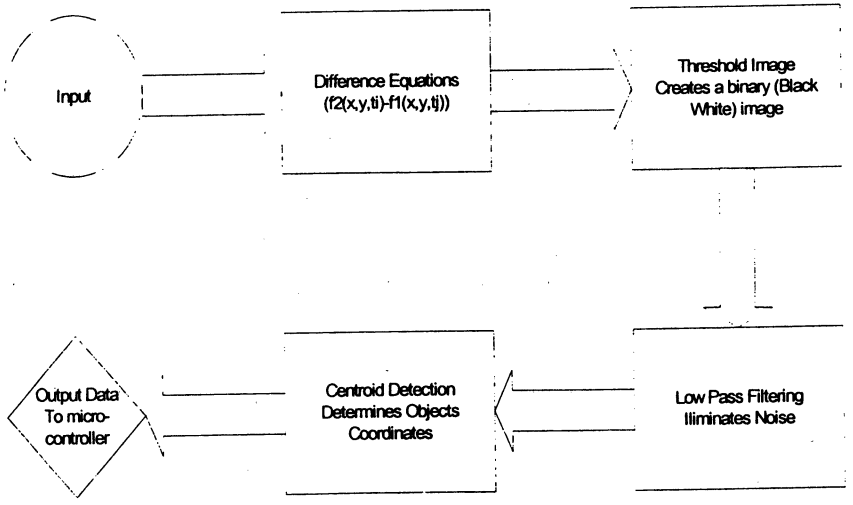
  - Can perform image analysis and extract movement based upon models.
  - Adaptable to most real world situations when motion detection and tracking are required.
  - Software programmable image processor makes changing applications relatively simple.
  - These systems are often extremely fast allowing real time processing.

Hardware Flow Block Diagram



Selected Technical Approach:

Image Processor based system



Design Specifications:

Number of Frames/Buffer/Second	8
Number of Buffers	4
Frame Rate = # of frames * # of buffers	32
Serial Communication:	
Serial Interface Type	RS-232 C
Data Transfer Rate	9600 bits/sec
No. of bits	8 data
	1 start
	1 stop
Largest command size (bytes - bits)	64 - 512
Smallest command size (bytes - bits)	32 - 256
Pan and Tilt Unit Specs:	
Max Pan Range	280 deg. Left to Right
Max Tilt Range	31deg. UP
	41 deg. DOWN
Max Pan and Tilt Speed	300 deg./second
Resolution	.05 deg.
Command completion times (average)	
PAN - small (< 30 deg.)	.3 seconds
PAN - medium (31 to 90 deg.)	.6 seconds
PAN - large (91 to 140 deg.)	1.2 seconds
TILT - small (< 16 deg.)	.2 seconds
TILT - medium (17 to 31 deg.)	.4 seconds
Moving Object	
Minimum object dimension (pixels)	35X35
Minimum object speed (change in pixels)	atleast 20

Schedule

Weeks 20-22: Final Report and Presentation development

Weeks 19: Fine tuning tracking and serial communication

Week 18: Configure software to utilize tilt axis

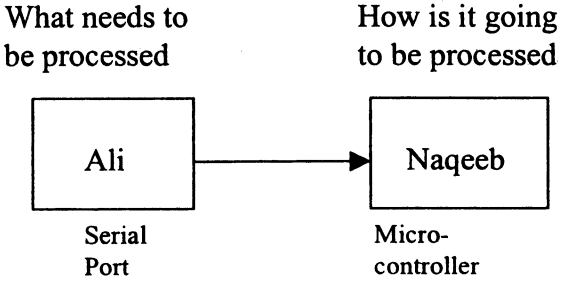
Weeks 16-17: Configure software to track on pan axis

Weeks 14-15: Enable serial communication between SUN and PTU

Weeks 4-13: Research

Weeks 1-3: Hardware/Software checks

Tasks



Cost Analysis / Business Plan

Prototype Cost:		
Parts		$6,525.00
Software		$0.00
Direct Labor (60 Hours 20/ hour)		$1,200.00
Company Facility / Capital Equipment	$32,780.00	
Depreciation Schedule	(40% the first year)	
Marketing Analysis:		
Expenses for Direct Sales and Advertising Costs		$15,000.00
Estimate Costs to Produce 1000 Units:		$
Parts (purchased at bulk rate)		$6,175,000.00
Labor (3 units/hour) @ 20/hour)		$5,000.00
Storage ($1/square feet/month)		$2,100.00
Total		$6,237,905.00
Overhead Cost (85% of the above)		$5,302,319.00
Expected Total Profit		$5,620,352.00
Grand Total		$17,160,476.00
Expected Sales		750 Units
Price Per Unit		$22,880.99
Shipping and Handling		$45.00

Design Constraints

Improving communication between SUN and PTU serial interface

Serial communication speed and command execution time

Computational overhead incurred calculating camera distance from target

Computational overhead incurred calculating background movement and compensation

Elements of Design

Realistic claims based on available data

Motion camera promote public safety

Improves understanding of machine vision and digital image processing

Assists colleagues and co-workers in image processing development

Goals and Design Accomplishments

√Panning against white background

√Tilting against white background

√Tracking an object against an ordinary background

Future Expansion

- The use of a modern image processor and personal computer.
- Background removal.
- Multiple object tracking.

EE 175 Senior Design Project

Professor Mansour Eslami

Maxim W-CDMA Transceiver Design

Senior Design Team:

Nadim Addus
Steven Gyford
Heath Deuel
Oscar Servin
Karl Doering
Michael Wilson

Technical Advisors:

Dave Devries - Bob Kelly - Daniel Kong

Date of Presentation:

June 8, 2001

Project Introduction

- Project Background
  - Welcome professors, fellow classmates, and visitors
  - UCR / Maxim Senior Design Project development
  - Project involves the analysis of and improvement upon a Wideband Code-Division Multiple Access (W-CDMA) transceiver
  - Projects tasks distributed into three major areas of the transceiver
  - Team / Team member introduction

- Communication System Overview
  - Historical perspective
  - Function of a transceiver
  - Various architectures of a transceiver
    - Homodyne
    - Heterodyne
    - Superheterodyne
  - W-CDMA versus other multiple access techniques
  - Critical components / blocks within a W-CDMA transceiver
  - Function of the various components / blocks

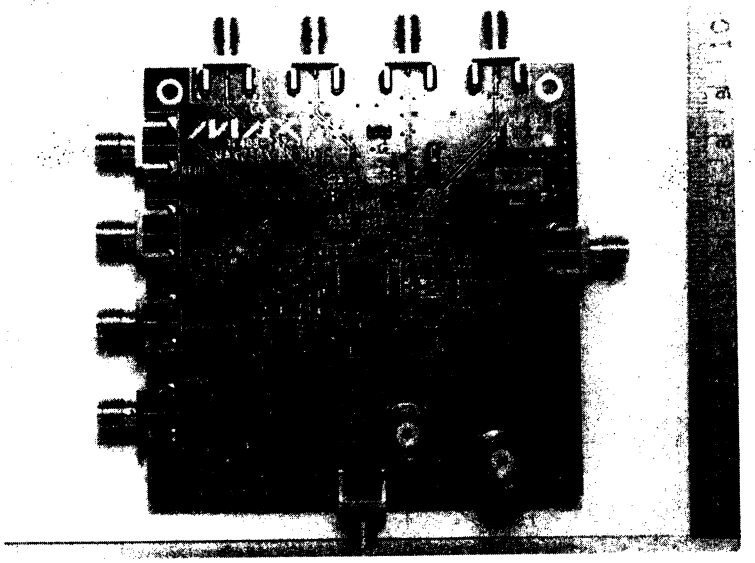


Figure 4.2.2.2-1. MAX2360 EV board.

W-CDMA Reference Design

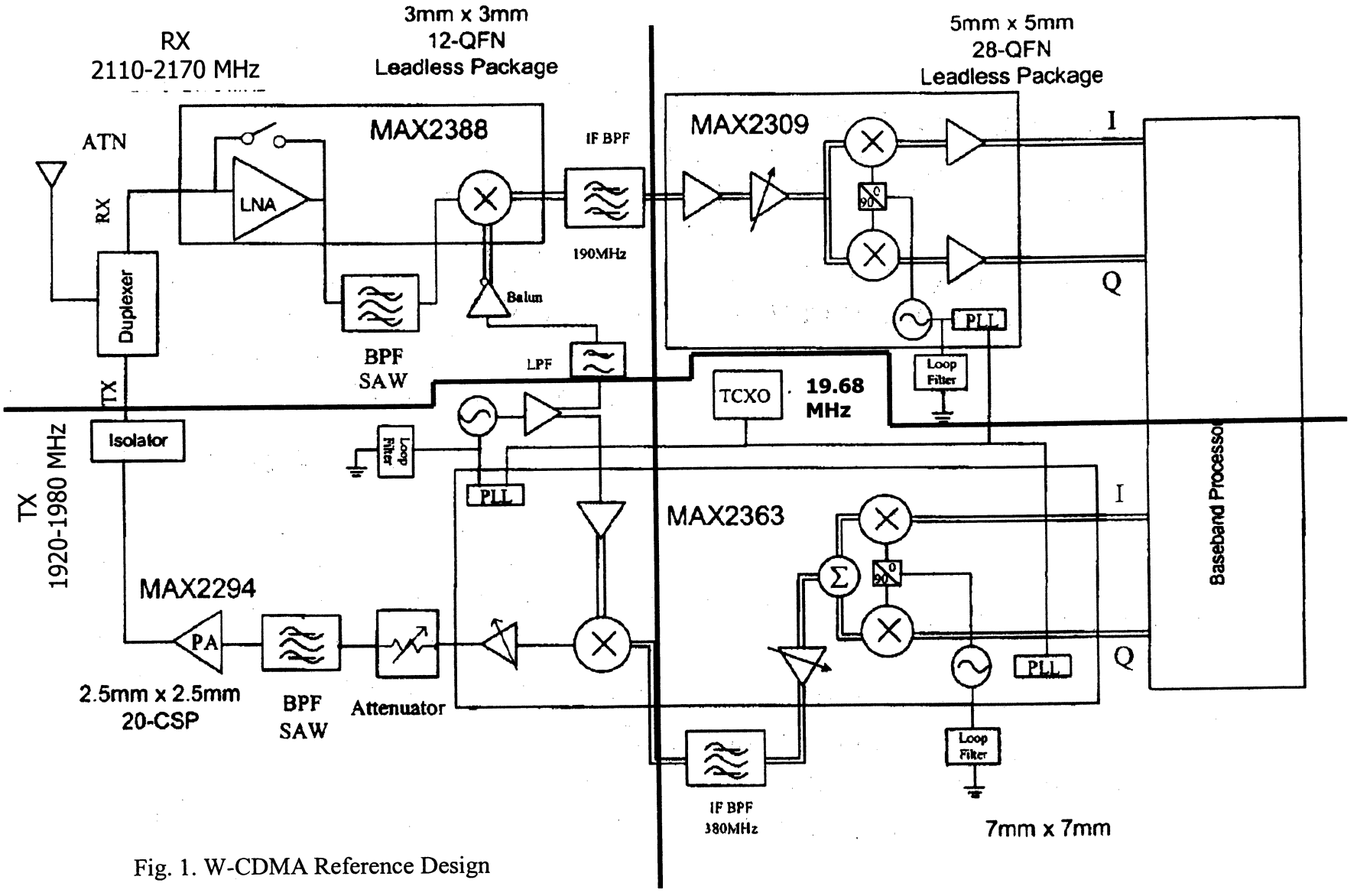


Fig. 1. W-CDMA Reference Design

Introduction

Problem Statement

- Trace signal through various components of the receiver (Rx range: 2110-2170 MHz)
- Calculation and analysis will determine dynamic range, cascade voltage gain, sensitivity, selectivity, cascade noise figure, and cascade third-order intercept (IP_3).
- Verification that reference receiver meets the *Third Generation Partnership Project* (3GPP) technical specifications
- Improvement of adjacent channel interferers rejection of I/Q baseband signals through design of low-pass filter

Design Specifications

Table 2.3.1-1. Required attenuation characteristics at selected frequencies.

Channels	Freq Offset (MHz)	Att. LPF (dBc)
CH-Wanted	0	0.0
CH-Adjacent	± 5	-10.0
CH-In-Band-Blk	± 10	-25.0
CH-In-Band-Blk	± 15	-45.0
CW-Out-Band1-Blk	>± 15	-45.0
CW-Out-Band2-Blk	>± 60	-55.0
CW-Out-Band3-Blk	>± 85	-55.0

Other design parameters:

- Filter output needs to be single-ended
- Order of filter
- Implementation, type, and topology of filter
- Voltage Gain of 6 dB
- Desired signal bandwidth of 1.92 MHz

Method of Solution

Our Design

- Determine order of filter from most stringent constraint; the corner frequency is chosen to be 3.0 MHz
- Filter's resistor and capacitor elements are determined from look-up tables
- Fourth-order Butterworth low-pass filter meets our requirements

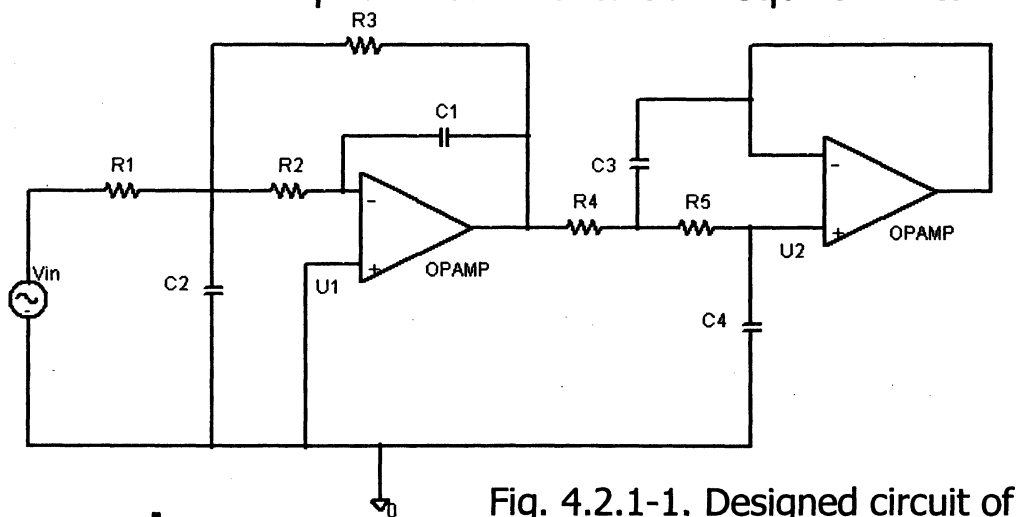


Fig. 4.2.1-1. Designed circuit of fourth-order Butterworth low-pass filter.

Alternative Approach

- **Different filter Implementations:**
  - Chebyshev: Ringing in pass-band causes unwanted noise in desired signal
  - Bessel: Poor attenuation in stop-band requires higher order filter
- **Various filter types:**
  - Passive: Require more space than active filters
  - Digital: Need high processor speed for large bandwidths

Evaluation (1)

Discussion of Results

- **Receiver Performance Summary**
  - Cascade Noise Figure: 2.4 dB which meets 5 dB requirement
  - Cascade Voltage Gain: 12.5 dB
  - Cascade Third-Order Intercept: – 4.12 dBm
- **Filter Performance Summary**
  - –3 dB point at 3 MHz
  - Meets our most stringent requirement of 39 dB of attenuation at 15 MHz
  - Maximally flat response in the pass-band

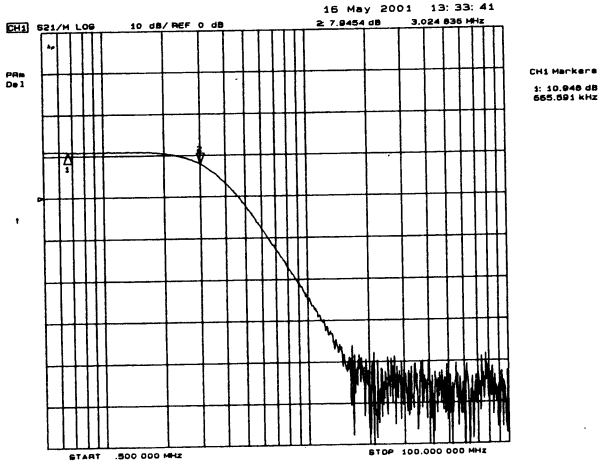


Fig. 4.3.1-1. Magnitude response of low-pass filter.

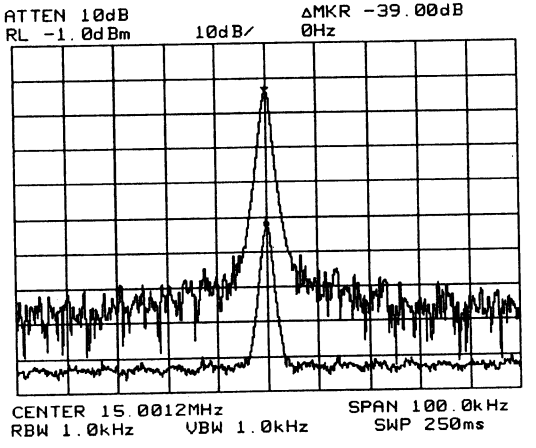


Fig. 4.2.1-4. 15 MHz blocking test of filter.

Evaluation (2)

Design Comparison and Tradeoff

- Simulated frequency response matched actual response
- Group delay (within 100 ns) and phase (as compared to *PSpice* simulation) performed as expected

Category	Simulated	Achieved
Group Delay	49 ns @ 2 MHz	50 ns @2 MHz
Phase	90 deg @ 2 MHz	90 deg @ 2 MHz

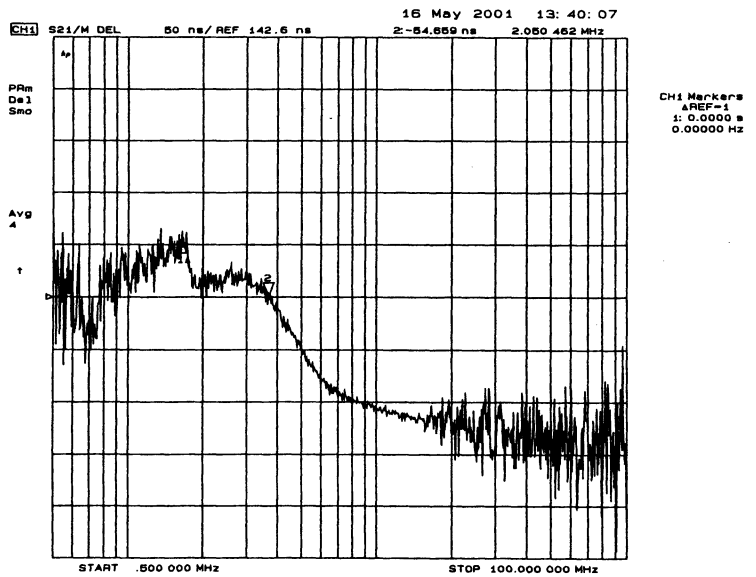


Fig. 4.3.1-5. Group delay of low-pass filter.

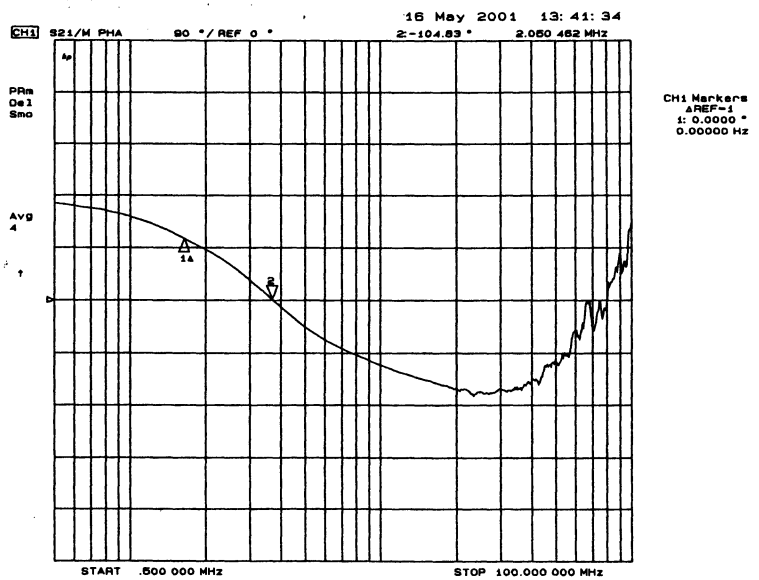


Fig. 4.3.1-6. Phase response of low-pass filter.

Meeting Expectations / Conclusions

Design Constraints

- Lack of component availability of exact designed value
- Pre-existing etched surface mount board
- Op-amp differential output not utilized

Lessons Learned

- Solution broken into more manageable pieces
- Final designed circuit needs additional "tweaking"

Expansion and Improvement

- Temperature considerations
- Design of application specific surface mount board for cleaner circuit

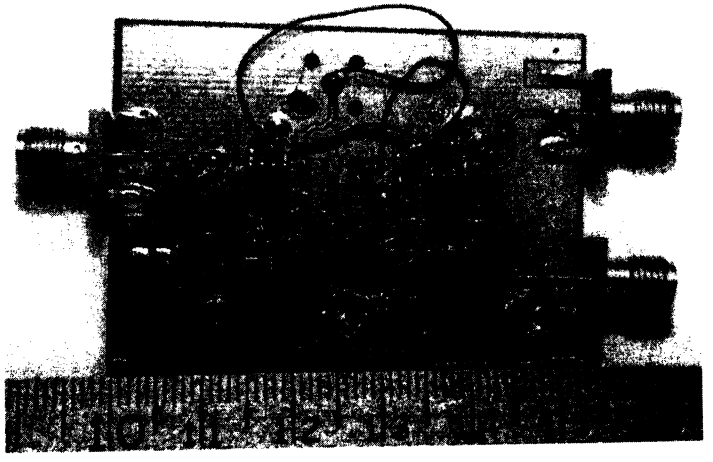


Fig. 4.2.1-2. Picture of actual fourth-order Butterworth low-pass filter.

Problem Statement

- The transmitter project is divided into two stages
  - Analysis of the transmitter portion of a W-CDMA transceiver
    - Become familiar with concepts involved in radio frequency design
    - Identify spurious frequency component
  - Design of an intermediate frequency band-pass filter
    - Meet specifications determined by the signal path analysis
    - Implement at lower cost than the current IF / SAW / BPF

Design Specifications

Table 2.3.2-1.1. Transmitter signal path specifications.

Signal Path Analysis Specifications	
Operating Frequency Range	1920 MHz - 1980 MHz
Output Level	23 dBm
Minimum Output Level Range	75 dB

Table 2.3.2-1.2. Transmitter filter specifications.

Filter Design Specifications	
Center Frequency	380 MHz
3 dB Bandwidth (minimum)	6.8 MHz
Attenuation at 190 MHz	37 dB
Attenuation at 760 MHz	40 dB
Differential Input Impedance	400 Ohms
Differential Output Impedance	600 Ohms

Our Design

- Examine Q_{bp} of filter to determine if it is realizable
  - Determine type and order of filter using steepness factor and tables
  - Initial examinations: 4th order 0.1 dB Chebyshev; 3rd order 6 dB Gaussian; 2nd order Butterworth
  - Selection basis: low-cost, phase response, high attenuation far from f_0, steepness factor
  - Select, determine component values; simulate & adjust for finite Q; transform to differential form; simulate again with available component values

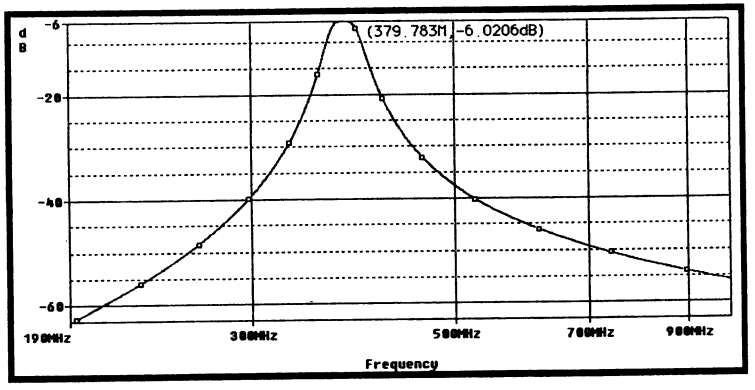


Fig. 3.2.2-2. Simulated response, 190 MHz – 1 GHz.

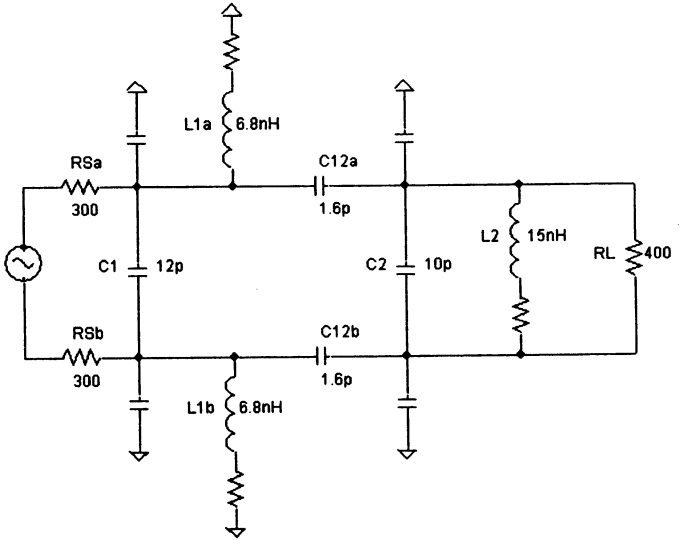


Fig. 3.2.2-3. Final circuit, after transformation to differential form.

Alternate Approach

- Alternatives: Active vs. passive; wideband vs. narrowband; response characteristics
- Configurations & techniques: LP to BP transform; parallel, series, & synchronously tuned
- Choice of narrowband coupled resonator: high Q, simplified tuning, capacitive coupled

Discussion of Results / Test Plan

- Initial plan: construct prototype on circuit board; measure response; examine effects on TX
- Intermediate trials: construct prototype on MAX2360 EV board instead of unetched board
  - Could not lock PLL at 760 MHz (board specifies an IF of up to only 300 MHz); modified tank circuit
  - PLL locks, but range is too narrow to allow testing of full response of filter (190 - 760 MHz)
  - Bypass on-board PLL with use of signal generator; obtained inconsistent data measuring w/ probe
- Final plan: revert to initial plan using prefabricated PCB with suitable pads and traces
  - Constructed circuit converting differential input and output to single-ended input and output
  - Response was measured on an HP 8753E RF network analyzer
  - Component values were tweaked to compensate for finite Q values and stray capacitance

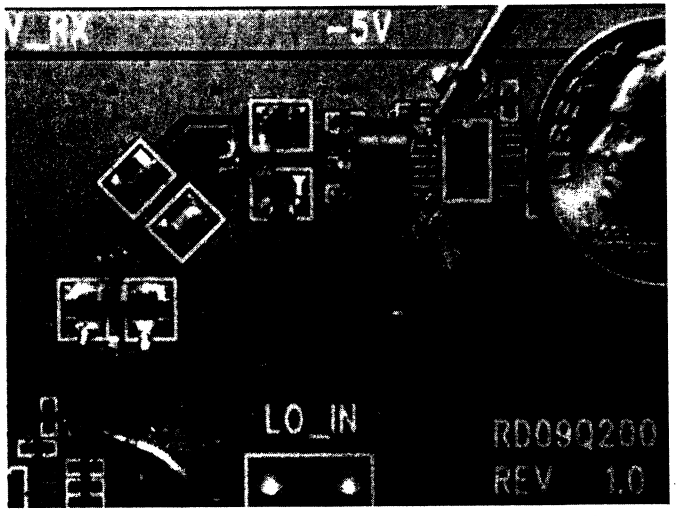


Fig. 4.2.2.3-2. Implementation of prototype (dime shows scale).

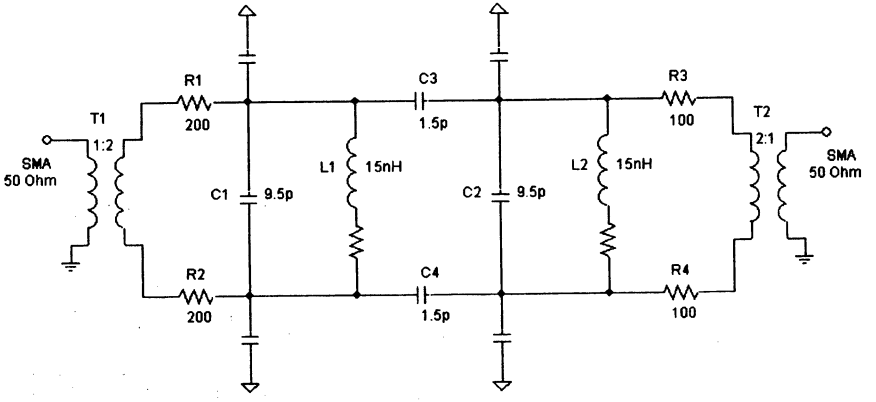


Fig. 4.2.2.3-1. Final prototype circuit.

Filter Performance: initial response & tuned response

- C_1 and C_2 adjusted several times between 8 and 12 pF to obtain desired response
- Final response of filter: 3 dB BW of 35.4 MHz; insertion loss of approximately 9 dB; attenuation of 39.7 and 44.2 dB at critical frequencies of 190 and 760 MHz, respectively
- Simulated response: 3 dB BW of 41 MHz; insertion loss of 12 dB

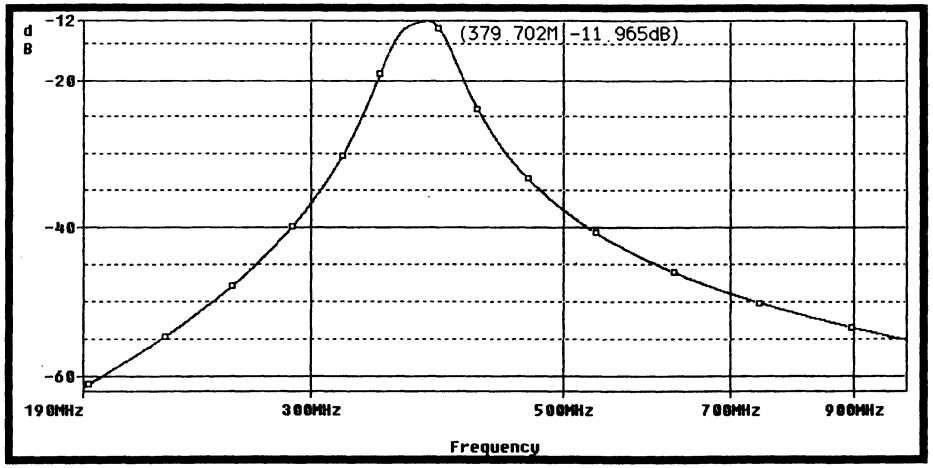


Fig. 4.3.2-5. Simulated response, 190 MHz – 1 GHz.

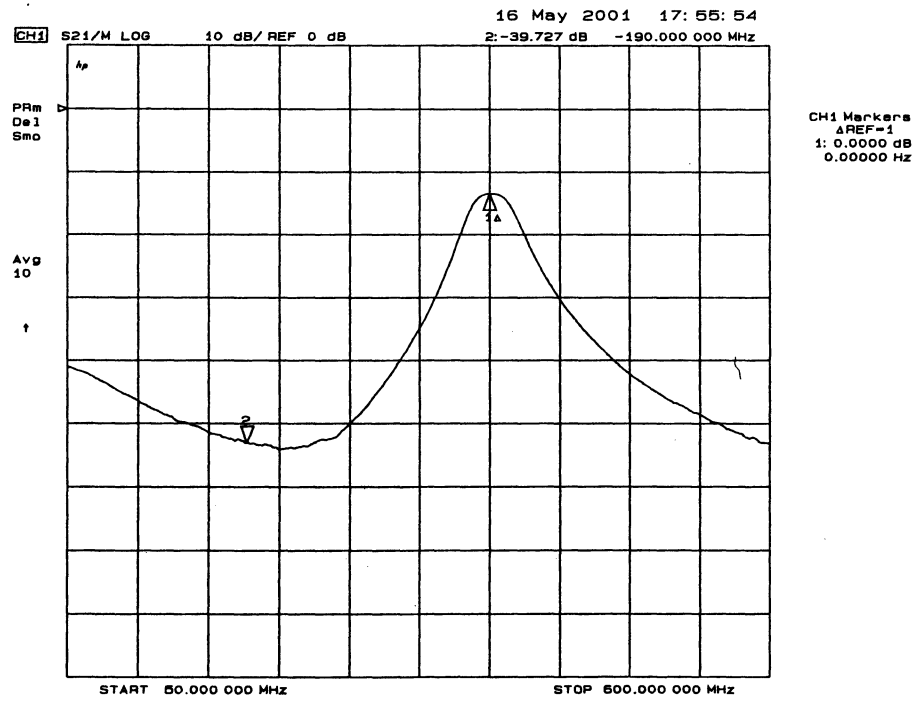


Fig. 4.3.2-3. Measured filter response, 50 – 600 MHz.

Meeting Expectations / Conclusions

Design Constraints

- Finite inductor Q; stray capacitance; discrete valued components; financial limitations

Lessons Learned

- Design of a low-order BPF at high frequencies is particularly challenging
- Many of our trials contained unrealistic component values, were extremely sensitive to component variation, or did not account properly for finite inductor Q

Expansion and Improvement

- Examine the quadrature modulator, VGA, or power amplifier in the TX path
- Implement the IF BPF on-board a working W-CDMA phone to determine the practical advantages and disadvantages in an uncontrolled environment
- Future senior design teams will benefit from an early start on researching RF basics prior to the beginning of their project

Conclusion

- Filter design specifications have satisfied all technical requirements under the given constraints
- The UCR / Maxim Senior Design Project has been a very valuable learning experience by providing the team "real world" engineering problem solving techniques and has helped establish networking foundations in the corporate environment.

Problem Statement

- Four clean Local Oscillators (LO) are needed for down- and up-conversion of our Radio and Intermediate Frequency signals in the ranges from 2360 MHz to 380 MHz.

Solution

- An Integer-N Phase Locked Loop design will be used to tune a Voltage Controlled Oscillator that will supply the transceiver with the proper LO.

- A well designed loop filter is the key to provide a clean signal. Our loop filter is a third-order lead-lag passive low-pass filter within our Phase Locked Loop.

Goals

- Determine the main criteria behind each of the Phase Locked Loops / Local Oscillators.

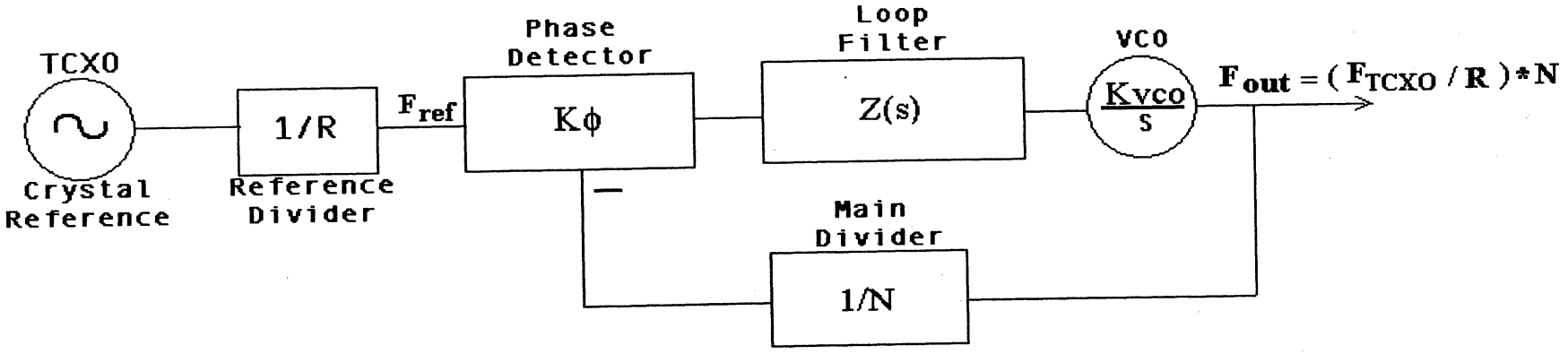
- Design the control loop components and parameters given some specifications for the radio operation.

- Justify the frequency plan and understand how it impacts the radio.

Method of Solution

Components	Pros	Cons
• Integer-N Phase Locked Loop	• Low Power • Small Circuitry	• High division ratio – significant degradation in phase noise performance
• Fractional-N Phase Locked Loop	• Improves phase noise • Improves loop bandwidth	• More circuitry • Adds spurious noise
• Crystal oscillator	• Clean sinusoidal signal	• Natural resonant frequency way below 100 MHz
• LC Oscillators	• None	• Impossible to design stable and accurate at such high frequency
• Phase Frequency Detector (PFD)	• Guarantees PLL to lock regardless of loop filter	• Adds noise
• EXOR Gates	• Good phase tracking for symmetrical signals (square wave)	• Poor performance when signal is not symmetrical
• JK flip flops (JK/ff)	• Symmetry of signal is irrelevant since JK/ff work on rising edge	• Pull-in range stays severely limited (No integrating term)
• Low-Pass Filter	• Simple, low cost, low phase noise	• Adds noise
• Voltage Control Oscillator	• Tuned to very high frequencies	• Tendency to drift

INTEGER-N ARCHITECTURE
PHASE-LOCKED LOOP



Loop Specificatons

$TCXO = 19.68MHz$ $Kvco = 15MHz/V$

$F_{ref} = 75kHz$ $K\phi = 2.1mA$

$F_{out} = 760MHz$ $R = 262.4$

$Fa = 500Hz$ $N = 10133.3$

$Ts = 5ms$

Transfer Function

$$\text{Forward loop Gain} = K\phi\, Z(s)\, Kvco / s = G(s)$$

$$\text{Closed Loop Gain} = \frac{G(s)}{1 + G(s)/N}$$

$$Z(s) = \frac{s(C2*R2)+1}{s^2(C1*C2*R2)+s(C1+C2)}$$

Simulation vs. Experiment

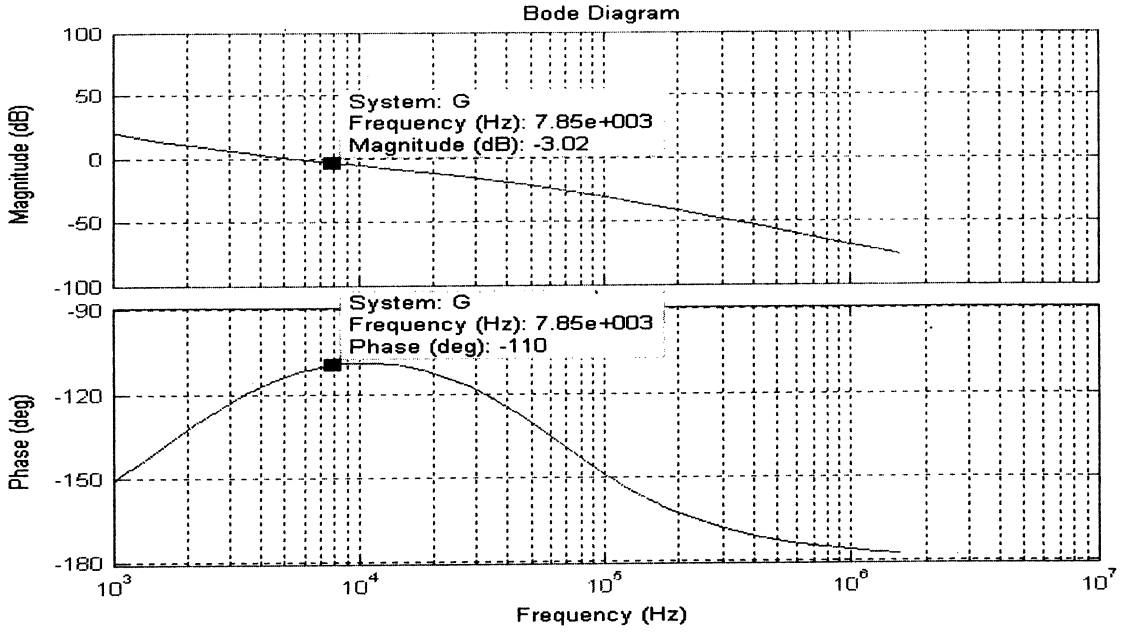


Fig. 4.2.3.2-6. Simulation of loop bandwidth.

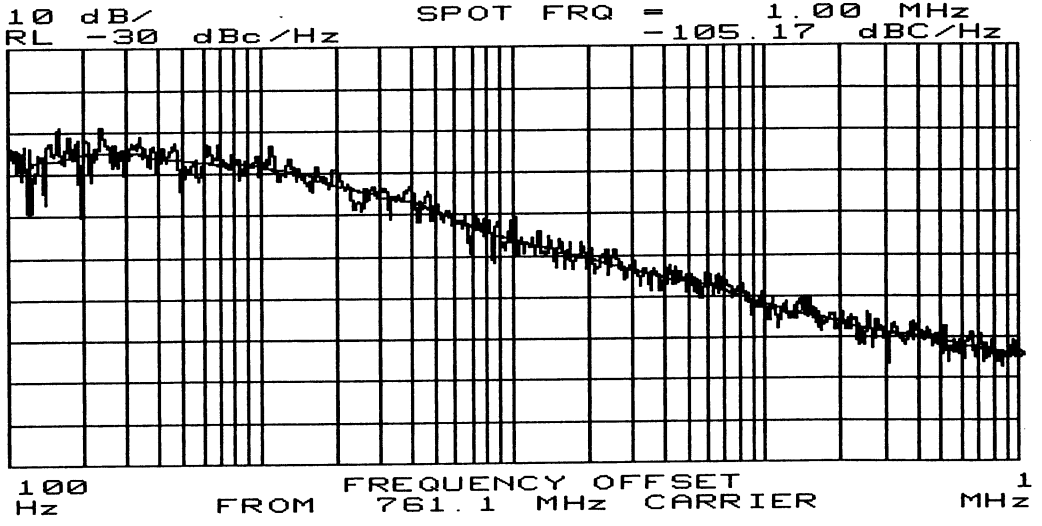


Fig. 4.2.3.2-4. Measured loop bandwidth.

Simulation

K_{vco} = 15 MHz/V

K_{ϕ} = 2.1 mA

F_{ref} = 75 kHz

Bandwidth = 7.85 kHz

Phase Margin = 70°

Experiment

K_{vco} = 30 MHz/V

K_{ϕ} = 175 µA

F_{ref} = 75 kHz

Bandwidth = 1.5 kHz

Phase Margin = 78°

Meeting Expectations

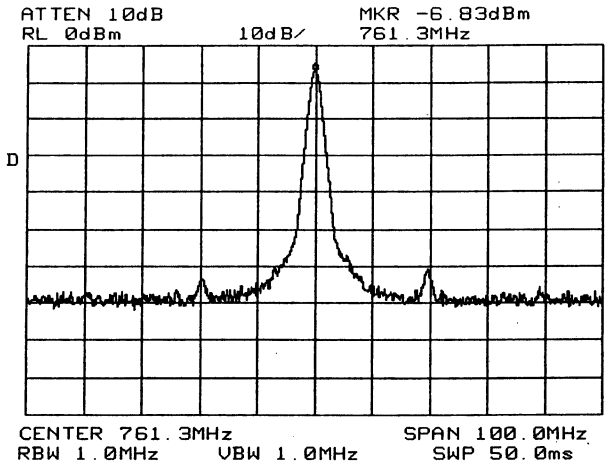


Fig. 4.2.3.2-1. Locked PLL with center at 761.3 MHz and spurs at multiples of 19.68 MHz.

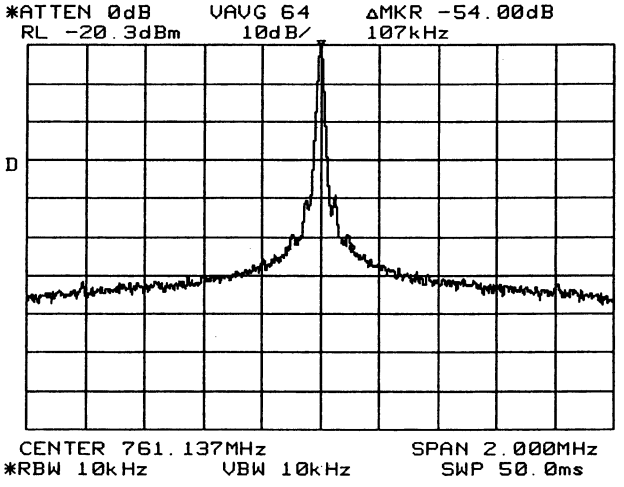


Fig. 4.2.3.2-2. Close-in phase noise.

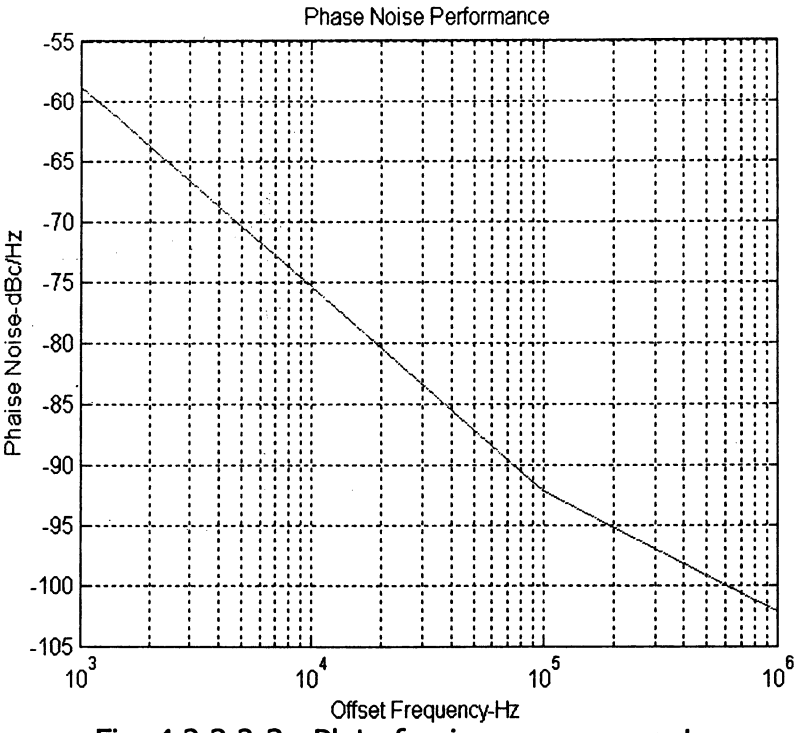


Fig. 4.2.3.2-3. Plot of noise measurements at different offset frequencies.

	Desired	Achieved
Spur Attenuation	– 58.16 dBc/Hz	– 58 dBc/Hz
Phase Noise Attenuation (1 kHz offset)	– 80 dBc/Hz	– 58.3 dBc/Hz
Settling Time	5 ms	5 ms

Conclusion

Mission Accomplished

- After a very exciting 6 months, we have successfully accomplished our mission.

Future Improvements

- Pre-developed time line that gives explicit tasks and dates for which each task should be completed
- Indefinite access to the proper test equipment
- Implementing the third-order loop filter
- Making charge pump current a point of concentration so that power saving techniques can be studied and implemented

Lessons Learned

- Selection of the proper components can have a serious effects on the system
- Part of a design is not only understanding the concepts, but also dealing with non-ideal properties, which adds additional constrains in our design that we didn't necessarily take into account when running the simulation.

Elements of Design

Issue	Effects of our design
Economic Factors	There are many economic factors that influence a design. We have covered a cost analysis in Chapter Five, which gives us a good idea of what it would cost to mass-produce our design. Though this is a good rough estimate, the fact that there are other companies out there wanting to make money from producing a similar product is another factor that must be considered. Through supply and demand, many companies may not be competitive enough to survive and this would cause loss of jobs, however it would also supply the customer with superior products.
Safety	While the actual manufacturing processes involved with mass-producing our design may involve some drawbacks to the environment, all responsibilities fall on the manufacturer to conduct itself accordingly. As for our responsibilities when making a prototype, all known precautions were taken to ensure the safety of all involved.
Reliability	No extensive tests were made to ensure the long-term reliability of our design. However, to the best of our knowledge, we have no reason to believe that our design would not be worthy of long-term use.
Aesthetics	The prototypes that were made during this project were constructed for test purposes only and were not optimized for appearance. They were merely meant to provide us with knowledge and skills related to our particular design. With further design and testing a prototype worthy of being produced, which not only works to designed specifications, but also looks good, could be achieved.
Ethics	In reviewing the IEEE Code of Ethics, we have done nothing but try to better our understanding of this technology as well as help each other along the way, working together as a team. We often criticized and complimented each other during our time working together. Throughout this project, we have conducted ourselves in nothing but a professional manner and have done nothing to harm the reputations of others involved in this project. By reporting all of our work and findings in this report, we have given credit where needed and we have presented our findings with the utmost honesty.
Social Impacts	With many people desiring portable communications devices in today's fast-paced world, our design will play a major role in furthering the wants and needs of these types of people.

Cost Analysis / Marketability

- Prototype Cost:
  - Parts $530
  - Software $2,920
  - Direct Labor $3,600
  - Capital Equipment $0

- Production Cost of 500,000 Units:
  - Parts $796,360
- Cost (sub-total) $803,410
- Overhead Cost $40,170
- TOTAL COST $843,580

- Expected Sales 490,000 units
- Estimated Price/Unit $1.72
- Current Price Per Unit $2.00
- Savings Per Unit $0.28
- TOTAL SAVINGS $137,200
- Hiring Bonus Cost $60,000
- **Expected Total Profit** **$77,200**

Acknowledgements

- We would like to give special thanks to the following extremely helpful people:
  - Dave Devries, Maxim Corporation
  - Warren Hauff, Maxim Corporation
  - Gary Huang, Maxim Corporation
  - Bob Kelly, Maxim Corporation
  - Daniel Kong, Maxim Corporation
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  - Zhongmin Yu, Maxim Corporation

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- Finally, we thank our faculty advisor Professor Mansour Eslami who made this entire project possible.