IV. Final Report

[1] Karl Doering, Nadim Addus, Heath Deuel, Steven Gyford, Oscar Servin, Michael Wilson, entitled - ***Wireless Communication Systems Block Analysis and Design.*** The Technical Faculty Advisor for this project was the author, in collaboration with Mr. Dave Devries, Mr. Bob Kelly, and Mr. Daniel Kong of the Maxim Corporation.

We have selected this item, because of our personal involvement in its creation. We hope that this report would be of both interest and help to our future students.

More importantly, we have included this project to emphasize that a multi-team project must be assembled coherently. As stated in the opening remarks of Section II of this part, senior design projects should be the result of a marriage between engineering programs and industry, a prospect that is fruitful for all parties involved. But that is not an easy task to arrange, since people in industry are under different sets of constraints from their counterparts in academia. In some instances, it may require decades of pursuing and working relationships with industry to build enough trust to let our students in their facility, nevertheless it can be done and should be explored.

Senior design projects may provide golden opportunities for a qualified faculty member to develop and operate a successful research enterprise continually, provided that projects are selected coherently and with an eye to the future. Thus, those who shy away from contributing to this activity are missing a remarkable chance to enhance their research productivity while helping undergraduate students. This instructor has enjoyed the experience of working with many of these young students specially when they come up with their "awesome" results.

Just as any good story, there is a time that one must say farewell and leave the reader. We close by saying that it has been truly an enjoyable year to work on this project. Best wishes to all you young people and so long until we meet again.

Final Report of Senior Design Project
Winter / Spring 2001
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Wireless Communication Systems Block Analysis and Design

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Executive Summary – We analyze and improve upon a Wideband Code-Division Multiple Access transceiver, dividing the task at the block level into three portions: receive, transmit, and frequency synthesis. Each portion is attacked by a team of two EE senior design students at UC Riverside, working with an industry engineer from Maxim Integrated Products. After performing preliminary research and analysis to become familiar with the reference architecture and design issues involved, each team works on a particular aspect of the design as described herein.

The design problem facing the receiver team is to improve adjacent interferers rejection at the I/Q baseband output of the receiver. To accomplish this, an active fourth-order low-pass Butterworth filter is designed, simulated, implemented, and tested. Of the numerous filter types available, this one is chosen for its gain, high linearity, maximally flat response in the pass-band, and minimal number of components required. The final design uses a Sallen-Key topology and provides 6 dB of gain in the pass-band, with a corner frequency of 3 MHz. A spreadsheet is created for performing the necessary calculations, and *PSpice* is used for simulation of the design. The circuit is realized in hardware, its characteristics extracted with an RF network analyzer, and fine-tuned to meet specifications. The realized circuit obtains 39 dB of attenuation at 15 MHz, meeting the most stringent specifications for the design.

The goal of the transmitter team is to design an IF filter in the transmit path of the radio. The filter must have lower cost and improved performance over the currently used SAW filter, in rejecting harmonics and other spurious signals generated by the quadrature modulation process. To meet the goal, analysis is performed to determine filter specifications and a passive second-order narrowband band-pass Butterworth filter is designed, simulated, and verified in hardware. A capacitive-coupled resonator architecture is chosen for its design characteristics and ease of tuning. A spreadsheet is created to automate design calculations and *PSpice* is used for simulation. Because of the high frequency range involved, special care is taken to account for finite inductor Q and stray capacitance present in the physical circuit. The prototype obtains a 3 dB bandwidth of 35.4 MHz, and 40 to 44 dB of attenuation at 190 and 760 MHz, respectively.

The design problem facing the frequency synthesizer team is to provide four clean local oscillators for the down- and up-conversion of the RF and IF signals in both the receive and transmit paths. To accomplish this goal, phase locked loops are used to produce clean signals at much higher frequencies than obtainable from crystal oscillators. An Integer-N PLL architecture is chosen for its low power consumption, small physical size, and economy. A third-order lead-lag passive low-pass filter is designed because the loop filter is key to generating an output with minimum noise. Key criteria include the amount of phase noise generated, the amount of spurious noise suppressed, and the time taken to lock to a specified frequency. *Matlab* code is written and used to calculate key values and to run simulations for given system specifications. The final loop filter design for the transmitter IFLO features a 1.5 kHz bandwidth, netting –58 dBc/Hz phase noise attenuation and spurious noise at a 1 kHz offset with a settling time of 5 ms.

Keywords – Wireless communications, Wideband Code-Division Multiple Access, Transceiver architecture, Low-pass filter design, Band-pass filter design, PLL design.

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Chapter One – Introduction

1.1. Introduction

This project involves the analysis of and improvement upon a Wideband Code-Division Multiple Access transceiver. We divide the tasks among ourselves at the block level into three portions: receive, transmit, and frequency synthesis. Each portion is attacked by a team of two EE senior design students at UC Riverside working with an industry engineer from Maxim Integrated Products. After performing preliminary research and analysis to become familiar with the reference architecture and design issues involved, each team works on a particular aspect of the design as described in this paper.

In the remainder of this chapter we give a brief historical perspective followed by a glossary of acronyms and abbreviations we frequently use. Chapter Two introduces the specific design problem of each team, providing a general problem statement followed by precise design specifications. In Chapter Three the method of solution for each team is presented, beginning with an overview of the chosen design solution among a variety of possible solutions. The designs are presented in detail, with the key features and functions of each component emphasized. In Section 3.3 alternative approaches to the design problem and the tradeoffs involved are examined more closely. Chapter Three closes with insight into some of the valuable lessons learned in the design process.

In Chapter Four, each team conducts a thorough evaluation of its design. Results from both *PSpice* simulations and hardware measurements are presented, compared, and contrasted. Both strengths and weaknesses in the design are stated and evaluated with respect to alternative methods of solution available.

Chapter Five deals with key administrative issues, including a complete cost analysis and a description of task organization and scheduling. In Chapter Six, the design constraints are reexamined. Discrepancies in the results from the original design specifications are examined and accounted for, and the corresponding effect on the final outcome is analyzed. The chapter closes with a table addressing elements of design, including economic factors, safety, reliability, aesthetics, ethics, and social impacts.

We conclude in Chapter Seven by discussing the impact of our work and possible future expansions.

1.2. A Historical Perspective

Since 1901, when Marconi first transmitted radio signals across the Atlantic Ocean, radio communication has progressed dramatically [14]. Early radio architectures were very simple and could be easily built out of one's garage with a few components. As radio communication became more popular and more and more communication by radio took place, people soon realized that the electromagnetic spectrum is a precious resource which must be shared among all involved. Frequency plans were created, and higher and higher frequency ranges were explored.

Design techniques advanced, and new architectures were developed to handle the problems encountered with higher-frequency designs.

Early radios worked in the kHz range, but today's W-CDMA architecture operates in the GHz range. Simple LC filters cannot be built to select narrow channels at such high frequencies, and techniques such as down-conversion, up-conversion, and intermediate frequencies are required, leading to the superheterodyne architecture commonly used today.

1.3. A Glossary of Acronyms and Abbreviations

3GPP	Third Generation Partnership Project
ACS	adjacent channel selectivity
Atten	added spurious attenuation due to R_3 and C_3
CDMA	code-division multiple access
dBc	decibels relative to carrier
dBm	decibels referenced to one milliwatt
DSP	digital signal processor
F_{comp}	comparison frequency
FDD	frequency division duplex
F_{out}	output frequency of the VCO
F_{ref}	crystal reference frequency
I/Q	in-phase and quadrature
IC	integrated circuit
I_{cp}	phase detector / charge pump gain
IF	intermediate frequency
IFLO	intermediate frequency local oscillator
IP_3	third-order intercept
K_{VCO}	VCO gain (tuning sensitivity)
LNA	low-noise amplifier
LO	local oscillator
Mcps	million chips per second
N	N divider value
PCB	printed circuit board
PFD	phase frequency detector
PLL	phase locked loop
Q	quality factor
R	R divider value
RF	radio frequency
RFLO	radio frequency local oscillator
RMS	root mean square (reference to phase noise)
Rx	receive
SAW	surface acoustic wave (filter)
SMT	surface-mount technology
Tx	transmit
TXCO	temperature-compensated crystal oscillator
VCO	voltage-controlled oscillator
w_c	true closed-loop bandwidth (rad/s)
W-CDMA	wideband code-division multiple access

Chapter Two – Design and Technical Results

2.1. Introduction

Over the course of six months, the Maxim / UCR (Maxim 6) project has studied a transceiver on a range of issues. These issues have been examined from the transmit, receive and control perspectives, based upon a reference design of a W-CDMA quadrature superheterodyne transceiver.

This chapter contains the problem statement and the presentation of the desired system specifications. The purpose of Section 2.2 is to discuss what our problem entails and give the reader a general understanding of what we are trying to solve. Section 2.3 illustrates the specifications for each component.

2.2. Problem Statement

Here we describe the technical problem to be solved for each of the three components of the transceiver, namely the receiver, the transmitter, and the frequency synthesizer components.

2.2.1. Receiver

The receiver portion of the overall project requires us to verify that the receiver in the W-CDMA superheterodyne transceiver reference design meets the Third Generation Partnership Project (3GPP) technical specifications through analysis of the system components. For this analysis we include factors influencing the architecture such as intermodulation, linearity, noise figure, and gain. Calculations are done to determine the effect of these factors on the cascaded system, as limitations of system performance due to these factors require the optimization of the design process to achieve better RF performance.

Once the receiver architecture has been validated, the second goal of this part of the project is to design a low-pass filter to be implemented at the output of the quadrature demodulator in the baseband I/Q signal path to further improve adjacent channel interferers rejection. Requirements for defining the filter characteristics are derived from the 3GPP specifications. These requirements determine the design of the filter, which are verified through simulation first, and secondly through measurements of a physical circuit's performance.

2.2.2. Transmitter

The efforts of the transmitter portion of the W-CDMA transceiver project are divided into two stages. The first stage is a comprehensive signal path analysis of the transmitter portion of the Maxim W-CDMA reference design in [9]. The signal path analysis enables us to master many of the fundamental concepts required in the design of a state-of-the-art radio transceiver system. The second stage of the project is to use these concepts of radio frequency design in combination with advanced techniques of high frequency filter design to design and implement a band-pass filter to replace the SAW / BPF in the IF portion of the transmitter.

2.2.3. Frequency Synthesizer

The reference design for the transceiver contains three PLLs to produce the four local oscillator signals that are needed. The primary result for the frequency synthesizer portion is to provide a clean signal for the transmit and receive path for up- and down-conversions of RF to IF signals [24]. We have designed the loop filter for all three PLLs and were lucky enough to test one. We have demonstrated that a fairly clean signal, which maintains a range of 30 kHz, can be generated by our VCO by implementing a good loop filter. An initial prototype of the TxIF / LO loop design has demonstrated that a signal of 760 MHz, with –58.83 dBc phase noise and negligible spurious noise can be produced to drive our modulator while the RF / LO up-converts the modulated carrier to the on-channel RF frequency for antenna transmission.

The goals for this project are threefold.

We first need to determine the main criteria behind each component of the PLL / LO. In order to meet our goals, it is necessary to understand and select the correct component of our PLL. When selecting the correct components we need to take into consideration the application of our design and specification of our system.

Understanding the frequency plan and justifying its effects on the radio is the second thing that is accomplished. The main focus of our design revolves around this idea. Understanding how and why the frequency must be down- and up-converted in certain areas is inevitable for the correct functionality of our radio [14].

Lastly, we need to calculate the control loop parameters given some specifications. The way that we will physically get a clean local oscillator to be mixed with our RF to provide the proper IF signal is by not only selecting the proper PLL components, but also having a good filter design. Selection of good components will help to avoid phase noise and the design of a good loop filter will allow us to eliminate spurious noise [1]. Further discussion on noise is to follow in the next chapter.

2.3. Design Specifications

Here we provide precise specifications for each of the components to be designed.

2.3.1. Receiver

The specifications that describe the attenuation characteristics for the low-pass filter, which show us the channels, their frequency offsets and the attenuation required at those particular frequency offsets, are given in Table 2.3.1-1. These characteristics are taken from the 3GPP technical specifications.

Table 2.3.1-1. Frequency and attenuation characteristics.

Channels	Freq Offset (MHz)	Att. LPF (dBc)
CH-Wanted	0	0.0
CH-Adjacent	± 5	-10.0
CH-In-Band-Blk	± 10	-25.0
CH-In-Band-Blk	± 15	-45.0
CW-Out-Band1-Blk	>± 15	-45.0
CW-Out-Band2-Blk	>± 60	-55.0
CW-Out-Band3-Blk	>± 85	-55.0

In addition to these specifications, we must also decide on a filter type, implementation, topology, and order. Another specification requires the filter to have a single-ended output as well as a voltage gain of 2 V in the pass-band. Since we are filtering both the in-phase and quadrature signals, two filters are needed. However, in order for the signals to be processed properly, they are required to be no more than 5 degrees out of phase and be within 0.5 dB of each other in magnitude. The final criterion to consider is the type of filter to be used for our design.

The first specifications that the 3GPP paper describes are the frequency bands and channel arrangement. The chip rate is set to 3.84 Mcps for all the information provided in the specifications [12]. For the receiver portion of the transceiver, the frequency band is set to 2110 to 2170 MHz with a separation of 190 MHz between the transmit and receive bands. Channel spacing is set to 5 MHz with a channel raster of 200 kHz [25].

The next set of specifications that are described are the requirements for the receiver. These are the specifications that will be used to determine whether or not the entire receiver chain is valid. The dedicated physical channel power required is $P_{DPHC\_Ec} = -117$ dBm / 3.84 MHz [25]. This is the minimum power for a signal that this receiver is required to be able to detect. In addition to the minimum levels, the maximum level is also defined to be –25 dBm / 3.84 MHz [25]. From knowing the minimum power level required by the receiver, we can determine that the noise figure (NF) for the entire receiver is 9 dB [12]. With a loss of 4 dB in the duplexer, the NF then becomes 5 dB for the rest of the receiver chain [12].

Adjacent channel selectivity (ACS) is another important factor to consider in that it determines whether or not the receiver can or cannot receive a desired signal in the presence of an adjacent channel signal. The specification for the ACS is used to determine the selectivity of the receiver at a frequency offset of 5 MHz. With a desired signal power of $P_{DPHC\_Ec} = -103$ dBm / 3.84 MHz and an adjacent signal power $P_{AC1} = -52$ dBm / 3.84 MHz, we can determine the selectivity of the receiver [12]. First the acceptable interference power is found, then the selectivity is found by subtracting the acceptable interference power from P_{AC1}. This yields a selectivity of 33 dB at ±5 MHz [12].

Another requirement of the receiver is the ability to receive signals in the presence of an unwanted interferer. These unwanted interferers are commonly called blockers. There are two types of blockers: in-band and out-of-band blockers. The minimum requirements for these blockers are described in the 3GPP specifications. The in-band blockers are centered at frequency offsets of ±10 MHz and ±15 MHz. Signal powers for the in-band blockers are –56 dBm / 3.84 MHz and –44 dBm / 3.84 MHz respectively [25]. Out-of-band blockers are located at frequency offsets of ±15 MHz, ±60 MHz, and ±85 MHz. Signal powers for the out-of-band blockers are –44 dBm / 3.84 MHz, –30 dBm / 3.84 MHz, and –15 dBm / 3.84 MHz respectively [25]. These blocking requirements can be used to determine the selectivity of the receiver at the frequency offsets described above.

Another specification that needs to be taken into consideration is the receiver's ability to receive the desired signal in the presence of third-order mixing products. Such specifications are known as intermodulation characteristics. The minimum requirements are defined for frequency offsets of ±10 MHz and ±20 MHz. The power of the signals at these frequencies is –46 dBm / 3.84 MHz [25]. From these specifications the selectivity of the receiver is determined to be 58 dB at 10 MHz and 20 MHz [12].

2.3.2. Transmitter

The signal path analysis performed on the transmitter and the design of the BPF for the IF portion of the transmitter are each accomplished with the consideration of certain required specifications. The signal path analysis is performed with the requirement for the transmitter to provide a signal output at a frequency ranging between 1920 MHz and 1980 MHz for a local oscillator up-convert frequency input range between 2300 MHz and 2360 MHz, respectively. Additionally, the transmitter output is required to maintain a minimum output level of +23 dBm with a minimum output level range of 75 dB over the entire operating frequency range [9].

The design specifications for the IF / BPF are derived from the signal path analysis performed on the transmitter. The IF / BPF prototype is used to replace the IF / SAW / BPF used in the reference design illustrated in [9]. To meet the design requirements, calculations of all spurious frequencies resulting from intermodulation and up-convert mixing functions are identified. The specifications of the filter design require the filter to have a center frequency of 380 MHz, an insertion loss of 8 to 12 dB, a 3 dB bandwidth of 6.8 MHz, and a minimum attenuation level of 30 dB at 360 MHz and 400 MHz. The design specifications are summarized in Table 2.3.2-1.

Table 2.3.2-1. Transmitter design specifications.

Signal Path Analysis Specifications	
Operating Frequency Range	1920 MHz - 1980 MHz
Output Level	23 dBm
Minimum Output Level Range	75 dB

Filter Design Specifications	
Center Frequency	380 MHz
3 dB Bandwidth (minimum)	6.8 MHz
Attentation at 190 MHz	37 dB
Attenuation at 760 MHz	40 dB
Differential Input Impedance	400 Ohms
Differential Output Impedance	600 Ohms

2.3.3. Frequency Synthesizer

Three PLLs are used in the reference design of a superheterodyne transceiver that we use in our design. Each PLL uses the system clock crystal oscillator at 19.68 MHz to generate a LO signal displaying unique characteristics. Each LO signal must contain an –80 dBc/Hz phase noise attenuation.

2.3.3.1. Radio Frequency Local Oscillator (RFLO)

This LO must tune over a range of 2300 MHz – 2360 MHz while having a switching speed less than 1 ms. This LO is used for both transmit and receive paths. The comparison frequency for this PLL is restricted to the channel spacing of the incoming RF signal, which is 200 kHz.

2.3.3.2. Receive Path – Intermediate Frequency Local Oscillator (Rx-IFLO)

This LO is fixed and therefore has no tuning range. The output frequency is 380 MHz. The switching speed is not an essential element in the performance of this PLL and therefore the design constraint can be relaxed to 5 ms. The comparison frequency for this PLL is determined by the designer.

2.3.3.3. Transmit Path – Intermediate Frequency Local Oscillator (Tx-IFLO)

This LO is also fixed, at 760 MHz, with a switching speed of 5 ms. The comparison frequency for this PLL is determined by the designer.

Table 2.3.3.3-1. System specifications.

Local Oscillator	V_{out} (MHz)	Switching Speed	Phase Noise Attenuation
RFLO	2300 – 2360	1 ms	–80 dBc/Hz
Rx – IFLO	190	5 ms	–80 dBc/Hz
Tx – IFLO	760	5 ms	–80 dBc/Hz

Chapter Three – Method of Solution

3.1. Introduction

This chapter presents our designs as well as reasons to why we made the engineering choices that we encountered. Section 3.2 details the architectures of our designs and advantages and disadvantages of the chosen architectures. Components used in the design are presented along with reasons to why these were selected. In Section 3.3 we continue our discussion of other methods to approach the solutions and explanations as to why these were not picked for our design. Section 3.4 states the lessons learned in selecting components for our architectures.

3.2. Our Design

In this section each of the three teams presents its design, emphasizing the key features and development.

3.2.1. Receiver

The implementation of the low-pass filter is a key factor that must be taken into consideration. A fourth-order Butterworth filter is selected for our design. This implementation is selected for its maximally flat magnitude response in the pass-band. Once the filter type is determined, the filter topology is selected. The next specification we take into consideration is the type of filter that is used. We choose to use an active filter for its linearity and lack of inductor in the circuit. This simplifies our analysis and the overall approach to our design. In the next step, we use one of the reference books [18] for filter design by which we take the following approach:

1. Determining requirements.
2. Finding filter or design that meet these specifications.
3. Normalizing.

Filter tables are used to simplify our circuit design, based upon the idea of constructing a fourth-order Butterworth filter by cascading two second-order filters. The tables contain scaling factors for the corner frequencies and the required Q for each stage of our filter. After completion of these tasks we are able to calculate the circuit component values required. Our requirements for the filter were already given in Chapter Two of this report. So given those requirements, our next step is to calculate the order (n) of the filter using Equation 3.2.1-1.

$$n = \frac{\log_{10}\left(\frac{\sqrt{10^{\left(\frac{A(dB)}{10}\right)} - 1}}{\sqrt{10^{\left(\frac{A_c(dB)}{10}\right)} - 1}}\right)}{\log_{10}\left(\frac{F_s}{F_c}\right)} \qquad (3.2.1\text{-}1)$$

Factors affecting this filter order include: cutoff frequency F_c, attenuation at cutoff A_c (dB) [4], the frequency F_s, and attenuation at stop-band A_s (dB). All these specifications must be met. After calculating filter order, the filter element values are looked up in a filter table. The topologies are given and we are able to come up with the circuit as shown in Fig. 3.2.1-1.

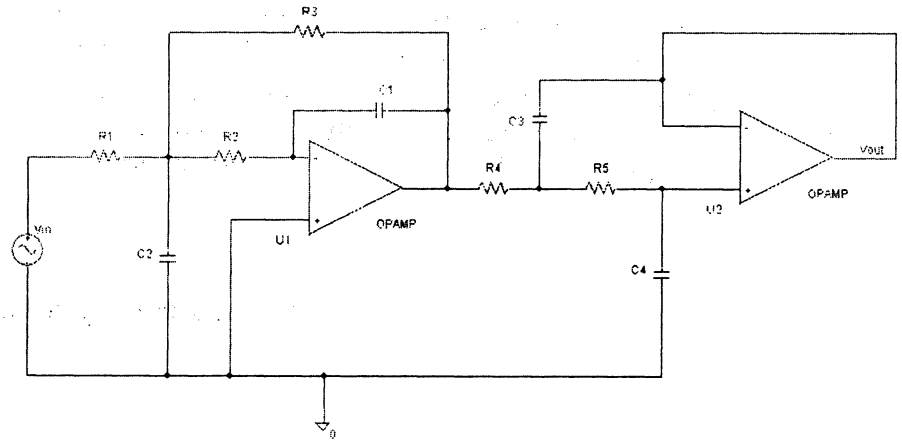

Fig. 3.2.1-1. Circuit diagram of the low-pass filter.

3.2.2. Transmitter

Our design consists of a passive band-pass IF filter in the transmit path as a replacement to the standard SAW filter originally present. Let us first examine the purpose of this filter.

From the W-CDMA reference design [9], this filter functions to suppress harmonics of the IF signal, resulting from the quadrature modulation process as well as any nonlinearities in the IF variable gain amplifier (VGA). Assuming the baseband I and Q channels are band-limited to, say, 5 MHz, at an IF of 380 MHz, undesired mixing products are expected to fall near DC and around 760 MHz and up. Therefore, the sharp response of the IF / SAW filter may not be necessary. For reasons of cost, replacing the SAW filter with a low-order LC filter is an attractive option.

In fact, at the frequencies at which harmonics are expected, a simple LC filter may even surpass the performance of a SAW filter. SAW filters tend to have rather high insertion losses and relatively flat response outside the pass-band. However, with an LC band-pass filter, attenuation generally increases the farther away from the center frequency.

Given the high center frequency at which this filter must operate, designing a practical passive narrowband filter is quite a challenge. Component values (and in particular inductor Q) are often either very sensitive or unrealizable, or both. There are a wide variety of filter types and design techniques available, including approximations, normalizations, and transformations as given in [7]. After much reading and experimentation with circuit simulators, the capacitive coupled resonator configuration was chosen. Such an architecture is desirable given our specifications, as it generally yields more practical values than low-pass to band-pass transformations and tuning is simplified since all nodes are resonated to the same frequency [18].

To determine the necessary order of the filter, we make use of an Excel spreadsheet, which we designed specifically for this purpose. This eliminates the tedious calculations required as well as the possibility of error in calculation, and makes it very easy to "feel out" the design by instantly observing the effects of modifying key parameters.

Our design process is as follows. The upper and lower pass-band frequencies f_u and f_l (respectively) are entered into the spreadsheet. The center frequency $f_0 = \sqrt{f_l f_u}$, pass-band bandwidth $BW_{3dB} = f_u - f_l$, and pass-band Q, $Q_{bp} = f_0 / BW_{3dB}$ are then filled in. Before continuing further, we examine Q_{bp} to determine whether the final circuit will be realizable. (If not, then either the specifications must be relaxed or a different implementation must be used.)

Next, the type and order of the filter must be determined. This task is accomplished based upon the band-pass steepness factor A_s = (stop-band bandwidth) / BW_{3dB}, the complexity (order) required to meet the specifications, and by examining reference design tables in [18] to choose a filter type based upon the desired phase and magnitude response characteristics.

Based upon our specifications and the response characteristics available, we initially examine a fourth order 0.1 dB Chebyshev resonator, a third-order traditional Gaussian to 6 dB resonator, and a second-order Butterworth resonator. Since we want a low-cost filter with flat phase response in the pass-band, high attenuation far from f_0, non-critical A_s, and a circuit simple enough to prototype with 0402 and 0603 surface-mount components, we choose the second-order Butterworth capacitive coupled configuration, Fig. 3.2.2-1.

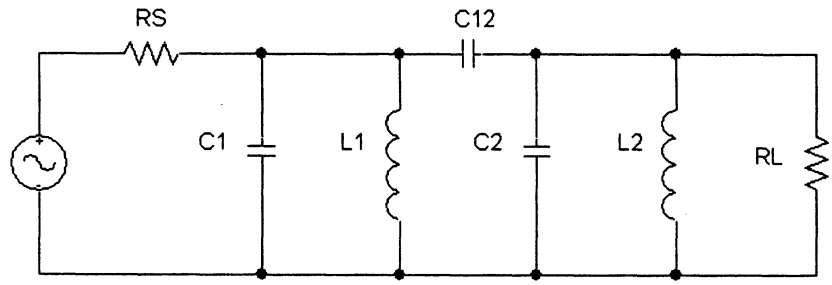

Fig. 3.2.2-1. Second-order base circuit configuration.

We obtain component values for this circuit using standard design tables and equations given in [18], and simulate the circuit in *PSpice*, producing the waveform in Fig. 3.2.2-2.

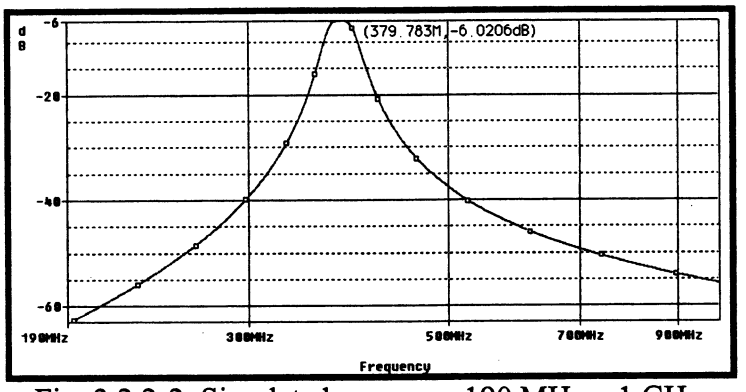

Fig. 3.2.2-2. Simulated response, 190 MHz – 1 GHz.

We then repeat the simulation a number of times, using standard component values at the limits of their specified tolerances, to obtain some indication of how sensitive the design is relative to component variations. Finally, we add additional capacitances and resistances to account for finite inductor Q, and stray capacitance present in a physical implementation, and we transform the circuit to its differential form. Our final circuit is shown in Fig. 3.2.2-3. (It is to be noted that the unlabelled components are not physically present in the circuit; these account for the effects just mentioned.)

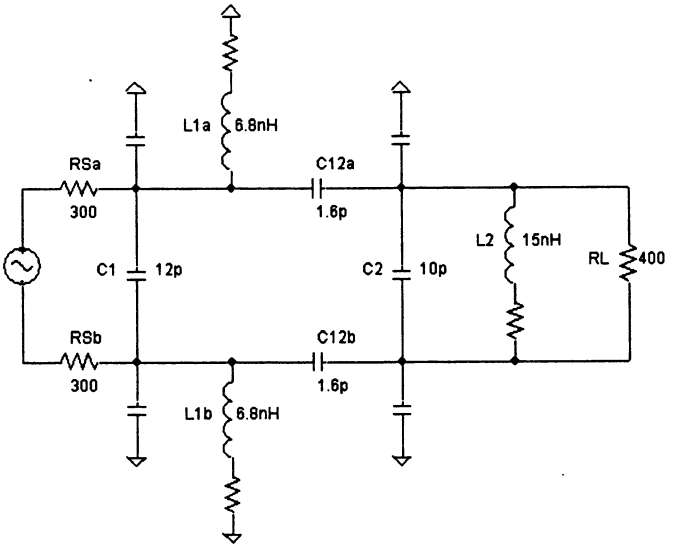

Fig. 3.2.2-3. Final circuit, after transformation to differential form.

3.2.3. Frequency Synthesizer

The best way to approach our problem is to use an Integer-N phase locked loop [22]. The components that make up our Integer-N / PLL are a crystal oscillator, phase-frequency detector, a VCO, low-pass loop filters, and dividers. The RF and IF / LOs will be similar componentwise, as well as in functionality.

A phase locked loop is a negative feedback loop, which tracks the error and corrects itself as changes are made to the input of the system. For phase locked loops, the quantity of interest

is the phase of the input and output. The purpose of the phase locked loop (PLL) is to track the phase of the input and to try to match it, so that the output phase is the same [3]. An ideal PLL has no change in phases.

The simplest architecture of a PLL consists of three blocks. The first is the Phase Detector. The function of the Phase Detector (PD) is to detect the phase of the input. The PD tries to measure the phase error between input and output signals. The next block is a Loop Filter, normally a low-pass filter, but that depends on the type of PLL that is being built (more on different types of PLLs in Section 3.3.3). The purpose of the filter is to suppress the higher-order harmonics. The last block in our PLL architecture is the VCO. The Voltage Controlled Oscillator is used to control the phase of the output.

The Integer-N Phase Locked Loop is a basic feedback loop that can produce a low-noise local oscillator (LO) signal at a specific frequency, which can be mixed with an incoming Radio Frequency (RF) signal. A PLL's performance is characterized by how fast it locks to a new frequency and by how much noise is exhibited by the output, also known as phase noise [3]. The Integer-N / PLL gets its name from the output frequency being an integer multiple of the reference input frequency.

3.2.3.1. Integer-N Phase Locked Loop

The Integer-N Phase Locked Loop is composed of four basic functional blocks: a phase frequency detector (PFD), a loop filter, a voltage-controlled oscillator (VCO), and a programmable divider (N). A general block diagram of an Integer-N / PLL is shown here in Fig. 3.2.3.1-1.

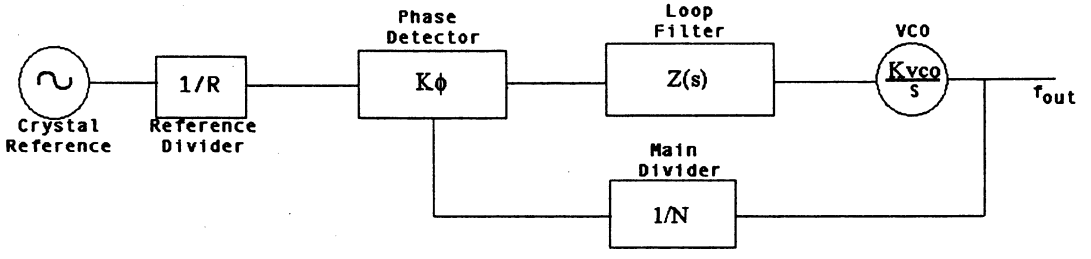

Fig. 3.2.3.1-1. Integer-N / PLL block diagram.

One of the most intriguing capabilities of the PLL is its ability to suppress noise superimposed on its input signal [1]. The PLL is a closed-loop feedback system that uses a Phase / Frequency Detector (PFD) to compare and adjust the system.

The Integer-N / PLL architecture is desired over other types of architecture for its advantages. The Integer-N / PLL provides functionality, low power consumption, savings in space, and it's economic [1]. Therefore, it has become the basis of wireless communication since it operates at low voltages and low currents. The switching speeds can be enhanced to the sub-millisecond range. This architecture does have its disadvantages however. One major

disadvantage is that the phase noise performance degrades significantly, because of its high division ratio.

3.2.3.2. Crystal Oscillator

In order for the PLL to track, we are required to have a good reference signal to be able to get a good lock on our system. We have found that crystal oscillators, typically flat disc-shaped quartz crystal resonators, provide a very clean sinusoidal wave. We have found that the Q of such an oscillator is typically greater than 2000, which means that the frequency stability is excellent and the phase noise at 1 kHz offset is superb [14]. The crystal oscillator provides excitations and resonance modes which are predictable, repeatable and most importantly, exploitable. For our design, we are required to have a crystal oscillator at 19.68 MHz. We cannot get any higher oscillation since this serves as the system clock for all digital components. The clock is also used in the microprocessor, which cannot read anything higher than 20 MHz. The drawback and reason why we do not use a crystal oscillator in place of our PLL is that the crystal tuned oscillator exhibits a natural resonant frequency well below 100 MHz, which is undesired for our design.

3.2.3.3. Phase Frequency Detector

The Phase Frequency Detector (PFD) is mostly used in PLL applications for several reasons. PFDs offer unlimited pull-in range, which guarantees PLL acquisition under even the worst operating conditions [3]. Secondly, because the output signal of the PFD depends on phase errors in the locked state of the PLL and on frequency errors in the unlocked state, a PLL which uses PFD will lock under any condition, irrespective of the type of loop filter used.

In order to understand how a PFD works, we must take a look at it in a more detailed manner. A PFD is composed of two D flip-flops, which take in four inputs. One input of each D flip-flop is set to the logical high, and the other input from each D flip-flop comes from the outputs of our PFD. One output of each D flip-flop is connected to a logical AND gate, which in turn is connected to the reset pin of both D flip-flops. Then the output of one of the D flip-flops is connected to an NPN / MOS transistor, and the second D flip-flop output is connected to a PNP MOS transistor. When the D flip-flop whose signal is connected to the N-channel MOS transistor is set high, the transistor conducts, so the final output is at ground potential. When the D flip-flop whose output is connected to the P-channel MOS transistor is high, the transistor conducts and the final output is some positive supply voltage.

The PFD that we are using in our design has two inputs and two outputs. The two inputs are the reference frequency that comes from the crystal oscillator, and the output frequency from the Voltage Controlled Oscillator (VCO), which is the frequency being fed back in our negative feedback control loop (PLL). The outputs of the PFD are used to drive two switched current sources, each of which is known as a "charge pump" [14]. The charge pump places a charge on a capacitor by sinking or sourcing current according to the difference in phase measured by the PFD. The charge on this capacitor is used as the controlling voltage to the VCO. Additional capacitive and resistive networks may be added to ensure stability and suppress ripples.

3.2.3.4. Loop Filter

The loop filter is a passive second-order filter that outputs a DC voltage to the VCO. The PLL must rely on the loop filter to maintain a low phase noise and low spurious output [6]. The design of the filter also determines the transient response or switching time. One can increase the order of the filter to obtain better phase noise attenuation.

Since this is a passive filter it only requires a number of capacitors and resistors. For a second-order filter there are two capacitors and one resistor.

The values for the components in the loop filter can be calculated using different methods. Following National Semiconductor's application note 1001 [8], there are parameters that need to be determined before the actual filter components are calculated. One must know the Voltage Controlled Oscillator (VCO) Tuning Voltage constant, which is the frequency versus tuning ratio [26]. We also need to know the Phase Frequency Detector / charge pump current (K_ϕ), which is the ratio of the current output to the input phase differential [8]. The radio frequency output of the VCO at which the loop filter is optimized (RF_{out}) and the frequency of the phase detector inputs, which are usually equivalent to the RF channel spacing, are also needed to determine the loop filter components. Lastly, the final parameter that must be known is the main divider ratio, which is equal to RF_{out} / F_{ref} [8]. Once these parameters are known, we can use the following *Matlab* code to calculate the loop filter components:

$$N = F_{out}/F_{ref};$$

$$T_1 = (\sec(\phi_p\pi/180) - \tan(\phi_p\pi/180))/1.256e5;$$
$$T_3 = \not\in((10^{(ATTEN/20)}-1)/(2\pi F_{ref})^2);$$
$$T_2 = 1/(w_c^2(T_1+T_3));$$

$$C_1 = (T_1/T_2)(K_\phi K_{vco})/(w_c^2 N))(\not\in(1+w_c^2T_2^2)/((1+w_c^2T_1^2)(1+w_c^2T_3^2))$$
$$C_2 = C_1(T_2/T_1 - 1)$$
$$C_3 = C_1/10$$

$$R_2 = T_2/C_2$$
$$R_3 = 0.1C_2R_2/C_3$$

Fig. 3.2.3.4-1. *Matlab* code to calculate loop filter components.

3.2.3.5. Voltage Controlled Oscillator

If the output frequency of an oscillator circuit can be varied by an input voltage, then the circuit is called a voltage controlled oscillator. A variable oscillator frequency is necessary in radio frequency applications so that exact channel selection can be achieved. It exhibits a tuning gain, K_{VCO}, which is also referred to as the sensitivity of the VCO and has units of frequency per voltage. The performance of the VCO is measured by looking at how much noise, or unwanted distortion, is generated and introduced into the system by the VCO [26]. By itself the VCO has a tendency to drift from the desired frequency and therefore must be controlled using modern

control system techniques. The goal of the VCO is to produce a noise-free signal that can be used as a local oscillator that will aid in the down- or up-conversion of a received signal.

The basic hardware of an oscillator requires an LC circuit that feeds to the collector of an NPN transistor. Usually there is a feedback wire from the LC circuit to the emitter of the same transistor. To obtain a variable frequency output, a tank circuit is incorporated into the circuit. This tank circuit has a role similar to the flywheel in a car, in that it is required to start the oscillation. This circuit consists of an inductor and capacitor in parallel, which gets an input from a varactor or reversed-biased diode. The duty of the tank is to store and release a pure sinusoidal signal.

Three different VCOs are required in our transceiver. The output frequency of the VCO, which produces the RFLO, needs to have a range of 60 MHz. The input voltage necessary to achieve this range is 0.5 to 2.5 volts, resulting in a gain of roughly 30 MHz/V [27].

3.3. Alternative Approach / Design Trade Off

Most engineering designs have a number of approaches available, and every engineering design consists of a number of design decisions and tradeoffs. In general, RF designs contain tradeoffs between noise, power, linearity, frequency, voltage, and gain [14]. Now, we discuss specific alternatives and tradeoffs we encountered in our designs.

3.3.1. Receiver

There are many different implementations of filters as well as many different types of filters in the market. For this project, three different filter implementations were explored. While we chose to use a Butterworth filter, we also looked into the possibility of using a Chebyshev or a Bessel filter. The three different types of filters that were considered for this project were active, passive, and digital filters. As we have already discussed, we selected an active filter, and in the following we discuss our reasons for not choosing a passive or a digital filter type.

Here we discuss two other filter implementations and the various advantages and disadvantages of each one. Chebyshev is one of the filter implementations that could have been used for our low-pass filter design. While it has the advantage of better attenuation in the stop-band, there is more ringing in the pass-band than that of the Butterworth implementation [17]. Ringing is undesired because it corrupts the signal, which is undesirable since our signal is already of a small magnitude. For this reason, we chose not to design a Chebyshev low-pass filter. The other filter implementation we looked at is the Bessel low-pass filter. While the Bessel filter implementation has excellent pass-band response, the attenuation in the stop-band is not so good as the Butterworth implementation [17]. This poor attenuation in the stop-band would result in the need for a higher-order filter, adding to the complexity of the circuit. In trying to design an appropriate filter, space is also a limiting factor and outweighs any advantages that the Bessel filter would offer in the pass-band.

The other factor we explored was the type of filter that could have been used. The advantage to using a passive filter is that there is no power supply required, which would benefit

our need for low power consumption. In addition to no power supply, passive filters can accommodate large bandwidths and create little noise [10]. One disadvantage to passive filters is that they require more space than an active filter of similar order. Another problem with passive filters is that they are difficult and time-consuming to design [10]. Though we spent a considerable amount of time designing an active filter, the process was straightforward. The other type of filter that we explored was the digital filter. The advantages to digital filters are that they are not temperature or time sensitive. Also, digital filters are easily implemented on a general-purpose computer or workstation and are easily altered to fit a new design specification, which saves time in the design process [19]. One disadvantage of a digital filter is the comparatively high cost for simple tasks. Since our design task is very simple for a digital filter, we have no need for such an advanced filter. A digital filter needs a high processing speed when the bandwidth is large [21]. In our case where the bandwidth is 3 MHz, a digital filter would be a poor choice. The last disadvantage with a digital filter is that the hardware is detailed and the software required is complex [21]. For this reason, the design of a digital filter would require too much time, and it would not be realizable.

3.3.2. Transmitter

As mentioned in Section 3.2.2 and above in 3.3.1, in filter design there are a number of alternative methods and architectures available. However, our band-pass IF filter has vastly different design constraints than does the low-pass filter in the receive path. Here also, like in the receive path we do not use a digital filter, but an active configuration is not a viable option either. Active filters are feasible only up to a few MHz, whereas LC filters are practical into the hundreds of MHz.

There are two main types of passive band-pass filters: wideband and narrowband. A wideband band-pass filter is implemented by cascading individual low-pass and high-pass filters. Narrowband band-pass filters cannot be implemented as such, because of the increase in loss at the center frequency as the ratio of upper to lower cutoff frequencies increases. Because we require a ratio of much less than 2, we design a narrowband filter.

With these considerations in mind, there are still a wide variety of configurations and techniques to choose from. For example, the low-pass to band-pass transformation [16] is often used to design such a filter from standard low-pass design tables. Such a filter may or may not be an all-pole filter. Architectures include parallel tuned circuits, series tuned circuits, and synchronously tuned filters. For example, we considered using an elliptic filter, but it suffers high inductance spread so as to be impractical above 100 MHz [13]. Although certain transformations can be performed to reduce this effect, the resulting circuit requires roughly twice as many capacitors, meaning increased cost and difficulty in construction.

We choose a narrowband coupled resonator configuration for its desirable characteristics for high-Q filters and for its simplified tuning (since all nodes resonate to the same frequency). Of the possible narrowband coupled resonator configurations, we choose the capacitive-coupled configuration over the inductive-coupled configuration. The circuit with fewer inductors generally takes up less space and is more economical.

3.3.3. Frequency Synthesizer

Part of our design was to understand why we picked the components that make our PLL. Understanding the advantages and disadvantages of such choices is a crucial part of developing our design. When picking components or methods of solutions that are already on the shelves, we found many that we did not choose as explained in this section.

When selecting the type or architecture, we found that the Fractional-N / PLL was a possible solution. What makes the Fractional-N / PLL appealing for our design is that it improves phase noise by increasing the reference frequency, which in turn improves switching speeds as well as loop bandwidth [23], [3]. If we recall, the Integer-N / PLL's major disadvantage is that it has a high division ratio, thus causing significant degradation in phase noise performance. We weighed the options and decided to stay with our Integer-N / PLL architecture, because the major disadvantage of the Fractional-N / PLL architecture is that it adds complexity in circuitry and adds spurious signals [6]. We decided that the disadvantage of the Integer-N / PLL architecture could be downplayed by decreasing the bandwidth of the loop filter. When trying to deal with more circuitry, we have to keep in mind that we want the lowest possible power consumption from our circuit, which means a smaller circuit. The less circuitry, the smaller the cell phones or laptops we can provide for customers. Once our decision was made on the type of architecture, we moved to selecting the proper components of our PLL.

The type of oscillator was one of the first components we looked at. We found many types of oscillators such as sinusoidal oscillators, op-amp / RC oscillators, LC oscillators and crystal oscillators among others. The choice for the reference oscillator was a fairly simple one because the range of frequency that we are working with eliminates most of the other choices, because stable and accurate RC and LC oscillators are almost impossible to design at such high frequencies. Not mentioning that each of these components, like any electronic device, produces noise, while the crystal oscillator does not.

One of the most important components in our PLL is the phase detector (PD). While searching for the correct phase detector, we again found numerous choices. Some of these choices were the EXOR gate and the JK flip-flop phase detector. Each of these had its own advantages and disadvantages that we had to pay close attention to. The advantage of the EXOR gate is that it provided phase tracking that could be maintained when the phase error is confined to the range $-\pi/2 < E < \pi/2$, assuming symmetrical signals [3]. The disadvantage is that the phase detector becomes severely impaired if the signals are not symmetrical, causing a reduction in loop gain, which means a smaller lock range and pull out range. The pull out range is the frequency range that causes the closed-loop system to unlock. If we chose the EXOR gate as our PD, we would be adding an additional constraint to our system, which is undesirable. The next possible choice for the phase detector is the JK flip-flop. The advantage of the JK flip-flop over the EXOR gate is that the symmetry of the signals is irrelevant since the JK flip-flop depends on the rising edge of the signal. The disadvantage, however, is that if the loop filter doesn't contain an integrating term, the pull-in range stays severely limited [3]. An integrating term in the loop filter adds not only complexity to our circuit, but it leaves no room for future changes. We therefore decided that we do not want to be limited by other unnecessary constraints and therefore chose the PFD instead. We must recall that the PFD's major advantage is that it

provides virtually unlimited pull-in range, which will cause any PLL that contains a PFD to lock regardless of the loop filter that is being used.

To select the type of loop filter was based on the type of PLL components that were chosen. We could have chosen an active low-pass filter versus our passive low-pass filter. The tradeoff is that we added less noise to our system when we chose a passive low-pass filter.

3.4. Lessons Learned

All of us have learned important lessons from our experience gained in working on our design problems. We share a few of those lessons below.

3.4.1. Receiver

The most significant lesson learned is in our approach to selecting the best solution to our problem. We have learned that a top-down method develops a design by initially proposing a solution in terms of block diagrams. Then each block diagram is broken down into a more detailed and manageable piece than otherwise. This is especially true at the beginning of the project when time is crucial. By following this process we were able to eliminate any unnecessary steps pertinent to the required task.

3.4.2. Transmitter

Designing a low-order band-pass filter initially sounded simple to us, but the more we worked on the design problem the more we learned about all of the design choices, tradeoffs, and issues involved. The target frequency range of our filter made the task particularly challenging. Computer simulation tools proved very useful, once we discovered how to simulate in *PSpice* circuits containing nodes with no direct DC path to ground. Even so, some designs that looked very good on paper or even in the simulator were either not realizable or would not have worked nearly as expected. Many of our preliminary trials required unrealistic component values, were extremely sensitive to component variation (for instance, there is no 0.1487 ± 0.00005 pF capacitor in the market), or did not account for finite inductor Q. Additionally, stray capacitance and even the inductance of small jumper wires used in a physical implementation had to be taken into account.

3.4.3. Frequency Synthesizer

In designing a system, we must be very precise in the selectivity of the components that make up our design. This will eliminate error in future steps. The selection of the proper components allows us to reach our goals in a smoother and more direct way. The process of selecting our components helps to avoid phase noise, reduce power consumption and eliminate the need for large circuits. We have learned that part of a design is not only understanding the concepts, but also dealing with non-ideal properties, which adds additional constrains in our design that we did not necessarily take into account when running the simulation.

Chapter Four – Evaluation

4.1. Introduction

Due to the requirements for highly specialized and expensive equipment, we were unable to construct our prototypes or take measurements at our local facilities. Special arrangements had to be made to take measurements in an adequately equipped environment. Maxim Integrated Products invited us to their laboratories in Sunnyvale, CA for two days to construct our prototypes and to conduct tests.

This chapter is concerned with evaluating the results of both simulation and actual measurements. In Section 4.2 we describe the ways in which we constructed and tested our prototypes, presenting our results and discussing their significance. In Section 4.3 we give comparisons between the final design and the original specifications, stating design tradeoffs encountered.

4.2. Discussion of Results / Test Plan

4.2.1. Receiver

The cascaded evaluation is carried for the entire receiver architecture. One of the parameters evaluated is noise figure of the entire system. This is one of the factors that determines system sensitivity. The actual mathematical calculation uses the Friis equation [4],

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} \tag{4.2.1-1}$$

where F and G are the noise factor and numerical gain of each stage in which

$$NF = 10 \log_{10} F \tag{4.2.1-2}$$

is the noise factor expressed in dB. The actual calculated values for the various parameters in Table 4.2.1-1 resulted in the overall noise figure of 5.0 dB. Using the IP_3 for each stage, the cumulative IP_3 of the cascade was also calculated. Also, IP_3, which has frequencies located close to the desired signal, was calculated to help determine the amount of channel interferers that would have to be attenuated.

Table 4.2.1-1. Cascade analysis for W-CDMA receiver.

Cascade Analysis for W-CDMA Receiver

Stage Name		Duplexer		LNA		RF Bandpass filter		Mixer		IF Band pass filter		IF Amplifier/ Demodulator
Stage#		1		2		3		4		5		6
A_V (dB)		-2		15		-2.5		12.0		-10		35
A_P (dB)		-2		15		-2.5		12.0		-10		35
Cumulative A_V (dB)			-2.00		13.00		10.50		22.50		12.50	
Stage NF (dB)		3.00		1.70		2.50		7.00		10.00		6.36
Cumulative NF(dB)	5.0		2.37		9.45		6.95		-8.64		-28.64	
Stage IP3 (dBm)		100		4.2		100		6.8		1000	<- Vrms ->	0.7
Cumulative IP3	-4.12 dBm		-6.12 dBm		9.30 dBm		6.80 dBm		73.01 dBm		700.00 mVrms	

There are many possible solutions to our design. As explained in Chapter Three, the approach we have taken in all of our analysis of the low-pass Butterworth filter is to make use of the Sallen-Key normalized low-pass prototypes. The Fig. 3.2.1-1 shows a complete schematic diagram, and the actual element values are given in Table 4.2.1-2. Our filter has an overall 3 dB gain with a cutoff frequency at 3 MHz.

Table 4.2.1-2. List of components and values used in the filter design.

Component	*PSpice* Simulation	Original Circuit	Final Circuit
C_1	53 pF	68 pF	68 pF
C_2	0.186 nF	22 pF	22 pF
C_3	0.138 nF	8.2 pF	22 pF
C_4	20 pF	56 pF	68 pF
R_1	461 Ω	1 kΩ	1 kΩ
R_2	131 Ω	332 Ω	332 Ω
R_3	923 Ω	2 kΩ	2 kΩ
R_4	1 kΩ	2.7 kΩ	1 kΩ
R_5	1 kΩ	2.7 kΩ	1 kΩ
U_1	Ideal op-amp	THS4121	THS4121
U_2	Ideal op-amp	THS4121	THS4121

The filter meets all specifications listed in Table 2.3.1-1. All capacitors in the circuit, which are the main contributor of weight, were found to have values in the range of picofarads. This addresses some of our application considerations that deal with the issue of lower weight as well as smaller size. In summary the active design performed very well and gave us an overall cascaded performance that closely approximates the results obtained by calculation.

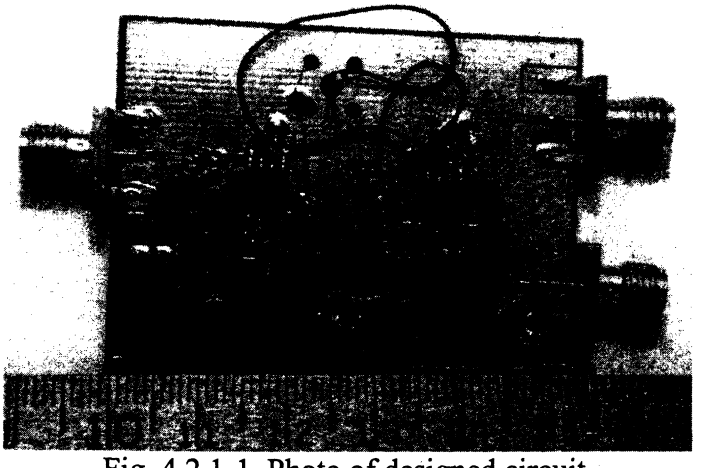

Fig. 4.2.1-1. Photo of designed circuit.

A test condition dictating the blocking performance required of the receiver was applied at 15 MHz. The Fig. 4.2.1-2 shows the actual performance under this test condition. When the receiver tries to process a weak signal in the presence of interferer, the weak desired signal tends to experience a vanishingly small gain. When the gain drops to zero, the signal is blocked [14].

So the receiver must be able to withstand a blocking signal of a certain level in dB. As shown in Fig. 4.2.1-2, the receiver meets our requirement. We are able to receive the wanted signal in the presence of an unwanted interferer at the specified frequency.

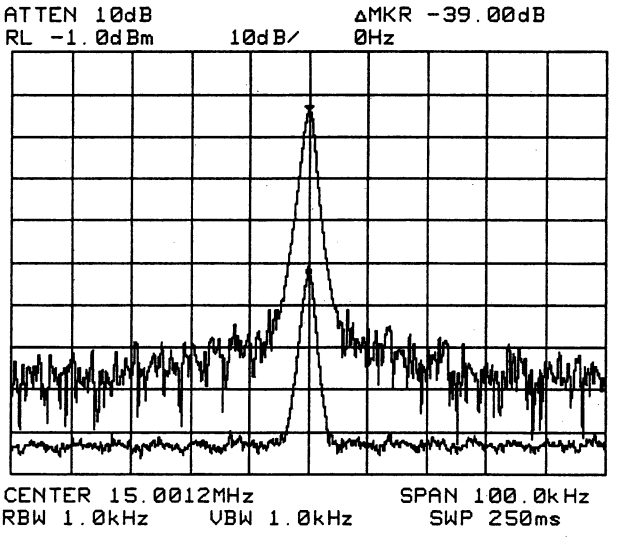

Fig. 4.2.1-2. Performance result obtained from network analyzer.

4.2.2. Transmitter

Shortly before heading up to the laboratories in Sunnyvale, we drove south to visit our advisor Mr. Bob Kelly in preparation. This consultation proved to be very beneficial and a definite test plan was formulated. However, upon arriving in Sunnyvale, we were given a MAX2360 evaluation kit to work with directly, and our test plan required substantial revision.

4.2.2.1. Initial Plan

The initial test plan was as follows: first, we construct a prototype of our filter on unetched FR4 circuit board. Physical construction consists of cutting grooves in the surface of the copper-plated board for electrically-open connections, which are verified with an ohmmeter. The surface-mount parts are then laid out and soldered in place. Measure the response of the filter by itself, then connect the filter to the MAX2360 evaluation kit and examine the effect of the prototype filter on the performance of the transmitter.

4.2.2.2. Intermediate Trials

Given the MAX2360 EV board, we attempted to implement the filter directly on the board by finding suitable traces and pads that can be reused for our purposes. This is a major constraint, but also one commonly encountered in practice, where a prefabricated board requires modification to function properly. Upon determining a physical layout given the constraints, we constructed our differential filter as given in Fig. 3.2.2-3.

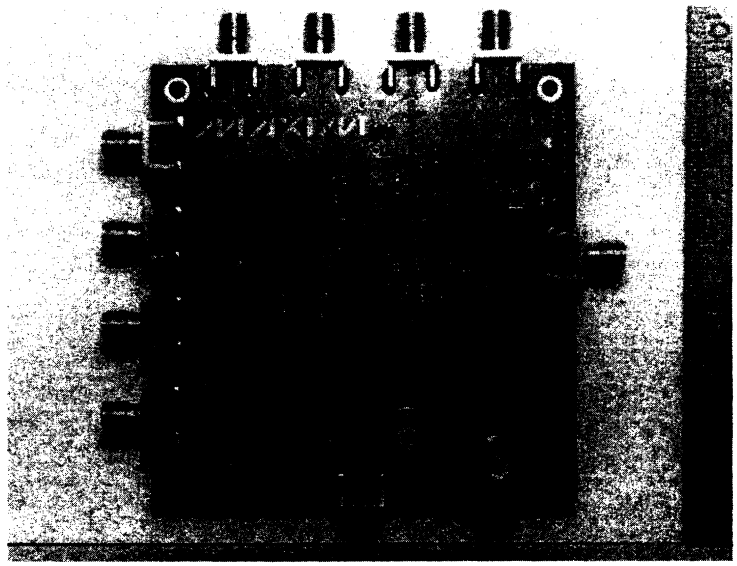

Fig. 4.2.2.2-1. MAX2360 EV board.

Our modified board was connected per the standard EV test setup, and we attempted to lock the on-chip PLL to twice the IF, or 760 MHz. However, we could not lock to the desired frequency. In fact, the evaluation board used specifies an IF of up to only 300 MHz. For the PLL to lock at 780 MHz, the tank circuit requires modification.

After performing the necessary modification, the PLL locked at 760 MHz, but the range over which it locked was too narrow to be of use in determining the response of our filter at critical frequencies. Therefore, yet another modification was performed to bypass the on-board PLL circuitry, such that the signal can be injected directly from a high-quality signal generator. Thus the signal range was no longer limited by the on-board circuitry, but by the range of the Agilent E4433B signal generator.

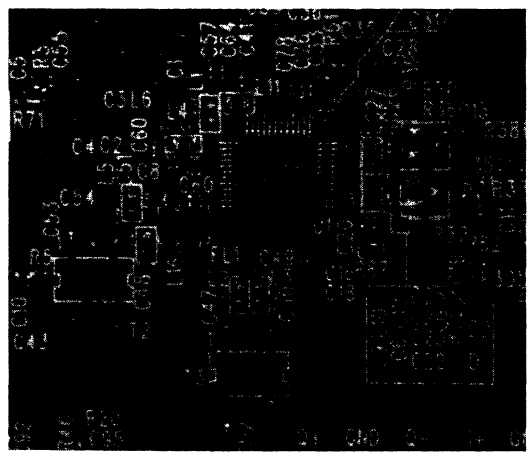

Fig. 4.2.2.2-2. Circuitry with all modifications.

Once all modifications were complete, in order to determine the response of our differential filter, we attempted to measure the magnitude of the input and output signals with an RF probe. In theory, the magnitude response was given by the difference in these two values. In

practice, this proved to be very difficult, and we were unable to obtain consistent data. Furthermore, the undesired inductance resulting from the two long blue jumper wires at this frequency could have only made matters worse!

4.2.2.3. Final Plan

From our intermediate trials, evidently our initial plan to build and test the filter off-board first is most appropriate. Rather than constructing a layout from scratch, we use a prefabricated PCB with suitable pads and traces (courtesy of Mr. Daniel Kong), as illustrated in Fig. 4.2.2.3-2.

The filter circuit is reconstructed on the PCB using the design values, conversion is made to 50 Ω single-ended input and output, and SNA connectors are attached. The response is measured on a HP 8753E RF network analyzer. Due to the finite Q of real inductors and stray capacitance in the prototype, component values are tweaked as necessary until a suitable response is obtained. The final circuit is given in Fig. 4.2.2.3-1, where the unlabeled components are representative of these effects.

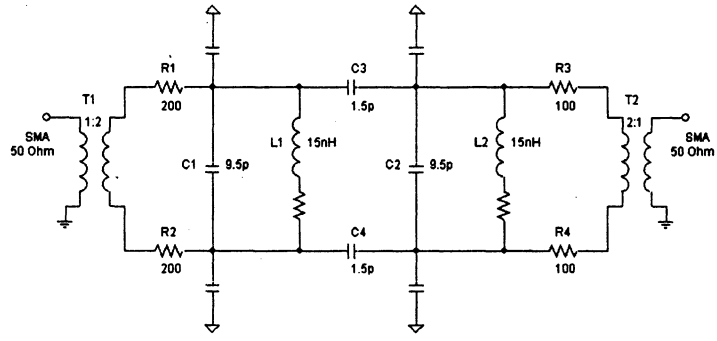

Fig. 4.2.2.3-1. Final prototype circuit.

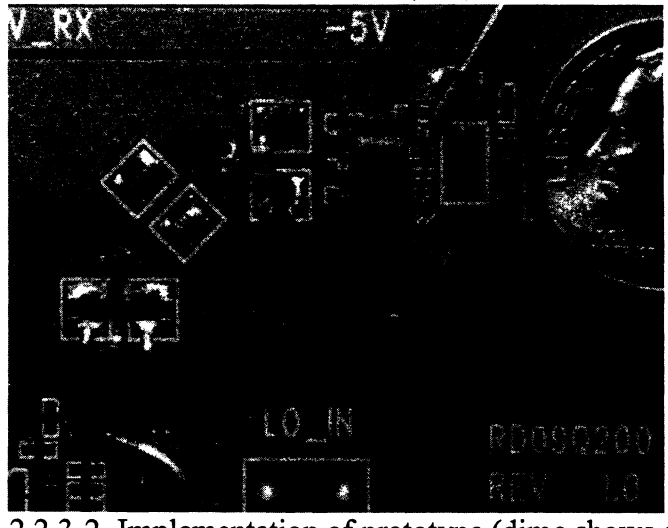

Fig. 4.2.2.3-2. Implementation of prototype (dime shows scale).

4.2.3. Frequency Synthesizer

The setup for the lab limited the way we tested our prototype. In order to measure the required fields for our design, we are required to have the entire transceiver already built for us.

Understanding the test bench is as important as understanding the actual design. We shall explain the test bench so that we can reference it in future sections. To generate our reference signal, we have two possible choices for signal generators. The first is an E4433B Agilent ESG-D Series Signal Generator with a frequency range of 250 kHz – 4.0 GHz. The second is a Hewlett Packard 8648C Signal Generator with a frequency range of 100 kHz – 3200 MHz. To view the frequency response we used an 8562EC Agilent Spectrum Analyzer with a frequency range of 30 Hz – 13.2 GHz. Our test bench included a PC with control software.

4.2.3.1. Test Plan

The structure of our design requires us to have the entire transceiver built. In order to implement our filter design, we use the MAX2360 EV board. This is an evaluation board that has been laid out specifically for testing the MAX2360 quadrature transmitter chip by potential customers. This board is an acceptable piece to test our IFLO / PLL design. Even though we had designed and simulated the RFLO and both Rx and Tx-IFLOs, the MAX2360 EV board only allows us to test our Tx-IFLO. The layout of the board calls for size 0402 surface mount monolithic chip capacitors and resistors. This means that we need to round our design values according to the 5% standard production values, shown in Table 4.2.3.1-1. With our resistor and capacitor values chosen, we replace the existing loop filter components with our own values.

The next step in testing our design is the proper setup of the PC Control Software. This is just a graphical user interface program that allows us to use the processor of a PC in place of a microprocessor that would be present in a production unit. After the program was set to the proper settings we attach all the proper signals and analyzer fittings.

Table 4.2.3.1-1. 5% Values for resistors and capacitors.

5% Resistor Values:										
1	1.2	1.5	1.8	2	2.2	2.4	2.7	3	3.3	3.6
3.9	4.3	4.7	5.1	5.4	5.6	6.2	6.8	7.5	8.2	9.1

5% Capacitor Values:											
1	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

4.2.3.2. Discussion of Results

We discuss the Tx-IFLO, which was the only one that was measured and tested. The first step in getting our measurements was to get our PLL to lock to any frequency [1]. Fortunately for us, because we are using a PFD, the PLL will lock regardless of our loop filter [2]. Our design made

sure that we locked at the desired frequency of 760 MHz. The PLL also generated the harmonics that were expected. This is visible on the spectrum analyzer graph shown below. The *span* feature on the spectrum analyzer can be used to view the actual output frequency and phase noise response over a target range. In this case, the span was 100 MHz.

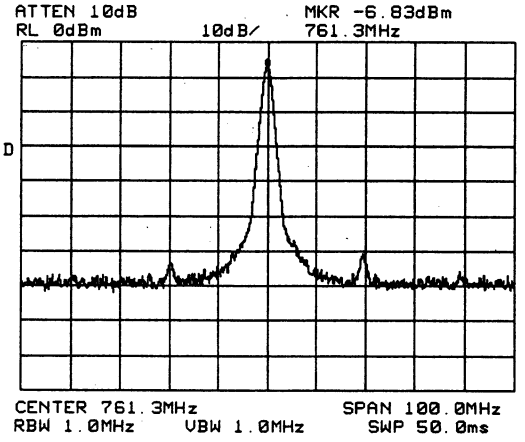

Fig. 4.2.3.2-1. Locked PLL with center frequency of 761.3 MHz and with spurs at multiples of the reference frequency, 19.68 MHz.

Once we got the PLL to lock at the correct frequency, we had to check if our design met its goal. The goal of the design was to design a loop filter, which would get rid of in-phase noise. For this particular IFLO, we needed to provide an output signal of 760 MHz, which we tracked at 761.3 MHz. The Fig. 4.2.3.2-2 illustrates our measurement in phase noise attenuation of approximately –60 dBc/Hz. It was also noted that we used two types of signal generators to simulate our crystal oscillator. We found that the E4433B Agilent ESG-D Series Signal Generator provided a good clean signal similar to a crystal oscillator with very little phase noise added. However, the Hewlett Packard 8648C Signal Generator was measured to provide an additional 4 dB of phase noise to our system. Therefore we decided to work with the Agilent Signal Generator.

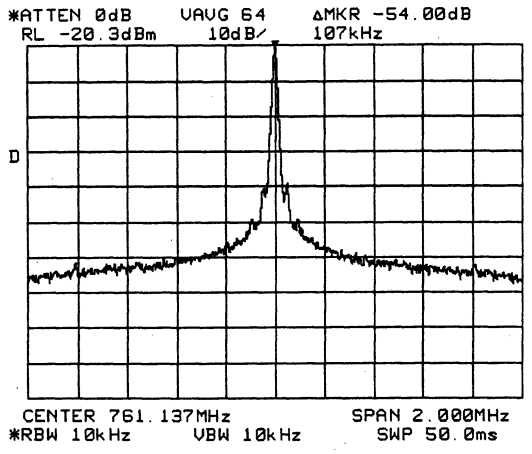

Fig. 4.2.3.2-2. Gives a closer look at the center frequency and the relative close in phase noise. From this figure one can see that we achieved roughly –60 dBc/Hz attenuation.

Next, Fig. 4.2.3.2-3 is a plot of the phase noise measurements at different spot frequencies ranging from 1 kHz to 1 MHz. Note that the amount of attenuation increases linearly with the logarithmic increase in frequency.

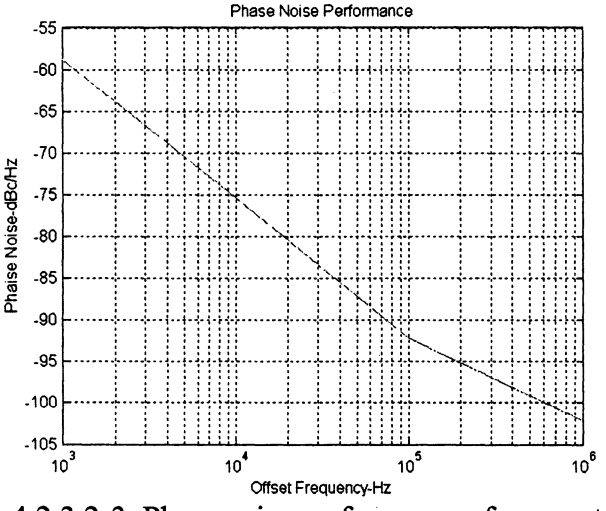

Fig. 4.2.3.2-3. Phase noise performance of our system.

Also, Fig. 4.2.3.2-4 is a graphical representation of the response of our system. This figure indicates that the system has approximately 2 kHz bandwidth. This plot is very similar to the Bode plot that resulted from the simulation, Fig. 4.2.3.2-5.

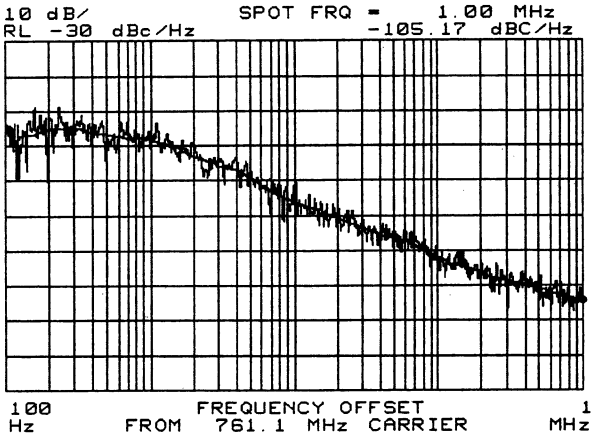

Fig. 4.2.3.2-4. Shows the measured loop bandwidth on the spectrum analyzer.

We simulated our loop performance to verify our design and to compare with the experimental data received. From Fig. 4.2.3.2-5, it can be read that the roll-off frequency in radians is 5.94×10^4. This corresponds to roughly 9 kHz bandwidth. The reason for the differences in bandwidth between simulation and experimental results are explained in Section 4.2.3.3.

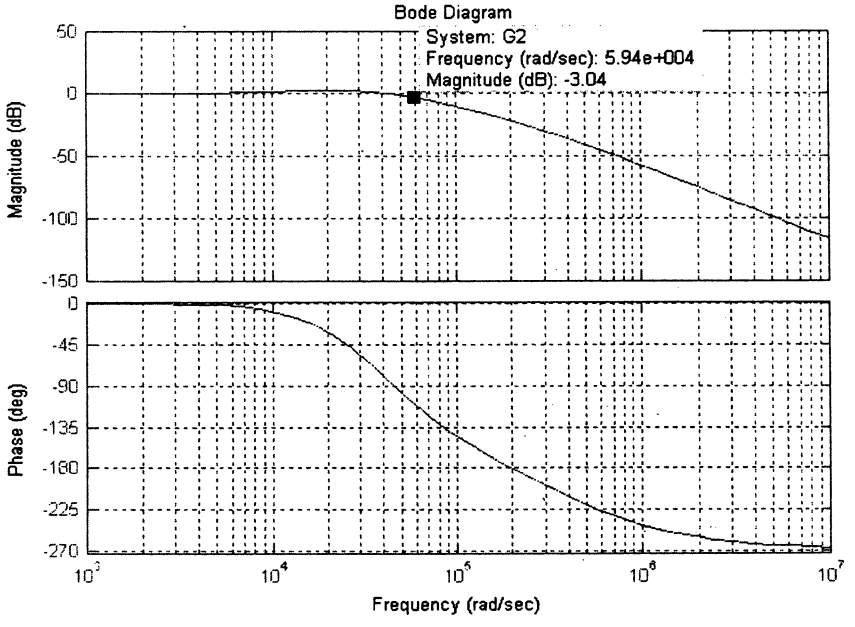

Fig. 4.2.3.2-5. Simulation of loop bandwidth performance.

4.3. Design Comparison / Design Trade Off

4.3.1. Receiver

We have already specified the required performance of our receiver and the filter. The amplitude response over frequency is one of the most important aspects of our design. It is crucial to the

overall system performance in that it determines the selectivity of our filter. It is a necessary factor in reproducing the original transmitted signal by avoiding signal distortion. This sets the allowable tolerance or dynamic range of our system. The frequency response is very close to those of the preliminary design in *PSpice*. There are notable similarities between Fig. 4.3.1-1 and Fig. 4.3.1-2. As expected the pass-band is maximally flat, giving a cutoff and corner frequency at 3 MHz.

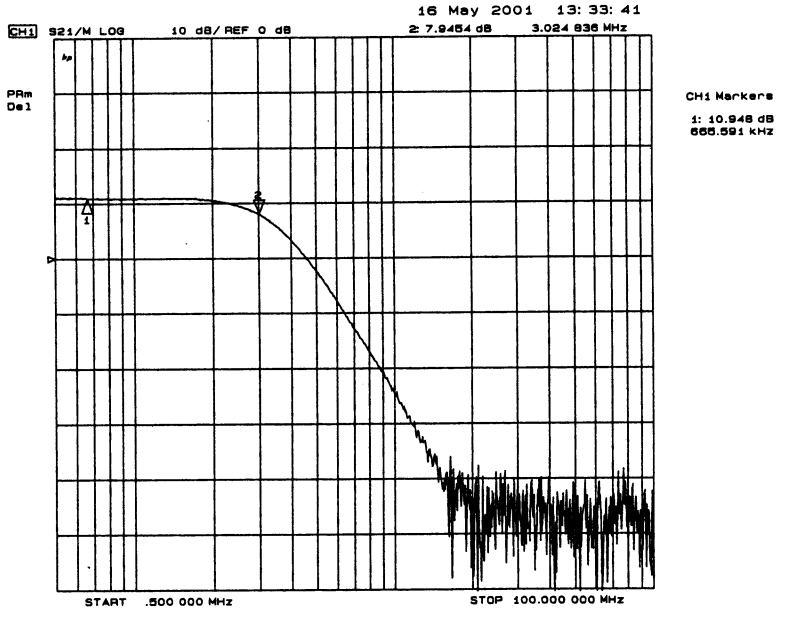

Fig. 4.3.1-1. Actual frequency response of the low-pass filter.

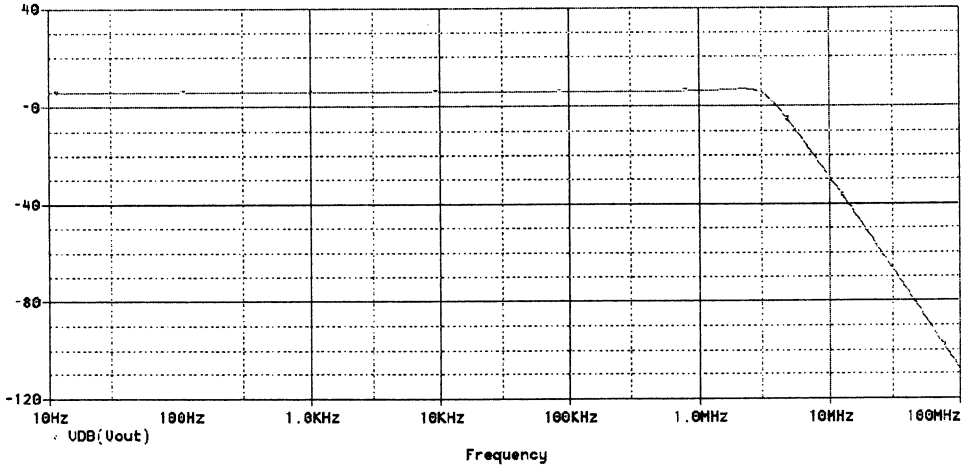

Fig. 4.3.1-2. Frequency response of the low-pass filter (*PSpice* simulation).

Poles and positions were also looked at and were designed using the Sallen-Key method to give the maximally flat response. We can see from Fig. 4.3.1-3 that about half-way to the 3 dB point, group delay departs from flatness and rises to a peak near the 3 dB point. The larger

the number of poles, the more rapid the amplitude drop-off beyond the 3 dB point and the more the group delay deviates from flatness. The data presented in Fig. 4.3.1-3 and Fig. 4.3.1-4 represent the group delay response and phase response of our Butterworth low-pass filter.

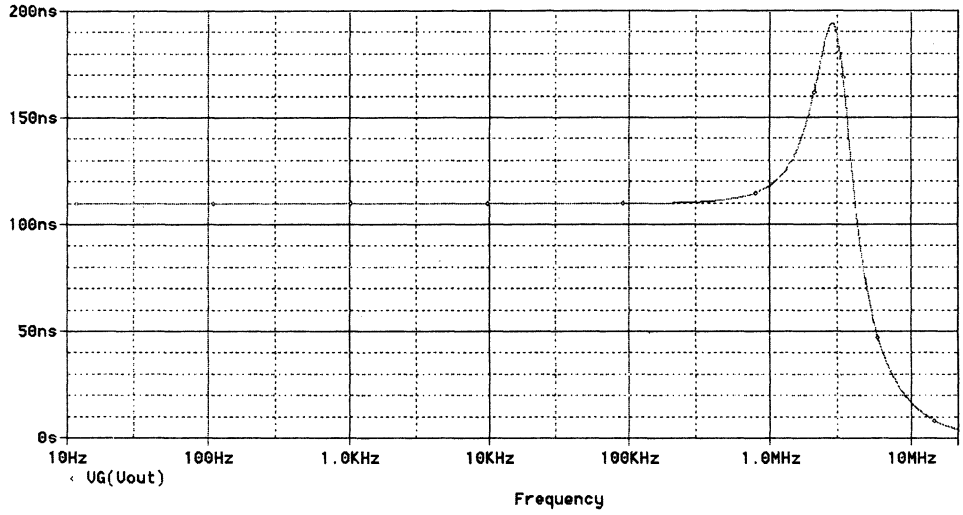

Fig. 4.3.1-3. Group delay of the Butterworth low-pass filter.

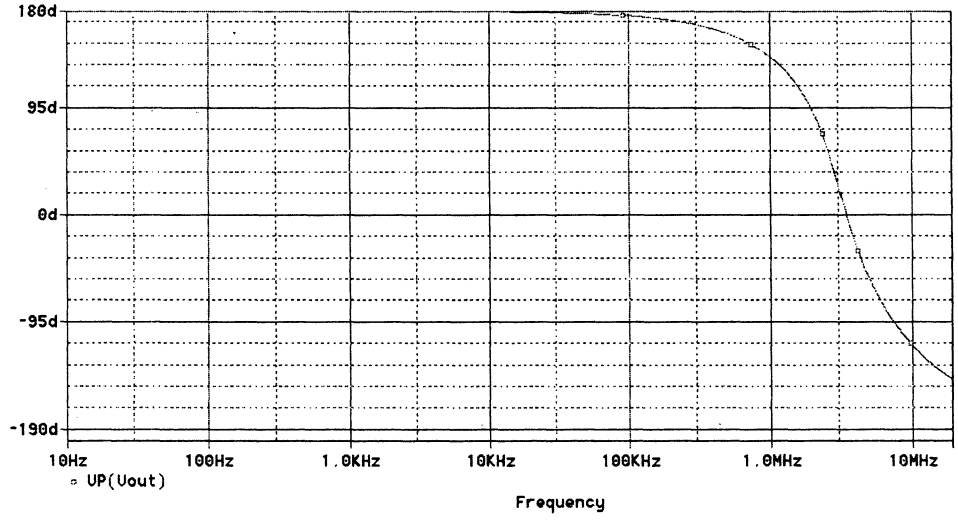

Fig. 4.3.1-4. Phase response the Butterworth low-pass filter.

The actual group delay and phase response of our filter generated by the network analyzer is similar to the one simulated in *PSpice*. The circuit was "tweaked" to show smaller deviation by replacing some of the components in order to obtain desired results. A complete list of components and values showing design changes to improve performance is given in Table 4.2.1-2.

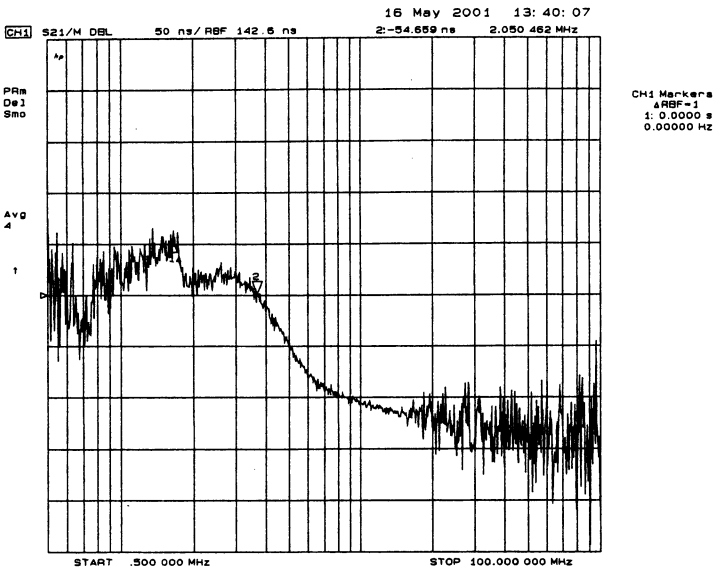

Fig. 4.3.1-5. Group delay of the Butterworth low-pass filter.

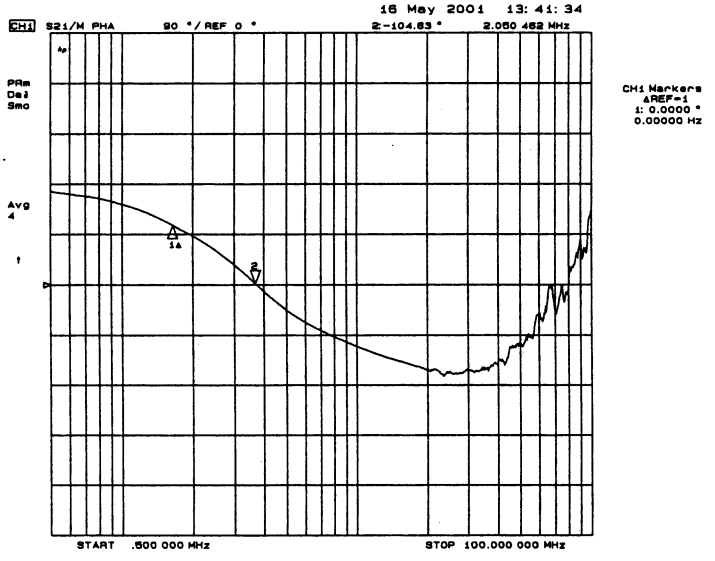

Fig. 4.3.1-6. Phase response of the Butterworth low-pass filter.

The various characteristics we have presented (amplitude and phase) are important since relative delays between components can introduce intersymbol interference. So it is desirable to have a rise time that allows the signaling element to attain its ultimate amplitude before the next element is received. Adjusting the locations of the poles and zeros of the transfer function is one way of controlling the rise time so that maximum amplitude is obtained. For this reason and reasons explained earlier, it is necessary to replace and change the components from the actual theoretically calculated values. For example, although the group delay in the *PSpice* model clearly shows the normal spike, the delay is not so easily seen as in the actual response generated by the network analyzer.

4.3.2. Transmitter

Due to the effects mentioned above, and the combined effects of component tolerances, we cannot expect our initial response to identically match the theoretical response. Indeed, as shown in Fig. 4.3.2-1 below, the initial magnitude response was centered 10 MHz lower than desired.

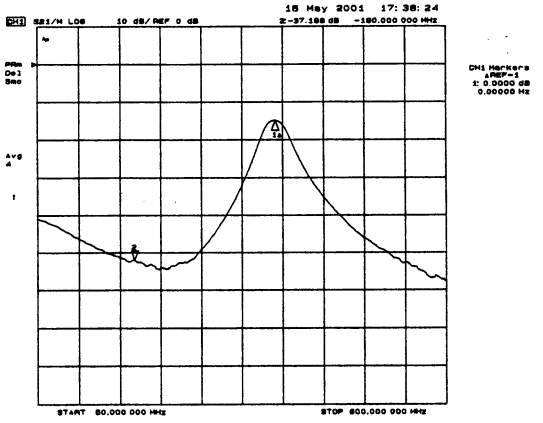

Fig. 4.3.2-1. Initial magnitude response of prototype.

To compensate, the capacitances C1 and C2 were decreased in order to raise the center frequency. After several tries using values between 8 and 12 pF, a response centered around the desired frequency of 380 MHz was obtained, as shown in Fig. 4.3.2-2.

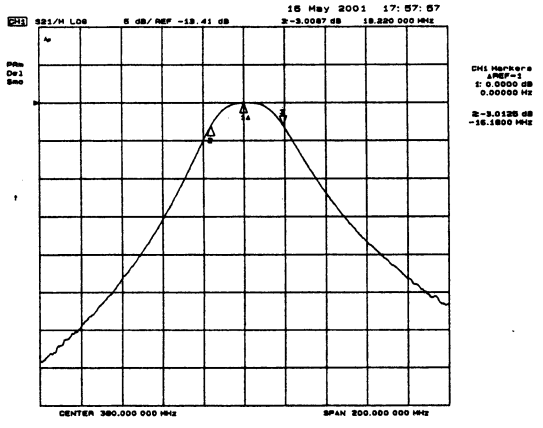

Fig. 4.3.2-2. Filter response after tuning.

From this plot the prototype filter has a 3 dB bandwidth of 35.4 MHz (363.8 to 399.2 MHz), and the insertion loss appears to be 13.41 dB. However, we must subtract the loss introduced by the baluns and resistors used to match the circuit to the 50-Ω single-ended network analyzer, yielding an insertion loss comparable to if not better than that of the standard SAW / IF filter.

We are also interested in knowing the attenuation of signals at our critical frequencies of 190 MHz and 760 MHz. As is clear from Fig. 4.3.2-3 and Fig. 4.3.2-4, these attenuations are

39.7 and 44.2 dB, respectively. Both values exceed the typical attenuation of the standard SAW filter of 37 and 40 dB (respectively) at these frequencies.

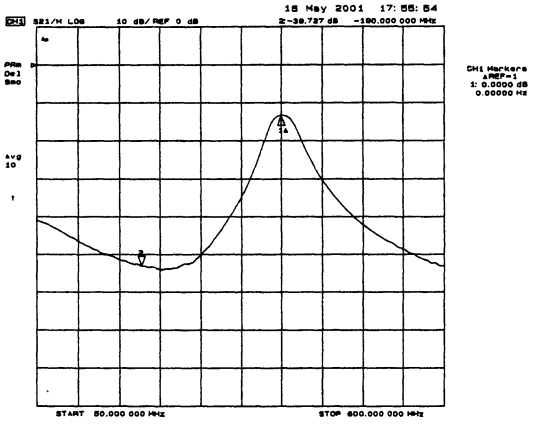

Fig. 4.3.2-3. Measured filter response, 50 – 600 MHz.

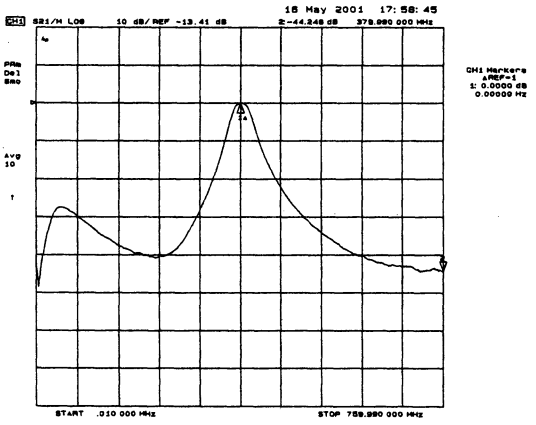

Fig. 4.3.2-4. Measured filter response to 760 MHz.

Finally, we compare the final measured response with the response obtained by simulation, using real-valued components. The response shown in Fig. 4.3.2-5 has a 3 dB bandwidth of 41 MHz (355 to 396 MHz), with an insertion loss of nearly 12 dB. It may seem surprising at first that the measured response is slightly *better* than the simulated response; however, this is easily explained. The values included in the simulation circuit to compensate for parasitic capacitance and finite inductor Q must have been slightly pessimistic. In addition, the measured response does not decrease steadily as in the simulation but shows a large, gentle ripple at lower frequency. Fortunately this anomaly occurs in a non-critical location (at which no significant spurious mixing products are expected) and for our purposes it can safely be ignored.

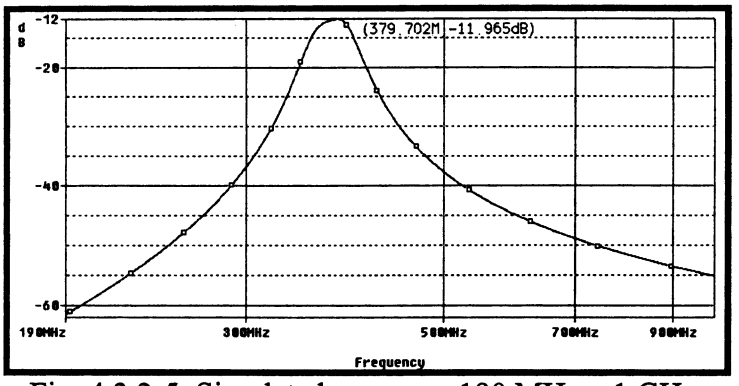

Fig. 4.3.2-5. Simulated response, 190 MHz – 1 GHz.

4.3.3. Frequency Synthesizer

The results of both simulation and the experiment have been stated and there are differences. The scope of this section is to explain the origin of these discrepancies. Perhaps the most noticeable difference is the system bandwidth, which is a function of the input and output parameters. Dissimilarities in the input parameters, namely VCO gain and current gain, most definitely cause the output parameters, or resistor and capacitor values and bandwidth, to differ from what was to be expected. For clarity all values, input and output, are presented in tabular form.

Table 4.3.3-1. Simulation and experimental data.

Parameter	Simulation Value	Experimental Value
K_{vco}	15 MHz/V	30 MHz/V
I_{cp}	2.1 mA	175 μA
F_{ref}	75 kHz	75 kHz
F_{out}	760 MHz	761.13 MHz
N-divider	10133.33	10133
C_1	227.69 pF	220 pF
C_2	81660 pF	68000 pF
C_3	22.769 pF	Open
R_2	11.332 kΩ	11 kΩ
R_3	406.43 kΩ	Short
Settling Time	230 μs	5 ms
Bandwidth	9.45 kHz	1.5 kHz

Actual VCO gain and I_{cp} gain were measured in the lab to see if they differed from what was expected. There was a sizable difference between what was measured and what the design had anticipated. Table 4.3.3-1 indicates that the current gain in the experiment is much less than what was expected. The effect of this decrease in current is a much smaller bandwidth, which can cause degradation in phase noise performance and slow the settling time of the system. The increase in VCO sensitivity in the experiment can also slow the settling time of the system and allow thermal noise from the loop filter to find its way onto the VCO output [15]. With the

knowledge of these key parameters being different from what were designed for, the entire set of calculations used to find RC values is compromised.

Another justification for our experimental results stems from the fact that implementing our exact capacitor and resistor values is not possible. For production reasons, capacitors and resistors are quantized according to 5% values that are standard in industry. We also had to quantize our values according to the industry standard, Table 4.2.3.1-1. It should be noted that the experimental comparison frequency is slightly different from the simulated value and this is because the computer program that controls the N-divider, in the experiment, can only take in whole numbers. However the result of this difference is negligible compared to the effects of K_{vco} and I_{cp}.

Lastly, the EV board that was used was not set up for a third-order system. That is, the pad for C_3 was left open and the pad for R_3 was shorted. In order for us to implement our third-order system we would have had to cut traces and risk permanently damaging the board. This resulted in our experimental results being based on a second-order system, where our design was for a third-order system.

Based on the approval of Mr. Devries, our Maxim advisor, our design was on the right track and the values for the first trial were better than expected. Had we had an additional workbench (all teams shared the same bench) we could have been able to make adjustments to some parameters and components, which were the sources of noise that we had identified.

Chapter Five – Administrative

5.1. Introduction

The administrative portions of the design project can be divided into two categories, budgeting and scheduling, respectively. These administrative portions are essential in planning the execution of each task throughout the project lifetime properly. Budgeting is obviously a primary concern as it enables us to plan the financial aspects of the project to ensure that the financial means are available for completion of the project. Scheduling is absolutely necessary to coordinate meetings and communicate progress amongst pertinent personnel.

5.2. Cost Analysis

The procedure to calculate cost and to write a business plan in this project is exactly the same as that outlined in class. However, this design is a part of a previously produced item at Maxim. Thus, most relevant expenses such as marketing and advertising are already paid through the earlier version of this item. The production cost will not change from the earlier version. Therefore we do not include that here either. The following shows the profit that this design will bring to the enhanced version of this product.

Prototype Cost	
Parts	$530
Software	$2,920
Direct Labor (6 personnel x 12 hours per day x 2 days x $25 per hour)	$3,600
Capital Equipment (purchase price = $94,045; but equipment on-hand) (depreciation schedule: 40% first year, 30% second & third year)	$0
Estimated Costs to Produce 500,000 Units	
Parts (Purchased at Bulk Rate)	$796,360
Labor (Assuming 10 units per hour @ $25 per hour)	$0
Storage ($0.70 per square foot per month for 300 Sq. Ft. for 6 Months)	$0
Advertising Costs	$0
Cost (sub-total)	$803,410
Overhead Cost (5% of Total)	$40,170
TOTAL COST	$843,580
Expected Sales	490,000 Units
Estimated Price Per Unit (All filters combined)	$1.72
Current Price Per Unit (All filters combined)	$2.00
Savings Per Unit	$0.28
TOTAL SAVINGS	$137,200
Hiring Bonus Cost ($10,000 per person)	$60,000
EXPECTED TOTAL PROFIT FOR MAXIM	$77,200

5.3. Organization of the Task

The project tasks are divided and distributed to each of the three teams: receiver team, transmitter team, and frequency synthesis team. The division of tasks between teams allows us to specialize in different areas of the W-CDMA transceiver to provide maximum efficiency towards the tasks at hand. This method of task division is an efficient means to accomplish a large task in a small amount of time; however, the true meaning of teamwork becomes apparent when the project end nears and each team member uses their individual brush to paint their portion of the final mosaic.

The primary means of scheduling tasks throughout the project are e-mail, teleconferences, meetings, and lectures. Logs of all communications are kept in each of our respective notebooks for record keeping. During the initial phase of the project, scheduling consists of the coordination of research assignments with our respective mentors via e-mail in order to guide us in the development of the necessary radio frequency design skills. Scheduled lectures given by mentoring Maxim engineers helped fine-tune the skills we are developing. Upon development of these skills, tasks were assigned from our mentors via e-mail to calculate necessary radio frequency design parameters pertinent to our respective designs. Teleconference sessions were established to answer technical questions that arose throughout the project. The communication links utilized to schedule the hardware design, implementation, and test phase of our project in Sunnyvale were strictly routed via the project advisor. A summary of the project timelines is provided in Table 5.3-1.

Table 5.3-1. Project timeline.

January	Senior design projects assigned
	Problem definition
	Purchase RF Microelectronics textbook by Ben Razavi
	Begin to read text and research on internet
February	Read first five chapters of Razavi
	Bob Kelly lectures on basic RF electronics
	Assignments to teams with respective mentors
March	Analysis of reference design begins
	Research continues; RF system analysis begins
	Begin preparing for mid-quarter presentations
April	Dave Devries lectures on effects of noise in a transceiver
	Mid-quarter presentations
	Focus shifts from "RF analysis" to "filter design"
May	Extensive research in filter design
	Filter design simulations
	Preparation for trip to Maxim Laboratories in Sunnyvale, CA
	Design, implementation, & testing of prototype filters
	Post-implementation analysis
June	Complete final report
	Generate slides for oral presentation

Chapter Six – Meeting Expectations

6.1. Introduction

This chapter focuses on the issue of whether or not the initial specifications of the design have been met. Perhaps the most substantial part of any project lies in the results that show if the design works. Section 6.2 explicitly declares whether the design has satisfied all the desired specifications. Section 6.3 summarizes important elements of design.

6.2. Design Constraints

As the constraints are very different for each of the three subproblems, they are addressed separately in the following three subsections.

6.2.1. Receiver

Many designs are created in today's world, however there must sometimes be some sacrifices. These include values on actual components not meeting designed component values, other component selections that may be suited to do the job but have features that are unnecessary, and other related hardware that is used for one design but not suitable for the task at hand.

When manufacturers create components such as resistors and capacitors, it is impossible to produce every value from one to infinity. For example, resistors come in discrete values like 1 kΩ, 2 kΩ, and 10 kΩ. Such is the case when building the physical prototype of our design. In Table 6.2.1-1 the designed values for resistors and capacitors are compared with the actual values used. One of the actual capacitors varied by 6 pF from the designed value. While the designer can take into account the fact that these components are not available for every value he or she can imagine, a certain amount of common sense as well as experience play a major role in the selection of components. Our design required some "tweaking" in order to correct for a bump located at the corner frequency. In the *PSpice* simulations a bump created an unwanted extra gain in the pass-band before transitioning to the stop-band as illustrated in Fig. 4.3.1-2. For this, the resistor and capacitor values of the second stage were altered to provide a smoother transition and to flatten out the bump, Fig. 4.3.1-1.

Table 6.2.1-1. Comparison between designed component values and actual values used (continued on the next page).

Component	Designed Value	Actual Value
C_1	74 pF	68 pF (±5%)
C_2	21 pF	22 pF (±5%)
C_3	22 pF	22 pF (±5%)
C_4	72 pF	68 pF (±5%)
R_1	1 kΩ	1.07 kΩ (±1%)
R_2	329 Ω	332 Ω (±1%)
R_3	2.3 kΩ	2 kΩ (±1%)

R_4	1 kΩ	1.07 kΩ (±1%)
R_5	1 kΩ	1.07 kΩ (±1%)
U_1	THS4121	THS4121
U_2	THS4121	THS4121

In our design we call for a single-ended output from our filter, yet we use an op-amp, which supports differential outputs. The op-amp is within the range of performance that is required by our design and meets these specifications, but is over-designed because it supports a feature that is not used. This design constraint arose from the fact that the op-amp used was the only one available to us that also met our design specifications.

The last design constraint that affected our design was the etched surface-mount board that was used to build our designed circuit. In the interest of time, the board used was designed for another filter, but had some similar design elements. For example, the circuit that the board was etched for used two op-amps. Since our designed circuit used two op-amps with surrounding resistors and capacitors, the board was suitable. It is important to note that none of these constraints had any adverse affect on our filter's performance.

6.2.2. Transmitter

The transmitter BPF design specifications in Table 2.3.2-1 require the IF / BPF to exhibit a center frequency of 380 MHz, a 3 dB bandwidth of at least 6.8 MHz, at least 37 dB of attenuation at 190 MHz, and at least 40 dB of attenuation at 760 MHz. Without taking finite inductor Q into account, designing a filter on paper to meet specifications is relatively easy. However, at our frequencies, once the effects of finite Q are taken into account, the insertion loss and 3 dB bandwidth can change drastically.

The availability of discrete-valued components (mentioned in the previous section) and the presence of stray capacitance are also constraints. However, these constraints can be partially overcome using the method to fine-tune a resonant circuit discussed in Section 4.3.2. This constraint of finite component values can be insightful to a beginning filter circuit designer, as the process of shaping the response of the filter immediately demonstrates practical effects of various component changes.

Perhaps a more crucial constraint is that of time during the implementation and testing phase. If the time available to assemble and test a high-frequency circuit is limited, as it usually is, this constraint proves very difficult to overcome. Many time-consuming circuit modifications can be necessary to assemble, test, modify, and fine-tune a filter design. This constraint is evident in Section 4.2.2, where many modifications become necessary prior to obtaining a satisfactory filter response.

Last, but certainly not least, financial constraints must be considered. Based on the cost analysis in Section 5.2, a production of 500,000 filters at a successful sales rate of 98% will result in an expected total profit of $77,200. This amount of profit results after a hiring bonus of $10,000 is given to each of the six graduating engineers assigned to the project. With all circuit

constraints, time constraints, and financial constraints considered, the experimental test results in Section 4.3.2 confirm that the filter design specifications have been met.

6.2.3. Frequency Synthesizer

The major goals in the design of a PLL frequency synthesizer, aside from producing the desired signal at a determined frequency, are to achieve low phase noise, low spurious output, and a quick settling time. The results for all three of these aspects have already been determined and presented in this report for both simulation and experiment. This section discusses whether the results meet industry requirements, and if not then what changes need to be made.

Phase noise:

Table 6.2.3-1. A typical VCO phase noise response [20].

Offset (kHz)	Phase noise (dBc)
1	-80
12.5	-105
30	-111
120	-121
900	-128

Our phase noise results:

Table 6.2.3-2. Measured VCO phase noise response.

Offset (kHz)	Phase noise (dBc)
1	-58.3
10	-75.3
100	-92.17
1000	-102.17

By comparing the above tables, it appears that our results are a little noisy. This is largely due to the small bandwidth having little effect on VCO phase noise. An alternative approach to the design, Fractional-N architecture, may have achieved better phase noise performance, but the degradation in spurious noise performance may not have been a wise tradeoff. Our spurious noise attenuation level at the first offset reference multiple is about –58 dB. For the transmit IF / PLL, the spurious noise level requirement is –58.16 dB [5]. Our spurious noise attenuation is acceptable but the overall phase noise performance did not fully meet minimum noise requirements. Any extra noise that is present from 0 to 1.5 kHz offset can be contributed to errors in loop filter design and has been justified in Section 4.3.3. The very same elements that cause our experiment to stray from our simulation cause our experiment to have a less than desired phase noise performance. Any extra noise present outside of 1.5 kHz is dominated by tank components, like the inductor and varactor, which are related to but not part of our design. Better attenuation can be achieved by using tank components with a higher

quality value [11]. Other possible reasons for insufficient noise performance outside our design reside in the bad board layout resulting in a crosstalk, and noise from the voltage supply.

The experimental settling time of our design was 5 ms. Under normal operating conditions for an IF / PLL, this time is sufficient since it does not need to switch from channel to channel. However, for a time duplex mode, the PLL would be turned off to conserve power, then turned on again to transmit the signal. This would create the need for a fast settling time of no more than 5 ms.

This design worked but could benefit tremendously from a few modifications. With the knowledge of actual design parameters, a revised design can be tailor-made to fit the system. The new design would have a profound increase in phase noise performance due to the customization of the loop filter to the surrounding components, whose exact characteristics are now known.

6.3. Elements of Design

Issue	Effects of our design
Economic Factors	There are many economic factors that influence a design. We have covered a cost analysis in Chapter Five, which gives us a good idea of what it would cost to mass-produce our design. Though this is a good rough estimate, the fact that there are other companies out there wanting to make money from producing a similar product is another factor that must be considered. Through supply and demand, many companies may not be competitive enough to survive and this would cause loss of jobs, however it would also supply the customer with superior products.
Safety	While the actual manufacturing processes involved with mass-producing our design may involve some drawbacks to the environment, all responsibilities fall on the manufacturer to conduct itself accordingly. As for our responsibilities when making a prototype, all known precautions were taken to ensure the safety of all involved.
Reliability	No extensive tests were made to ensure the long-term reliability of our design. However, to the best of our knowledge, we have no reason to believe that our design would not be worthy of long-term use.
Aesthetics	Prototypes that were made during this project were constructed for test purposes only and were not optimized for appearance. They were merely meant to provide us with knowledge and skills related to our particular design. With further design and testing a prototype worthy of being produced, which not only works to designed specifications, but also looks good, could be achieved.
Ethics	In reviewing the IEEE Code of Ethics, we have done nothing but try to better our understanding of this technology as well as help each other along the way, working together as a team. We often criticized and complimented each other during our time working together. Throughout this project, we have conducted ourselves in nothing but a professional manner and have done nothing to harm the reputations of others involved in this project. By reporting all of our work and findings in this report, we have given credit where needed and we have presented our findings with the utmost honesty.
Social Impacts	With many people desiring portable communications devices in today's fast-paced world, our design will play a major role in furthering the wants and needs of these types of people.

Chapter Seven – Conclusions

7.1. Introduction

This chapter is designed to give closure to the entire project and report. Each of our three design tasks proved to be challenging and to require creativity. Intriguing hours were spent on understanding each component and its effect on the entire system. Our designs proved to be accurate through simulation and by way of actual implementation, and can be implemented in industry with only minor modifications. We are satisfied with our results and feel that we have fulfilled our job requirements.

7.2. Expansion and Improvement

7.2.1. Receiver

Due to a time constraint certain aspects like temperature were not tackled in our design. These aspects of design were not crucial to a successful demonstration of our design. Another consideration that was not addressed was the concept of "commercial application." Therefore, this report creates the foundation for future investigations in those areas. Although some of these issues were not considered, those did not impact our design in any way. The issues that were not addressed could be something for future expansion and design improvement for the next generation. Overall, the results presented in this report regarding all aspects of our design show that our design worked quite well.

7.2.2. Transmitter

The UCR / Maxim Senior Design Project has been a very valuable learning experience. The project has given us valuable experience in radio frequency communication system analysis and design, which would not have been obtained through available coursework at UCR. The project has provided us with an exposure to "real world" engineering problem solving techniques and has helped us to establish networking foundations in the corporate environment. Some possibilities for expansion within the transmitter project are to examine in greater detail one of the other areas within the transmit path, such as the quadrature modulator, variable gain amplifiers, or power amplifier. A possibility for future work on the IF / BPF is to implement the filter on-board a working cellular phone in order to determine its practical advantages and disadvantages.

7.2.3. Frequency Synthesizer

Though this project has resulted in a complete working design, there is much to be desired and that can be passed on to the next group of students that wish to take on this project. Since this was a new project, new goals and objectives were created as the project developed. The next group of students could benefit from a pre-developed time line that gives explicit tasks and dates for which each task should be completed. This would ensure proper progress throughout the project. Indefinite access to the proper test equipment would tremendously improve the end

results because the students would have the capabilities to design and test as they go through each step in building their project.

Future students should also look into implementing the third-order loop filter, which would provide a spurious-free signal. The design of the third-order filter is complete, so future students may want to take measurements and compare this to the simulated and actual requirement in order to analyze its impact on the system. Future students should pay closer attention to the amount of charge current being used so that techniques such as turbo tracking can be implemented. Understanding and knowing how the equipment works will speed up the process.

7.3. User's Manual

The MAX2310 EV kit is used in testing the receive low-pass filter, and the MAX2360 EV kit is used in tests involving the transmit IF band-pass filter and frequency synthesizer designs. Please refer to the corresponding evaluation kit documentation for additional information on conducting tests with these boards.

Appendix A: Parts List

A.1. Receiver portion

Part Name	Quantity	Value/Part Number	Manufacturer
Resistor	3	1.07 kΩ (±1%)	
Resistor	1	2 kΩ (±1%)	
Resistor	1	332 Ω (±1%)	
Capacitor	2	68 pF (±5%)	Murata
Capacitor	2	22 pF (±5%)	Murata
Capacitor	4	0.1 μF (±5%)	Murata
Op-Amp	2	THS4121	Texas Instruments
Jumper Wires	6	Various lengths	
Surface Mount Board	1		
Coaxial Connectors	3		

A.2. Transmitter portion

A.2.1. Production circuit (given in Fig. 3.2.2-3)

Designation	Qty	Value	Part Number
C_1	1	12 pF 5% ceramic capacitor (0402)	Murata GRM36C0G120J050
C_2	1	10 pF 5% ceramic capacitor (0402)	Murata GRM36C0G100J050
C_{12a}, C_{12b}	2	1.6 ± 0.1 pF ceramic capacitors (0402)	Murata GRM36C0G1R6B050
L_{1a}, L_{1b}	2	15 nH 5% inductor (0603)	Coilcraft 0603CS-15NXJBC
L_2	1	6.8 nH 5% inductors (0603)	Coilcraft 0603CS-6N8XJBC

A.2.2. Prototype circuit (given in Fig. 4.2.2.3-1)

Designation	Qty	Value	Part Number
C_{1a}, C_{1b}	2	8 ± 0.5 pF ceramic capacitor (0402)	Murata GRM36C0G080D50
C_{2a}, C_{2b}	2	1.5 ± 0.1 pF ceramic capacitors (0402)	Murata GRM36C0G1R6B050
C_3, C_4	2	1.5 ± 0.1 pF ceramic capacitors (0603)	Murata
L_1, L_2	2	15 nH 5% inductors (0805)	Coilcraft
R_1, R_2	2	200 Ω 5% resistors (0603)	
R_3, R_4	2	100 Ω 5% resistors (0603)	
T_1, T_2	2	Balun transformers (B5F type)	Toko 458DB-1011
	2	SMA connectors	Digikey J502-ND
	1	PCB	
	6"	Coaxial wire	

A.3. Frequency synthesizer portion

Designation	Qty	Value	Manufacturer
C_1	1	220 nF 5% ceramic capacitor	Murata
C_2	1	68 pF 5% ceramic capacitor	Murata
R_2	1	11 kΩ 5% resistor	

Appendix B: Equipment List

HP 8560E Spectrum Analyzer (30 Hz –2.9 GHz)	$19800
Agilent E4433B ESG-D Series Signal Generator (250 kHz – 4 GHz)	$18450
Hewlett Packard 8753E RF Network Analyzer (30 kHz – 6 GHz)	$35600
Hewlett Packard E3630A Triple Outlet DC Power Supply	$525
Hewlett Packard 8648C Signal Generator (100 kHz – 3.2 GHz)	$16000
Personal Computer	$2000
Stereo Microscope (20X)	$1450
Weller WES50 Soldering Station (2 @ $110 ea)	$220

Appendix C: Software List

MATLAB, Version 6.0	$845
MAX 236x EV PC-Control Software Ver 5.00.26	Freeware
Microsoft Office XP Professional	$580
ORCAD PSPICE, Version 9.0	$1495
PLL Made Easier, Version 1.5	Freeware

Appendix D: Special Resources

Maxim Headquarters Facilities
Maxim Technical Personnel

Appendix E: Parts Cost Breakdown

MAX 2361 Evaluation Board		$200
MAX 2310 Evaluation Board		$200
Printed Circuit Board		$30
<u>Transmitter Differential Band-Pass Filter (goes on EV board or a production unit):</u>		
(2) 6.8 nH 5% inductors (0603)	10ea = $5.63, 1000ea	= $198.75
(1) 15 nH 5% inductor (0603)	10ea = $5.63, 1000ea	= $198.75
(2) 1.6 pF ± 0.1 pF ceramic capacitors (0402)	10ea = $2.38, 1000ea	= $91.50
(1) 10 pF 5% ceramic capacitor (0402)	10ea = $0.77, 1000ea	= $18.20
(1) 12 pF 5% ceramic capacitor (0402)	10ea = $0.77, 1000ea	= $18.20
<u>Transmitter Band-Pass Filter Prototype:</u>		
(2) 1.5 pF ± 0.1 pF ceramic capacitors (0603)	10ea = $0.87, 1000ea	= $32.30
(2) 9.5 pF 5% ceramic capacitors (0402)	10ea = $0.77, 1000ea	= $18.20
(2) 15 nH 5% inductors (0804)	10ea = $5.63, 1000ea	= $198.75
(2) 100 Ω 5% resistors (0603)	10ea = $0.80, 1000ea	= $16.82
(2) 200 Ω 5% resistors (0603)	10ea = $0.80, 1000ea	= $16.82
(2) Balun transformers (B5F type, TOKO 458DB-1011)	1ea = $2.89, 100ea	= $186.12
(2) SMA connectors (DIGI-KEY J502-ND)	1ea = $5.88, 500ea	= $1265.25
(1) Coaxial wire spool	100ft = $34.39, 500ft	= $150.46
<u>Receiver Low-Pass Filter:</u>		
(1) 332 Ω 1% resistor (0402)	10ea = $0.84, 1000ea	= $177.00
(3) 1.07 kΩ 1% resistors (0402)	10ea = $0.84, 1000ea	= $177.00
(1) 2 kΩ 1% resistor (0402)	10ea = $0.84, 1000ea	= $177.00
(4) 0.1 uF ± 5% ceramic capacitors (0603)	1ea = $0.24, 10000ea	= $1000.00
(2) 22 pF ± 5% ceramic capacitors (0603)	1ea = $0.24, 10000ea	= $1000.00
(2) 68 pF ± 5% ceramic capacitors (0603)	1ea = $0.24, 10000ea	= $1000.00
(2) THS4121 Texas Instruments Op Amp (DGN)	1ea = $3.51, 5000ea	= $9750.
(1) Jumper Wire 30 AWG	75ea = $5.49,	N/A
(1) Surface Mount Board	1ea = $3.08,	N/A
(3) SMA connectors (DIGI-KEY J502-ND)	1ea = $5.88, 500ea	= $1265.25
<u>Frequency Synthesizer Loop Filter:</u>		
(1) 11 kΩ 5% resistor (0402)	10ea = $0.80, 1000ea	= $16.82
(1) 68 nF ± 5% ceramic capacitors (0402)	1ea = $0.24, 10000ea	= $1000.00
(1) 220 pF ± 5% ceramic capacitors (0402)	1ea = $0.24, 10000ea	= $1000.00

Appendix F: *Matlab* Code for Loop Filter Design

```
%Heath Deuel
%Oscar L. Servin
%Senior Design

%Software to design a loop filter.

Phase = 55;                    %Degrees.
Kvco  = 15e6;                  %Hz/V.
Kphi  = 175e-3;                %Amps.
Fref  = 75e3;                        %Hz.
Fout  = 760e6                        %Hz.
ATTEN = 20;                          %dB.

N = Fout/Fref;

%First time constants.
T1 = (sec(Phase*pi/180)-tan(Phase*pi/180))/1.256E5;

%Third time constants.
T3 = sqrt((10^(ATTEN/20)-1)/(2*pi*Fref)^2);

%Cutoff frequency.
wc1 = (tan(Phase*pi/180)*(T1+T3))/((T1+T3)^2+(T1*T3));
wc2 = (((T1+T3)^2+(T1*T3))/((tan(Phase*pi/180)*(T1+T3))^2));
wc3 = sqrt(1+wc2)-1;
wc = wc1*wc3     %rad
BW3 = wc/(2*pi) %Hz

%Second time constant.
T2 = 1/((wc^2)*(T1+T3));

%Second-order bandwidth.
wp = 1/(sqrt(T2*T1))     %rad
BW2 = wp/(2*pi)          %Hz


C1 = (T1/T2)*((Kphi*Kvco)/(wc^2*N))*(sqrt((1+wc^2*T2^2)/((1+wc^2*T1^2)*(1+wc^
2*T3^2))))
C2 = C1*(T2/T1 - 1)
C3 = C1/10

R2 = T2/C2

%Rule of thumb, choose R3 to be AT LEAST twice the value of R2!
R3 = 0.1*(C2*R2)/C3

%Damping ratio.
zeta = ((R2*C2)/2)*sqrt((Kphi*Kvco)/(N*(C1+C2+C3)));

%Natural frequency.
wn = sqrt((Kphi*Kvco)/(N*(C1+C2+C3)));

%Settling time.
Ts = 4/(zeta*wn)
```

```
pause

C1 = 330e-12;
C2 = 68000e-12;
R2 = 11e3;

%Transfer function second-order approximation (closed loop).
numZ = [(C2*R2) 1];
denZ = [(C1*C2*R2) (C1+C2) 0]

Z = tf(numZ,denZ)
H = tf([1],[N 0])
G = H*Z*Kvco*Kphi

%Third-order open loop.
numZ1 = [(C2*R2) 1];
denZ1 = [(C1*C2*C3*R2*R3) (C2*C3*R2+C1*C2*R2+C1*C3*R3+C2*C3*R3) (C1+C2+C3) 0]

Z1 = tf(numZ1,denZ1)
H1 = tf([1],[N 0])
G1 = H*Z1*Kvco*Kphi

%Third-order closed loop.
numZ2 = [(C2*R2) 1];
denZ2 = [(C1*C2*C3*R2*R3) (C2*C3*R2+C1*C2*R2+C1*C3*R3+C2*C3*R3) (C1+C2+C3) 0]

Z2 = tf(numZ2,denZ2)
H2 = tf([1],[N 0])
G2 = H*Z2*Kvco*Kphi/(1+H*Z2*Kvco*Kphi)

clf
grid on
Bode(G)
hold on
%Bode(G1)
%Bode(G2)
```

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