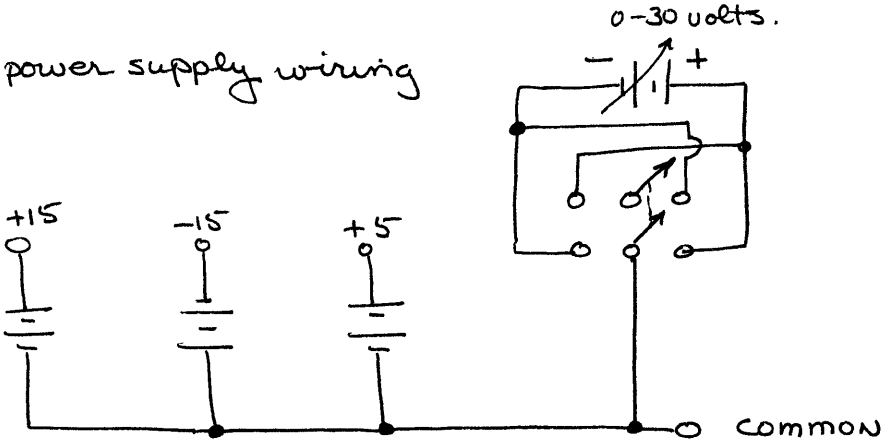
station lay-out

simplified power supply wiring



Dmm is electrically separate from common

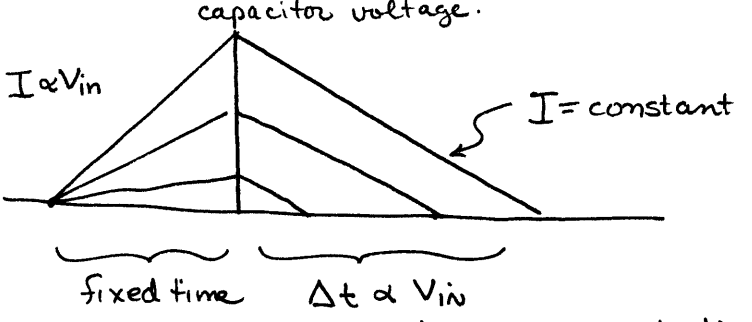
three modes of measurement.

- single ended
- differential
- current

frequency limited performance.

uses low frequency, very accurate dual slope integration

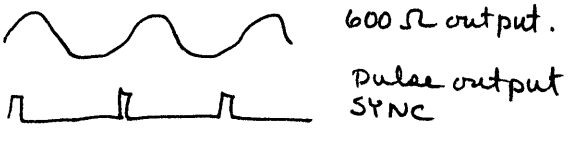
see p. 418 Horowitz

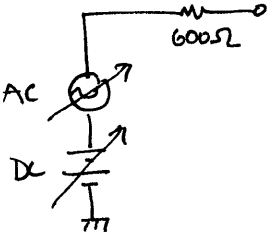


use digital counter to time this period

Signal generator

2 - outputs.





EEAP 243 Lecture #2.

Lab #1 done this week

Lab partners posted tonite if not assigned

Labs due tuesday next week. (where ?)

announce in next class

→ Office hours Thursday 10 – 3

Lab questions assigned : 1, 4, 7 MUST BE TYPED

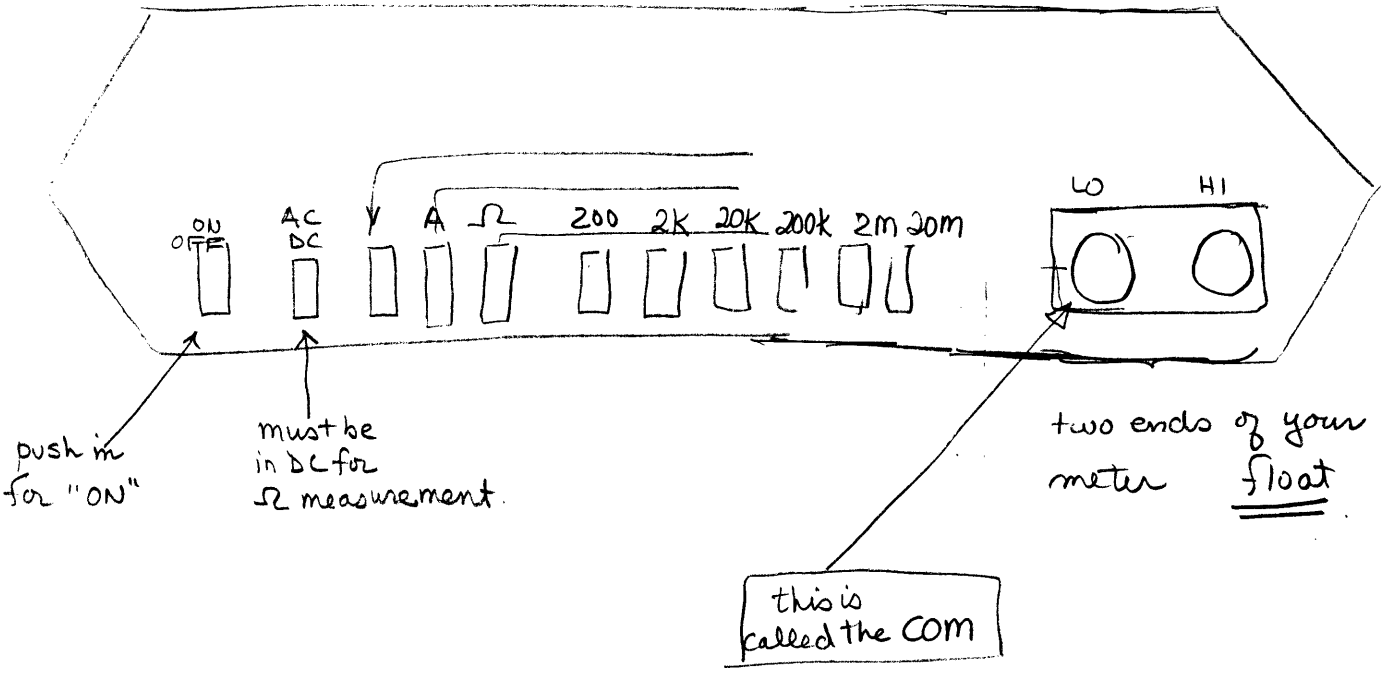
INCLUDE DATA LOG SHEET
(will be returned)

T.A. must initial data sheet (and date it)

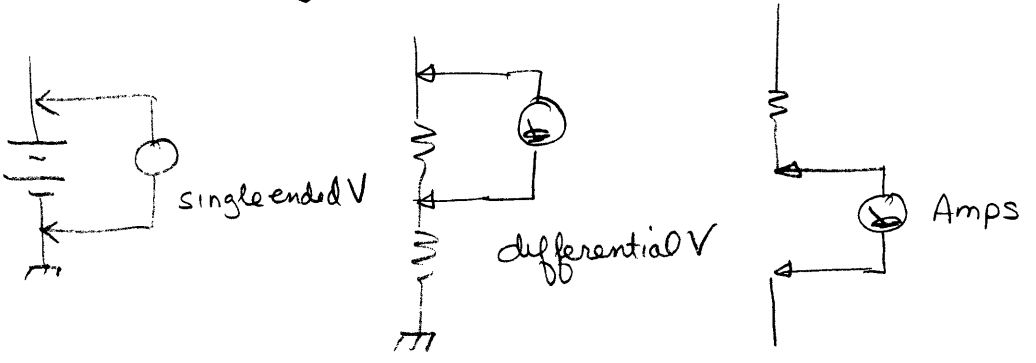
make up labs MONDAY
TUESDAY } evening 7-9 pm.

Dmm

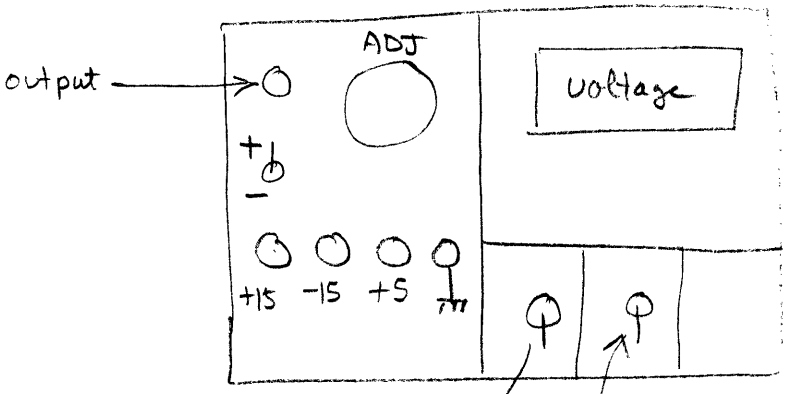
we don't have Keithley's
we have Flukes.



How to measure voltage & current

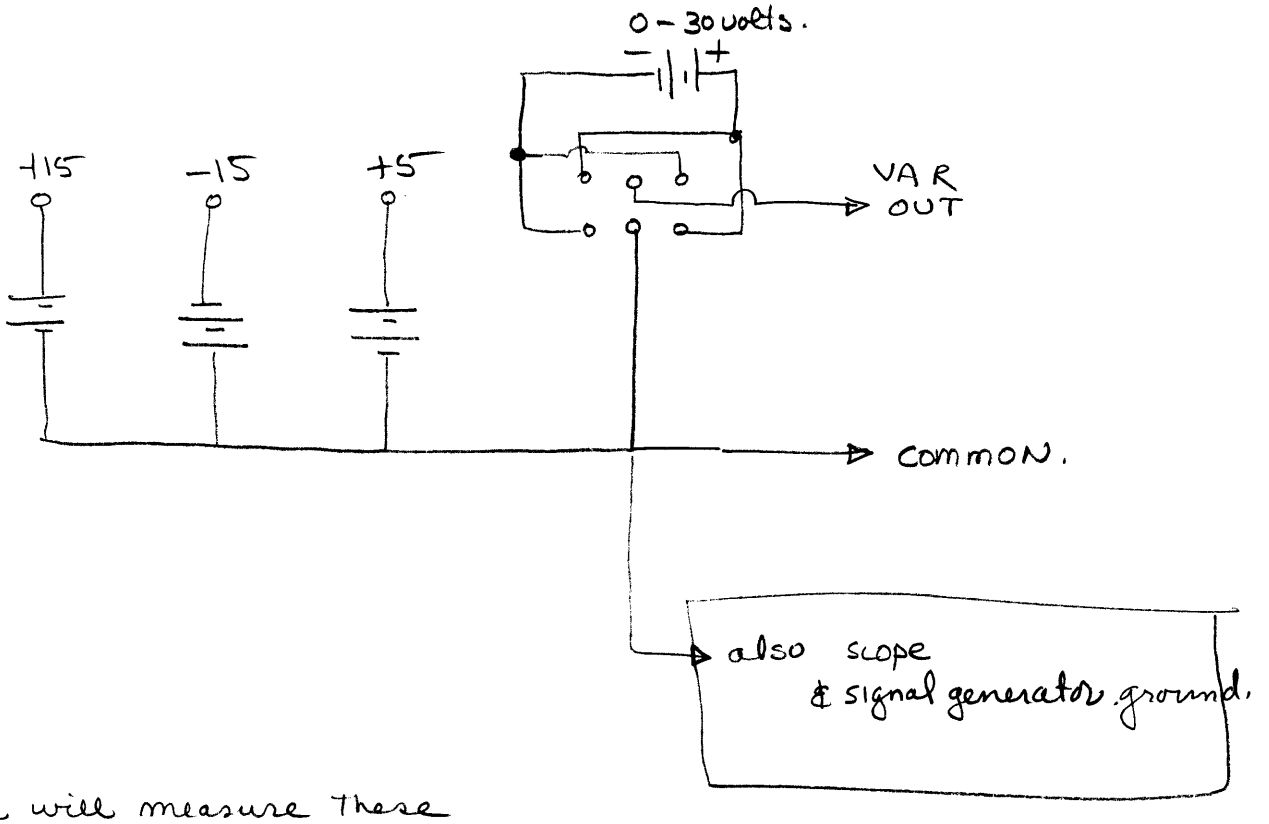


Power supplies:



all power incl. instruments.

power to supplies

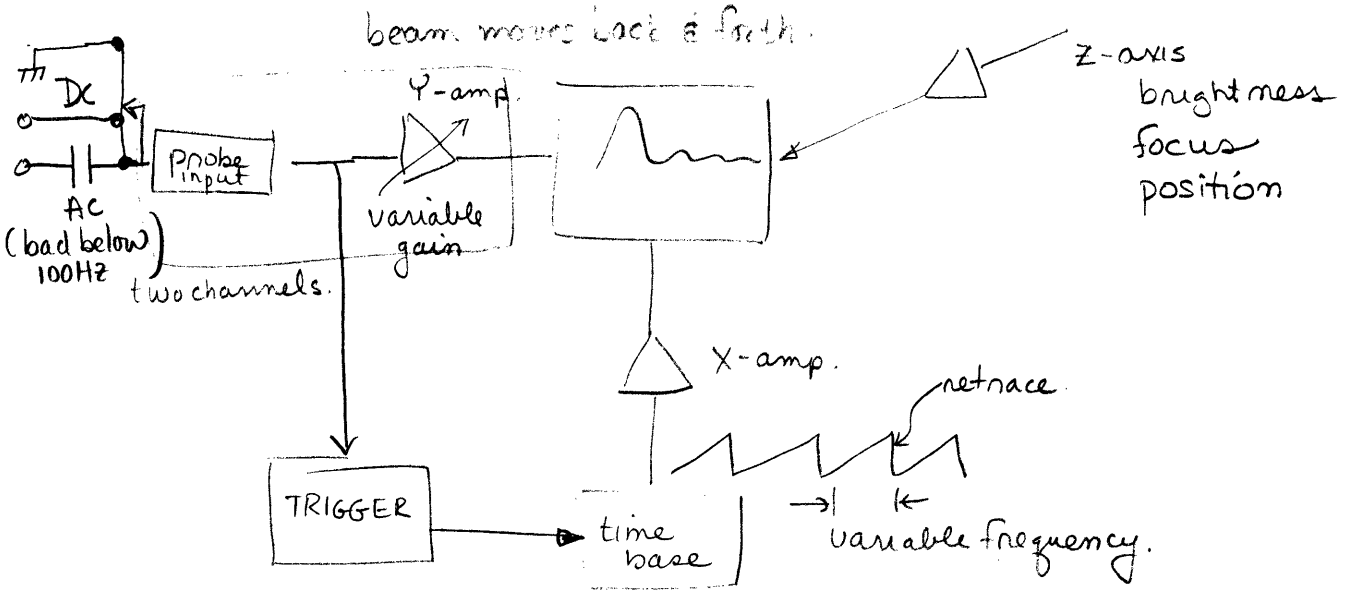


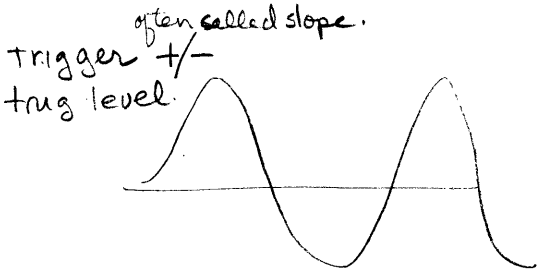
You will measure these voltages. Use DC power switch

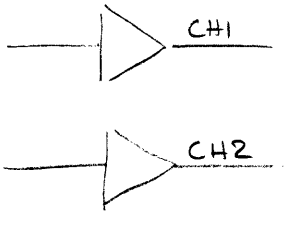
No reading if com not connected!

Scope

basic background



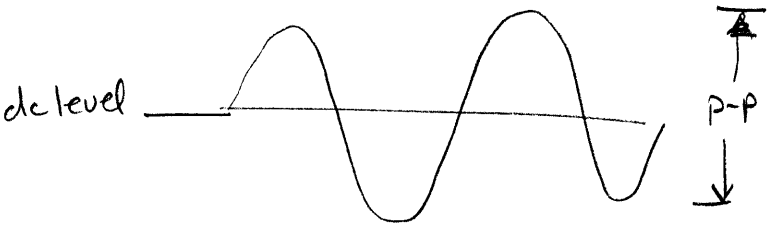




CH1 } single channel.
CH2 }
DUAL } most used.
ADD }
X-Y

POINT OUT VARIABLE SENSITIVITY. multiples sensitivity
i.e. reduces it
TURN CLOCKWISE

MAGNIFY – don't push IN.



adjust to coupling you want.

adjust gnd to some screen marking.

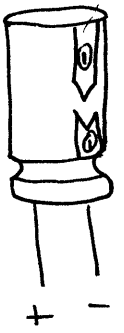
trigger slope +/− } synchronizes oscillator with
level input voltage level.

Bright Line should always be out.
Is a special automatic sweep.
if NO signal keeps screen display!

lab write-ups due by start of next lab – typically Tuesday.

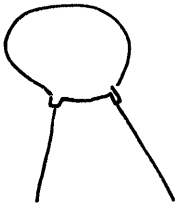
resistors
(transparancy)

capacitors
electrolytics
tantalum



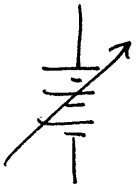
can explode if you reverse polarity

disk ceramics



flat.

symbols used



variable power supply

signal generator

RSB or pot.

go to rsb.

EEAP 243

CIRCUITS LABORATORY

LABORATORY HANDBOOK

SPRING 1988

PROFESSOR F. MERAT
GLENNAN 515
368-4572

EEAP 243 COURSE GRADING POLICY

1. Each lab will be worth a maximum of four points.
   A≥3.5
   B≥2.5
   C≥1.5
   D≥1
   F<1
2. Late labs will be deducted 1 point per day late to a maximum of three points to be deducted–any lab not handed in will count -3 points toward your final grade.
3. There will be no final.
4. All grades will be based upon points accumulated in the course through graded labs.
5. The final course grade will be based upon the following point distribution:
   A≥52.5
   B≥37.5
   C≥22.5
   D≥15
   F<15

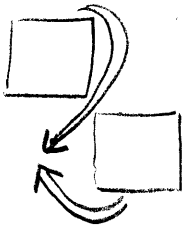
   assuming that 15 labs will be assigned. If 15 labs are not assigned (very likely) the grade cutoff points will be reduced proportionately.
7. Lab writeups will consist of the data collected by the lab group PLUS the answers to assigned questions. The proper collection of the lab data will be worth one point; the answers to the lab questions will be worth three points.

☞ Your grade will be based upon a strict interpretation of this point distribution and the above rules. There will be no exceptions without notes from the Dean's Office.

No student who has not passed EEAP 241 (or its equivalent) and is not concurrently enrolled in EEAP 242 will be allowed to take EEAP 243. The only exception will be students who have already taken EEAP 242 or its equivalent.

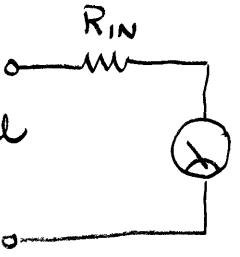
LAB #2 (Assign questions 2, 4, 6, 7)

Lab requires two meters — work across

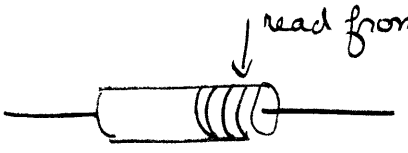


models of most instruments include internal resistances

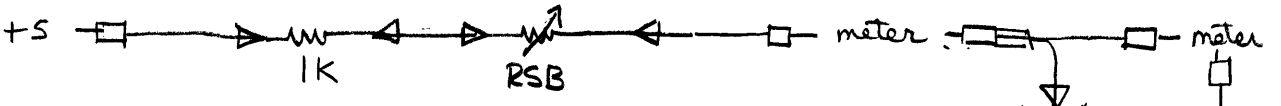
typical meter model

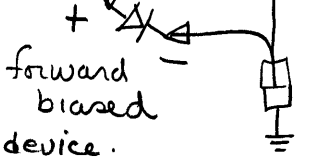


resistors

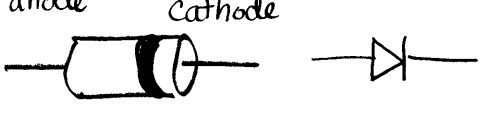


connect circuit on your proto board or <u>just use clips.</u>

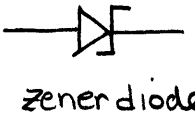




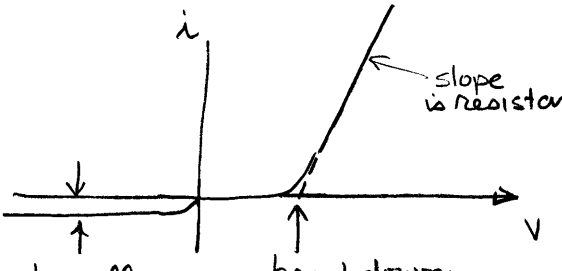
ordinary diode

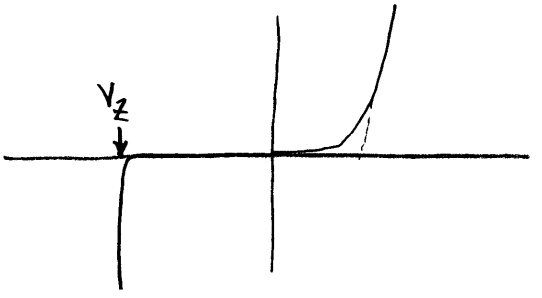


Boylestad and Nashelsky have a good explanation

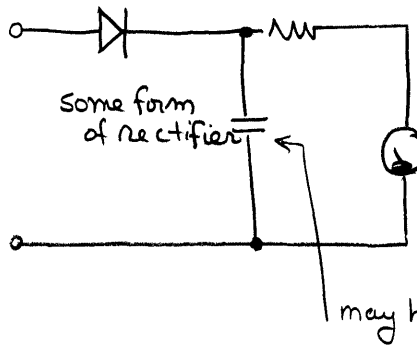


zener diode



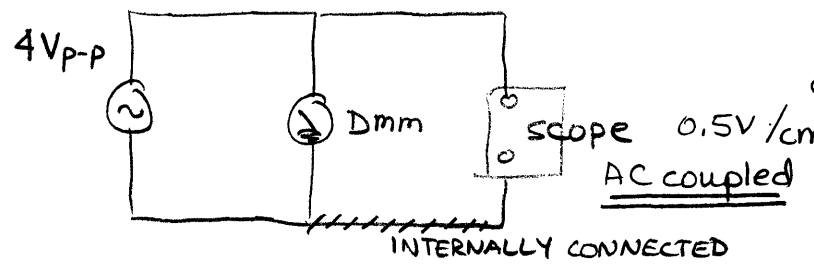


AC measurements:



dc meter (will measure ac AND DC present)

could be confusing



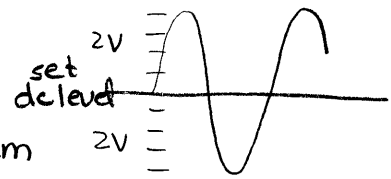


table 2-5

	vernier signal generat	range	time	scope	meter
frequency ↓			[this is NOT critical]	(Volts Not cm)	(set to AC volts)

RMS Measurements

general

$$V_{RMS} = \sqrt{(AC)^2 + (DC)^2}$$

more technically:

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T V^2(t)\,dt}$$

For sinusoidal signals the above formula reduces to

if $V(t) = V_m \cos \omega t$

$$V_{RMS} = \frac{V_m}{\sqrt{2}}$$

For signals of different frequencies

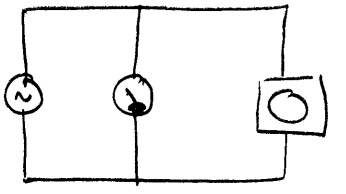
$$V_{1rms} = \sqrt{V_{f1,rms}^2 + V_{f2,rms}^2 + \ldots + V_{fn,rms}^2}$$

↑ one of these can be dc

Note that the rms value of a dc voltage is the dc voltage.

For triangle $V_{RMS} = \frac{V_m}{\sqrt{3}}$

for this lab



$4V_{p-p}$ +1V DC offset

DC coupled

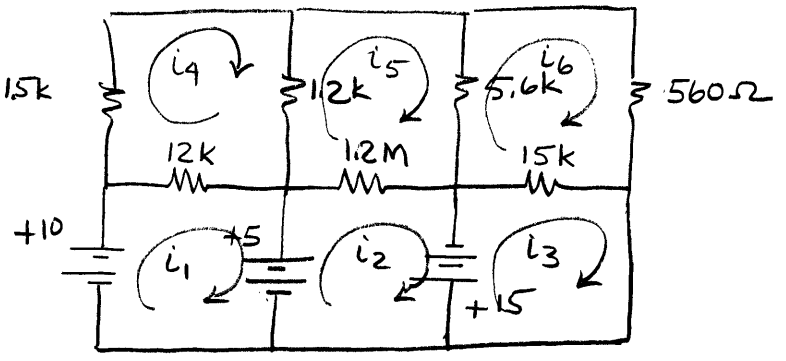
do for sine square triangle pulse

measure AC & DC components.

pulse is a little misleading

Part 4 KCL

LAY THIS OUT BEFORE YOU COME TO CLASS



Record tolerances of your resistors

use superposition
loop equations, etc.

$$-10 + 12k(i_1 - i_4) + 5 = 0$$

$$-5 + 1.2M(i_2 - i_5) - 15 = 0$$

$$+15 + 15k(i_3 - i_6) = 0$$

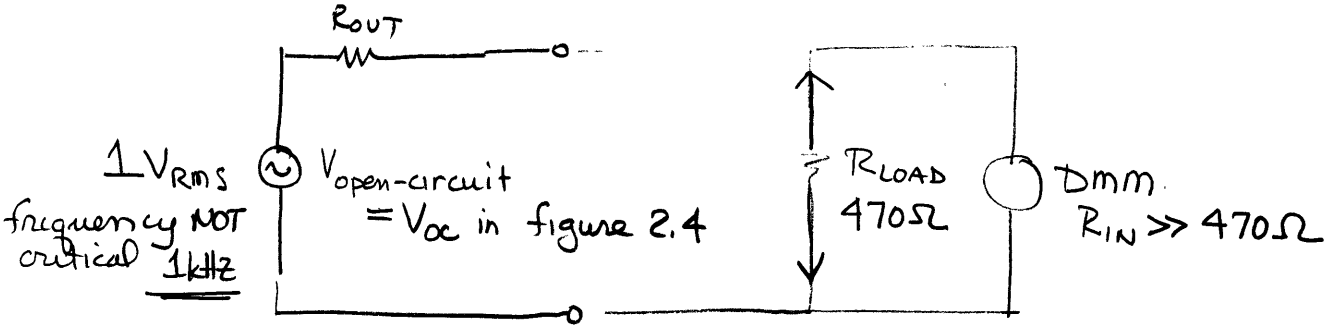
$$15k(i_4) + 12k(i_4 - i_1) + 1.2k(i_4 - i_5) = 0$$

$$1.2k(i_5 - i_4) + 1.2M(i_5 - i_2) + 5.6k(i_5 - i_6) = 0$$

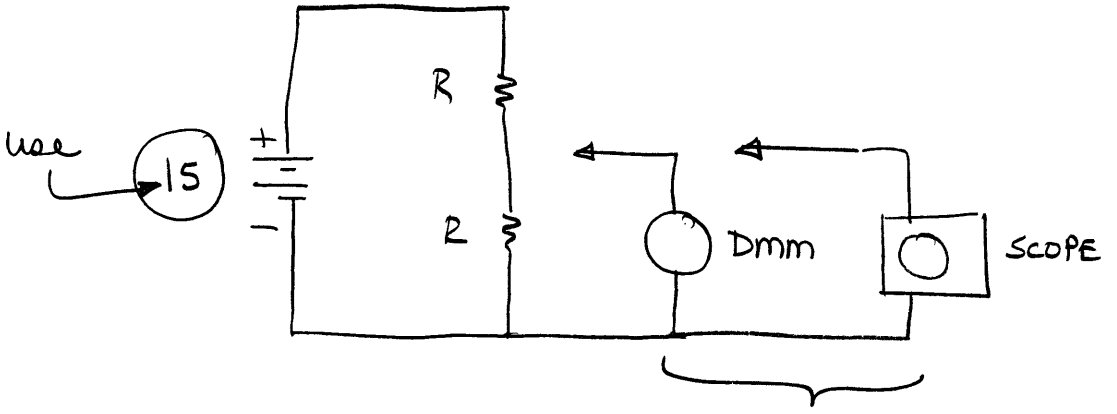
$$5.6k(i_6 - i_5) + 15k(i_6 - i_3) + 560\, i_6 = 0$$

6 equations in 6 unknowns.

Part 5 – Z of test equipment



VOLTAGE DIVIDER



R initially = 10kΩ.

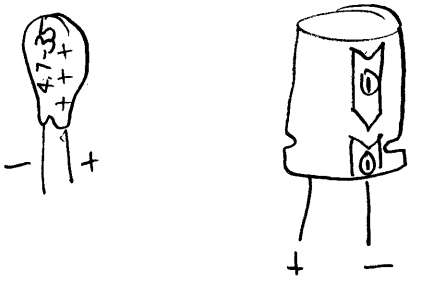
probably won't detect any differences until R=1M or 10M

capacitors

marked with value in microfarads
or scientific notation in picofarads $\#\#\times 10^{\#}$

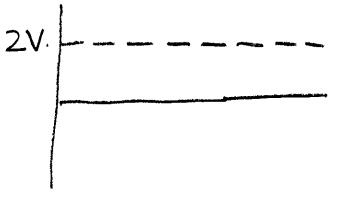
$\therefore 333 = 33{,}000\,pf = .033\,pf.$

very important which way electrolytics go in a circuit

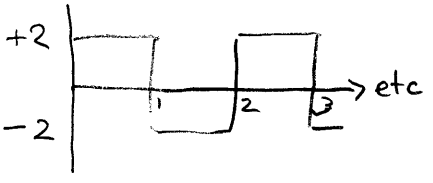


capacitors can explode if polarity is reversed

rms voltages $V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}$



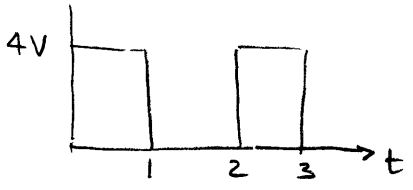
$V_{rms} = 2V.$ since $\sqrt{\frac{1}{T}\int_0^T 2^2\,dt} = \sqrt{\frac{1}{T}4t\Big|_0^T} = 2$



$$V_{rms} = \sqrt{\frac{1}{2}\left[\int_0^1 (2)^2\,dt + \int_1^2 (-2)^2\,dt\right]}$$

$$= \sqrt{\frac{1}{2}4 + \frac{1}{2}\cdot 4} = \sqrt{4} = 2$$

Add two together



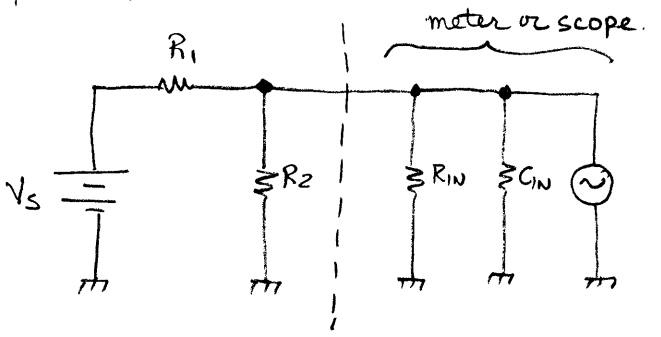
$$V_{rms} = \sqrt{\frac{1}{2}\int_0^1 (4)^2\,dt} = \sqrt{\frac{1}{2}\cdot 16} = 2\sqrt{2}\ \text{volts}$$

this is the basis for the formula

$$V_{rms} = \sqrt{V_{AC,rms}^2 + V_{dc}^2}$$

$$= \sqrt{4+4} = 2\sqrt{2}$$

Input impedance and time response.



for dc. $V_{o,ideal} = V_S \dfrac{R_2}{R_1+R_2}$

$V_{o,real} \quad V_S \cdot \dfrac{R_2 \parallel R_{IN}}{R_1 + R_2 \parallel R_{IN}}$

if $R_1 = R_2 = R$ for $R_{IN} \gg R$ $V_o \cong \frac{1}{2} V_S$

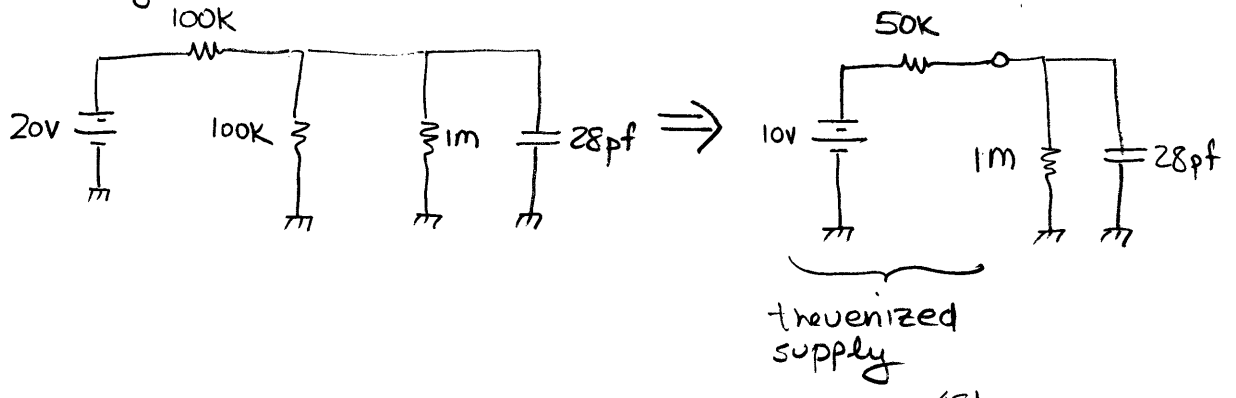
for $R_{IN} \ll R$ $V_o \to 0$

to calculate R_{IN}, you want $R_{IN} \cong R$

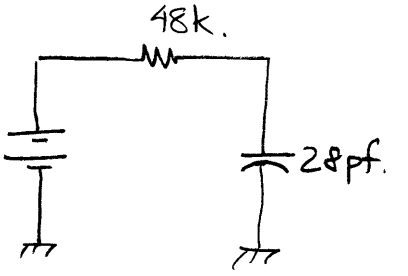
R_{IN} meter $\cong$ 10M

R_{IN} scope $\cong$ 1M $\quad C_{IN,scope} = 28pf$

Is C negligible?



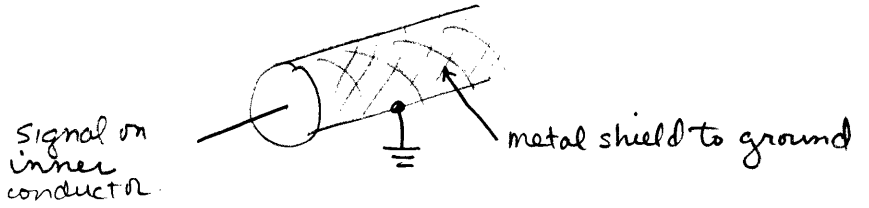
$\Rightarrow$ Thevenize again



$$f_{cutoff} = \frac{1}{2\pi RC} = \frac{1}{2\pi (48\times10^{3})(28\times10^{-12})} \cong$$

bare wires pick up a lot of noise because they act as antennas

coax is used to reduce noise

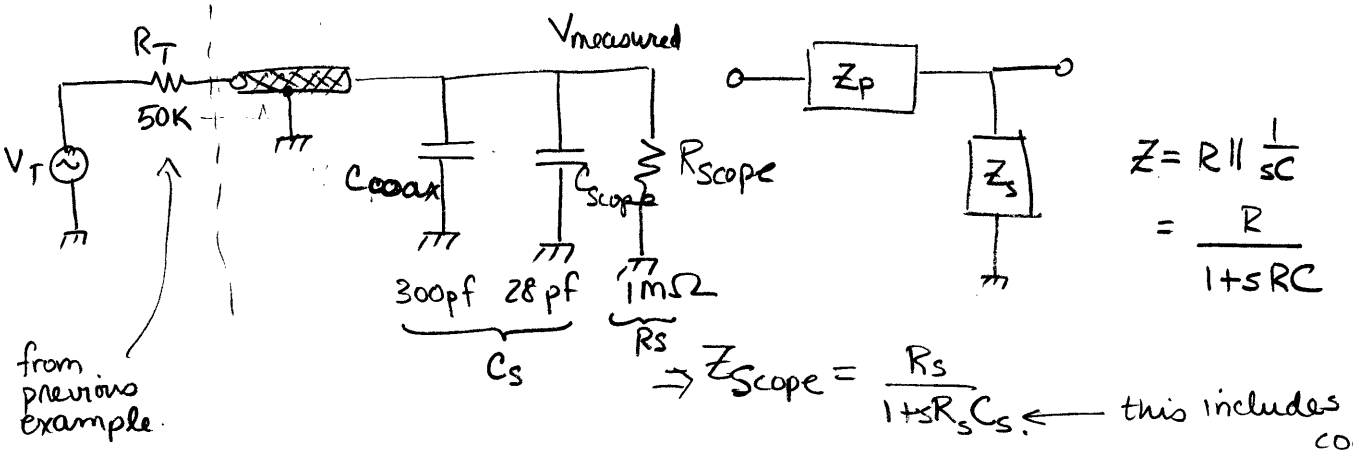


shield adds a lot of capacitance, possibly 50pf/foot.

a 6 foot length of cable is now 300 pf
+ 28 pf of scope.

$$f_{cutoff} = \frac{1}{2\pi(48\times10^3)(328\,pf)} \approx 10\,kHz,\ \text{not very useful.}$$

improve by compensating probe.



$$Z = R \parallel \frac{1}{sC} = \frac{R}{1+sRC}$$

$$\Rightarrow Z_{Scope} = \frac{R_s}{1+sR_sC_s}$$ ← this includes the coax.

$$\frac{V_{measured}}{V_T} = \frac{Z_{scope}}{R_T + Z_{scope}}$$

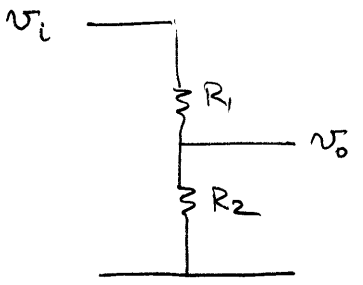
for the above conditions

$$\frac{V_{measured}}{V_T} \approx 0.95 \text{ at low frequencies}$$

$$f_{cutoff} = \frac{1}{2\pi RC} = \frac{1}{2\pi(1M \parallel 50K)(300+28\,pf)}$$

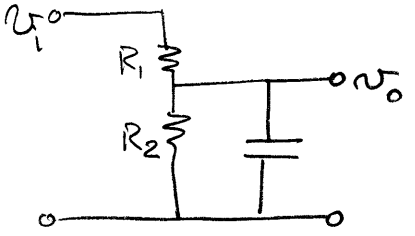
$$\cong 10.1\,kHz$$

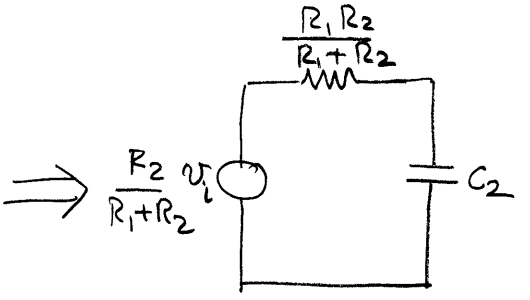
time domain analysis – Consider a simple attenuator



independent of f

in reality we have

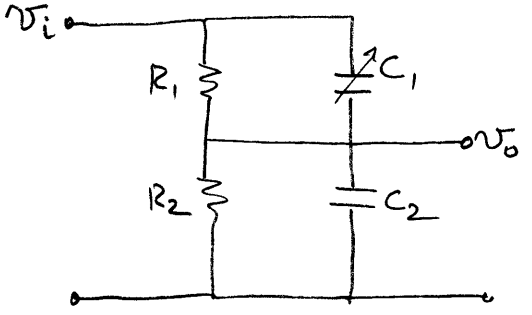




If $R_1 = R_2 = 1\,M$ and $C_2 = 15\,pF$.

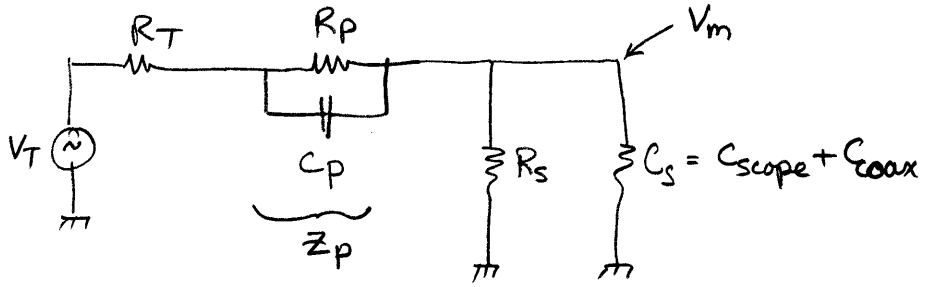
$$f_{cutoff} = \frac{1}{2\pi(500\times10^3)(15\times10^{-12})}$$

The way to extend the frequency response is to <u>compensate</u> the probe by bypassing it with a capacitance C_1



if $R_{f1} = R_{f2}$ the bridge will be balanced independant of frequency.

Now, what happens with probe



$$\frac{V_m}{V_T} = \frac{Z_s}{R_T + Z_s + Z_p} \quad \text{where} \quad Z_s = \frac{R_s}{1+sR_sC_s} \quad Z_p = \frac{R_p}{1+sR_pC_p}$$

$$= \frac{\frac{R_s}{1+sR_sC_s}}{R_T + \frac{R_p}{1+sR_pC_p} + \frac{R_s}{1+sR_sC_s}} \quad \text{multiply through by } \frac{1+sR_sC_s}{1+sR_sC_s}$$

$$= \frac{R_s}{R_T(1+sR_sC_s) + R_p\left(\frac{1+sR_sC_s}{1+sR_pC_p}\right) + R_s}$$

Now, consider what happens if $R_pC_p = R_sC_s$

$$\Rightarrow \frac{R_s}{R_T(1+sR_pC_p) + R_p + R_s}$$

$$= \underbrace{\frac{R_s}{R_s+R_p}}_{\text{voltage divider with no frequency dependence.}} \frac{R_s+R_p}{R_T(1+sR_pC_p) + R_p + R_s}$$

define $R_{eq} = R_s + R_p$

$$\frac{R_{eq}}{R_T(1+sR_pC_p) + R_{eq}}$$

but $R_pC_p = R_pC_p\frac{C_s+C_p}{C_s+C_p} = \frac{R_pC_sC_p + \overbrace{R_pC_pC_p}^{R_sC_s}}{C_s+C_p} = \frac{R_pC_sC_p + R_sC_sC_p}{C_s+C_p}$

$$= (R_s+R_p)\left(\frac{C_pC_s}{C_p+C_s}\right)$$

$\uparrow$ C_{eq}

$$\therefore \frac{V_{measured}}{V_T} = \underbrace{\frac{R_S}{R_S + R_p}}_{\text{division factor.}} \underbrace{\frac{R_{eq}}{R_T(1 + s R_{eq} C_{eq}) + R_{eq}}}_{H(s)\text{ frequency response factor}}$$

Suppose we set $R_p = 99\,M\Omega$

then $C_p = \frac{R_S C_S}{R_p} = \frac{1m\,(328\,pf)}{99m} = 3.31\,pf$

$$\therefore \frac{V_{measured}}{V_{in}} = \frac{1}{1+99} = \frac{1}{100}$$

$R_{eq} = R_S + R_p = 1m + 99m$

$C_{eq} = \frac{C_S C_p}{C_S + C_p} = \frac{(328)(3.31)}{328 + 3.31}$

$= 3.28\,pf.$

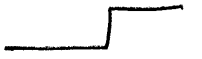
$$H(s) = \frac{R_{eq}}{R_T + s R_T R_{eq} C_{eq} + R_{eq}} = \frac{\frac{1}{R_T + R_{eq}}}{1 + s\frac{R_T R_{eq}}{R_T + R_{eq}} C_{eq}}$$

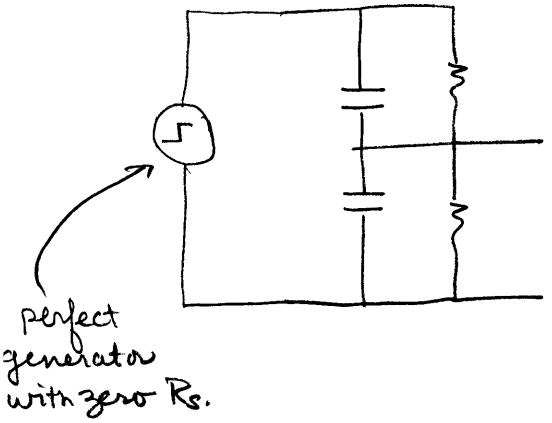
$$= \frac{R_{eq}/R_T + R_{eq}}{1 + s\left(\frac{R_T R_{eq}}{R_T + R_{eq}}\right) C_{eq}}$$

$$H(0) \rightarrow \frac{R_{eq}}{R_T + R_{eq}} = \frac{100M}{48K + 100M} \cong .9995$$

$$f_{cutoff} = \frac{1}{2\pi\left(\frac{R_T R_{eq}}{R_T + R_{eq}}\right) C_{eq}} \cong \frac{1}{2\pi\,(48K)(3.28pf)} \approx 970\,kHz.$$

Which is actually better than scope with no coax.

Consider the response to a unit step in voltage, 



by Kirchoff's Law $V = \frac{q}{C_1} + \frac{q}{C_2} = \frac{C_1+C_2}{C_1C_2} q.$

at $t = 0^+$

$$v_o(0^+) = \frac{q}{C_2} = \frac{\frac{C_1C_2}{C_1+C_2} V}{C_2} = \frac{C_1}{C_1+C_2} V$$

∴ the initial output voltage is determined by the capacitors.

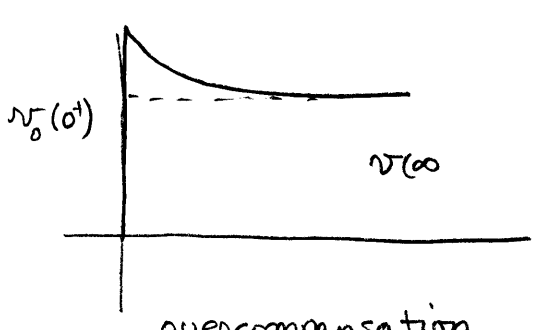
the final output voltage will be determined by the resistors

$$v_o(\infty) = \frac{R_2}{R_1+R_2} V$$

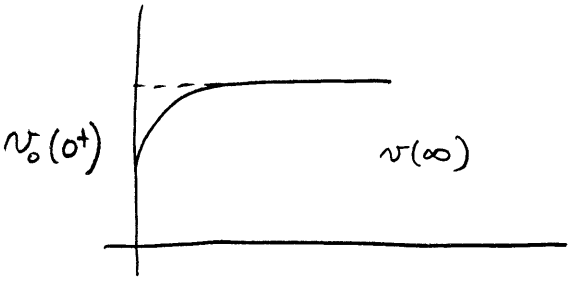
For the circuit to be compensated $v_o(0^+) = v(\infty)$ or any other time in between. Then

$$\frac{C_1}{C_1+C_2} V = \frac{R_2}{R_1+R_2} V \quad \text{or} \quad C_1R_1 + C_1R_2 = C_1R_2 + C_2R_2$$

$$\text{or} \quad R_1C_1 = R_2C_2.$$

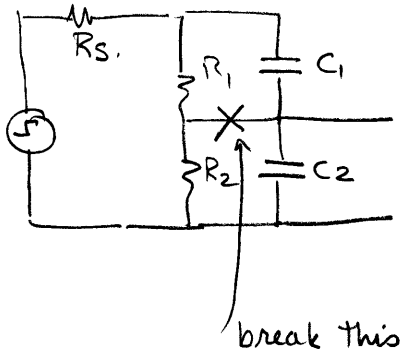


overcompensation

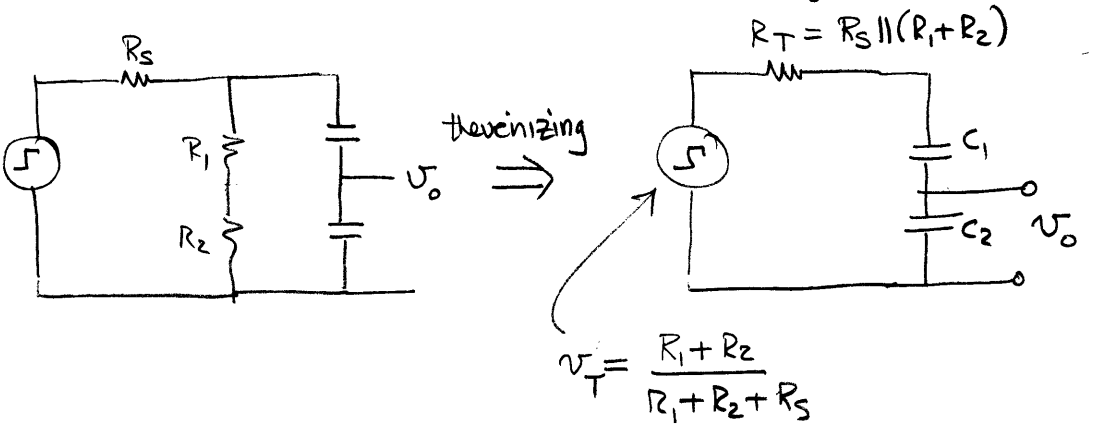


undercompensation

If we include the source impedance R_S we get.



break this connection for the moment since the capacitors alone determine $v_o(0^+)$ and the resistors alone determine $v_o(\infty)$



If $R_S \ll (R_1+R_2)$ <u>usually true</u> then the input waveform will have a time constant $\tau \cong R_S C'$ where $C' = \dfrac{C_1 C_2}{C_1+C_2}$.

If the input were directly connected to the output, i.e. the input of the scope the time constant would be

$$\tau' \cong R_S C_2 \quad \text{connected straight through.}$$

so, the improvement in rise-time is $\dfrac{\tau'}{\tau}$ (direct / probe) $= \dfrac{R_S C_2}{R_S C'} = \dfrac{C_2(C_1+C_2)}{C_1 C_2}$

$$= \frac{C_1+C_2}{C_1} > 1$$

$\therefore$ probe decreases timeconstant

However, this is at the expense of signal level since

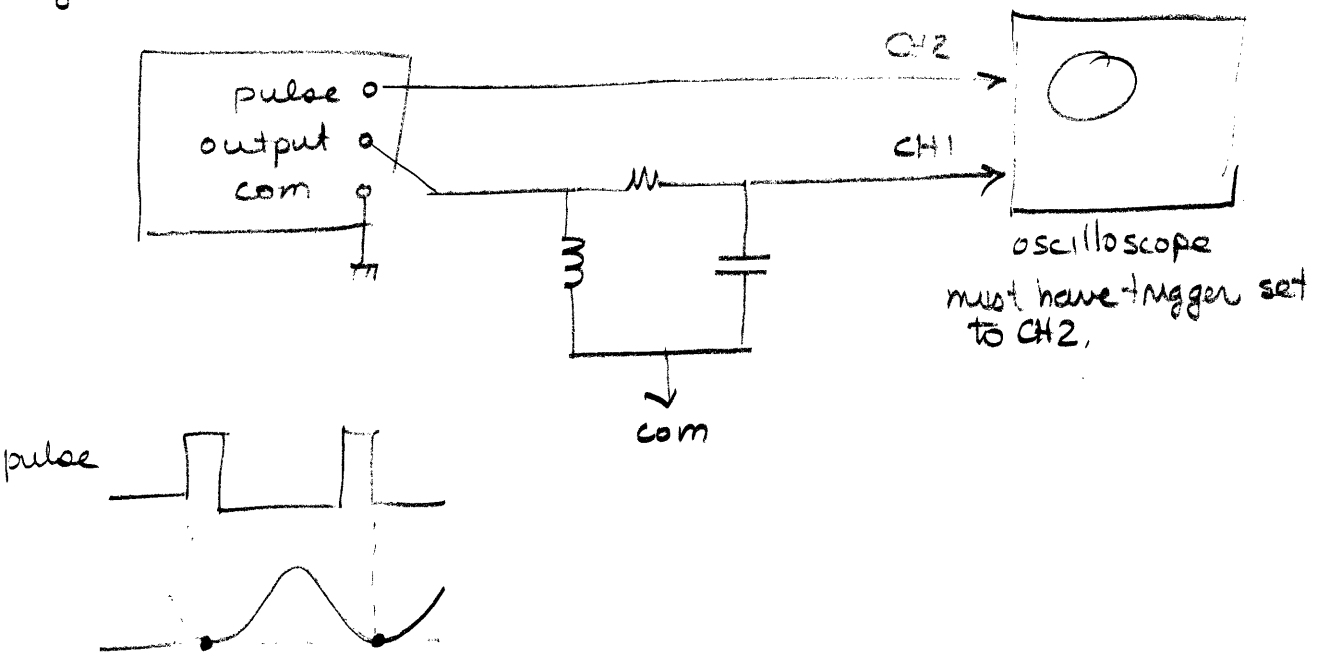
$$\frac{v'(\infty)}{v(\infty)} = \frac{\dfrac{R_2}{R_S+R_2}}{\dfrac{R_2}{R_1+R_2+R_S}} = \frac{R_1+R_2+R_S}{R_2+R_S} \approx \frac{R_1+R_2}{R_2}$$

$\therefore$ probe decreases signal by $\dfrac{R_2}{R_1+R_2}$.

Boylestad & Nashelsky – Electronic Design & Circuit Theory

diodes	74
power diodes	92
zener diodes	74-82

Figure 4.1

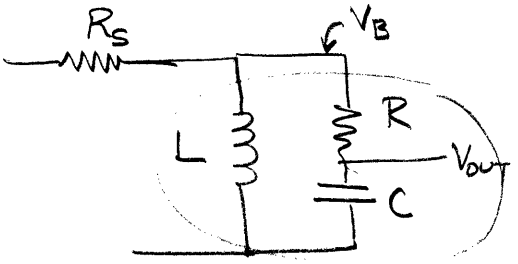


can set your scope to get 8 divisions across using variable adjust on time base

$$\frac{360}{8} = \frac{45^\circ}{\text{div.}}$$

use DMM to measure series L of inductor !

don't do part 2.



$$Z_{11} = j\omega L \,||\, \left(R + \frac{1}{j\omega C}\right) = \frac{(j\omega L)\left(R + \frac{1}{j\omega C}\right)}{R + j\omega L + \frac{1}{j\omega C}}$$

$$\frac{V_B}{V_S} = \frac{Z_{11}}{Z_{11} + R_S} = \frac{(j\omega L)\left(R + \frac{1}{j\omega C}\right)\frac{1}{R + j\omega L + \frac{1}{j\omega C}}}{(j\omega L)\left(R + \frac{1}{j\omega C}\right)\frac{1}{R + j\omega L + \frac{1}{j\omega C}} + R_S}$$

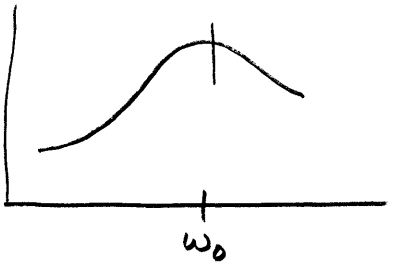
$$= \frac{(j\omega L)\left(R + \frac{1}{j\omega C}\right)}{(j\omega L)\left(R + \frac{1}{j\omega C}\right) + R_S\left(R + j\omega L + \frac{1}{j\omega C}\right)}$$

$$\frac{V_{OUT}}{V_S} = \frac{(j\omega L)\left(R + \frac{1}{j\omega C}\right)}{(j\omega L)\left(R + \frac{1}{j\omega C}\right) + R_S\left(R + j\omega L + \frac{1}{j\omega C}\right)} \left(\frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + R}\right)$$

$$= \frac{\frac{\omega L}{\omega C}}{R_S R + \frac{j\omega L}{j\omega C} + R j\omega L + R_S j\omega L + \frac{R_S}{j\omega C}}$$

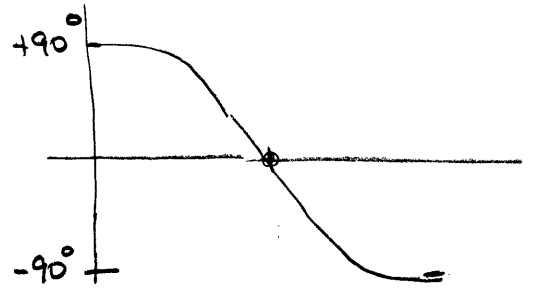
$$= \frac{L/C}{R_S R + \frac{L}{C} + j\left(R\omega L + R_S \omega L - \frac{R_S}{\omega C}\right)}$$

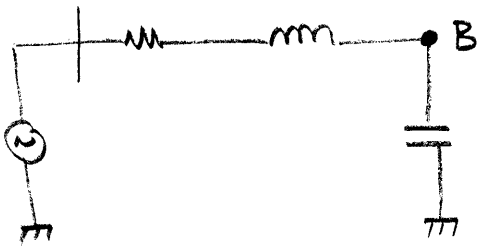
$\left|\frac{V_{OUT}}{V_S}\right|$



$\angle \frac{V_{OUT}}{V_S}$

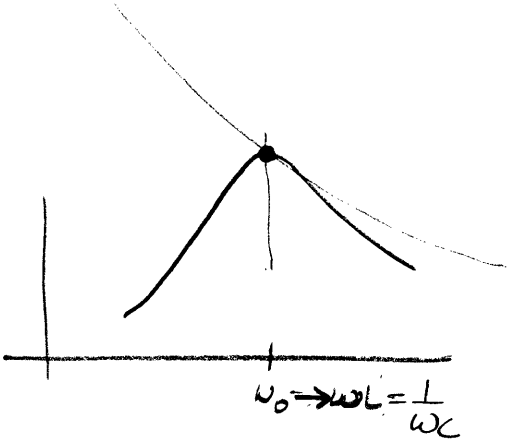
$\angle 0 - \angle +90$





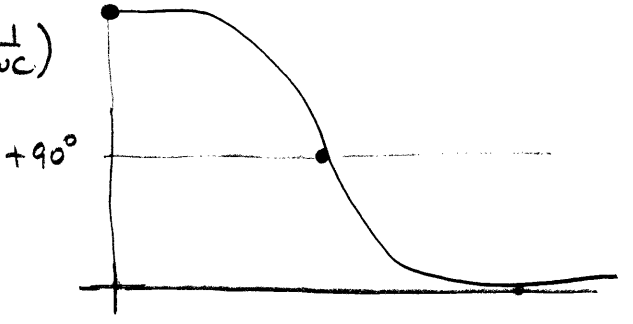
$$\frac{V_B}{V_S} = \frac{\frac{1}{j\omega C}}{R_S + j\omega L + \frac{1}{j\omega C}}$$

$$\left|\frac{V_B}{V_S}\right| = \frac{\left|\frac{1}{j\omega C}\right|}{\left|R_S + j\left(\omega L - \frac{1}{\omega C}\right)\right|}$$



$$\angle \frac{V_B}{V_S} = \angle \frac{1}{j\omega C} - \angle R_S + j\left(\omega L - \frac{1}{\omega C}\right)$$

$+90°$



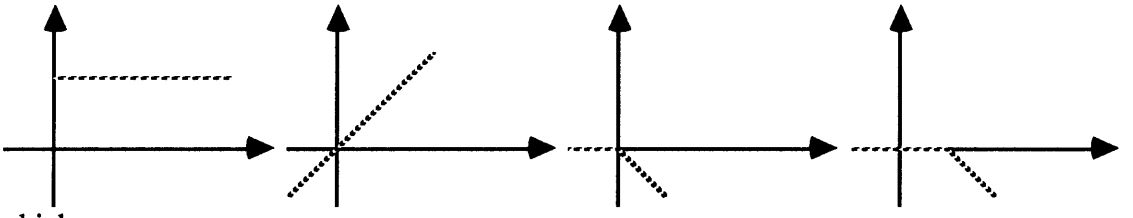
Given that

$$H(s) = \frac{10s}{(1+s)(1+\frac{s}{10})}$$

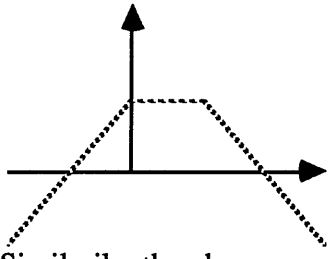
plot $|H(j\omega)|$ and $\angle H(j\omega)$

Solution:

$$20 \log_{10}|H(j\omega)| = 20 \log_{10}(10) + 20 \log_{10}|\omega| - 20 \log_{10}|1+j\omega| - 20 \log_{10}|1+\frac{j\omega}{10}|$$



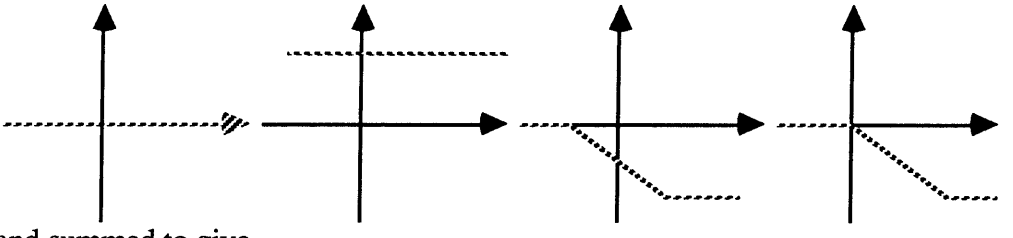
which sum up to



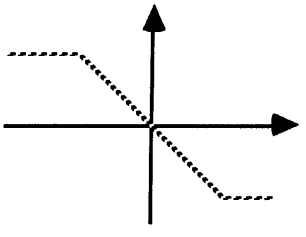
Similarily, the phases are

$$\angle H(j\omega) = \angle 10 + \angle j\omega - \angle(1+j\omega) - \angle(1+\frac{j\omega}{10})$$

which can be graphically represented as

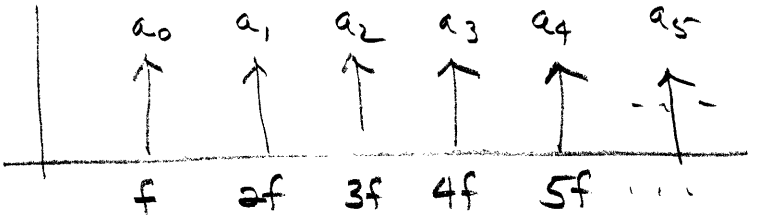


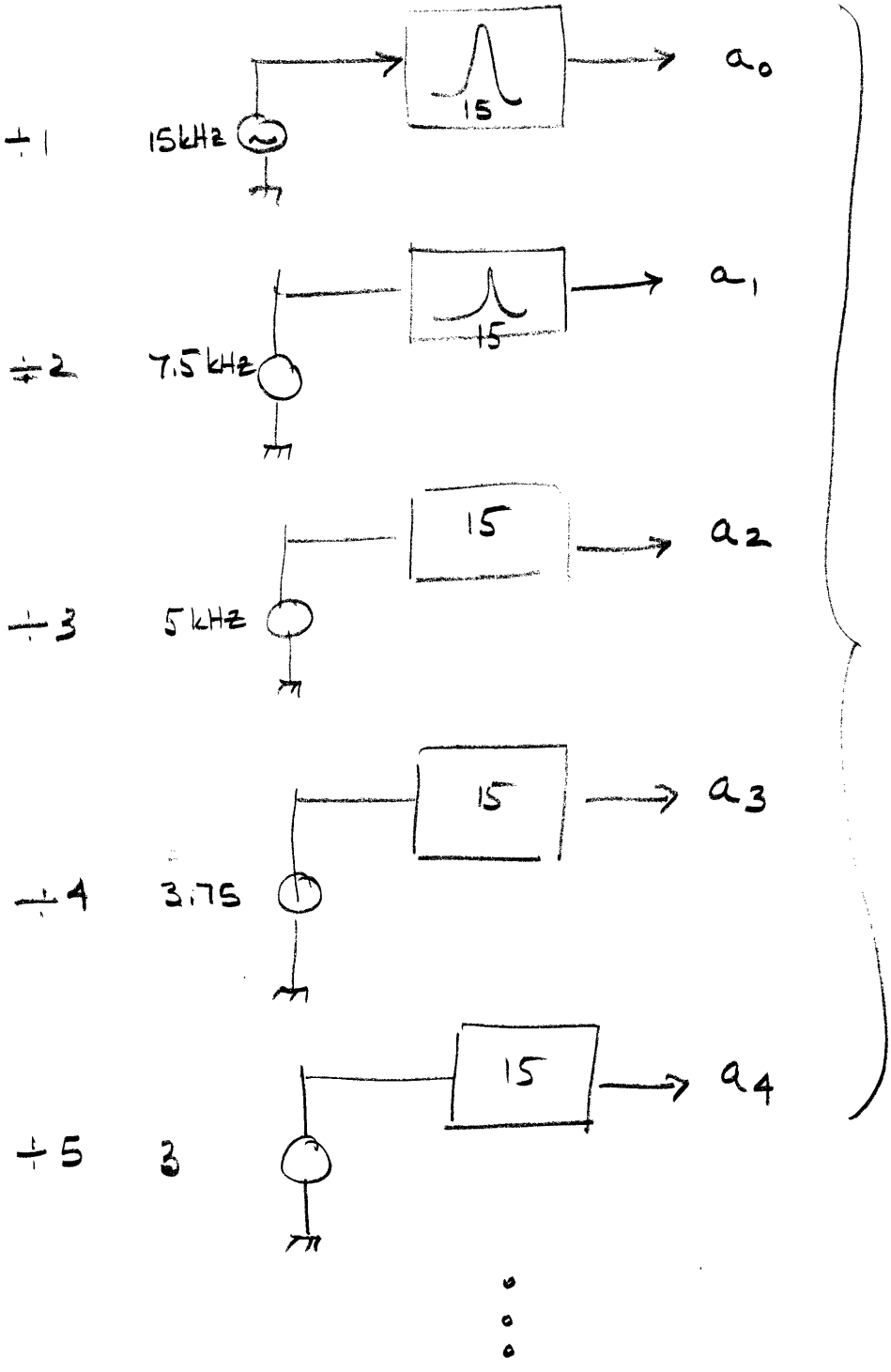
and summed to give



Fourier Analysis

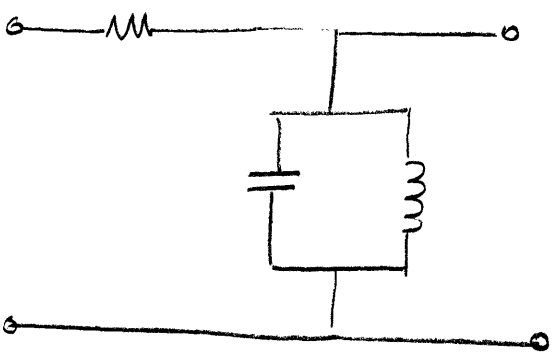
periodic signals





doesn't give phase just magnitude

Part 3 resonance.

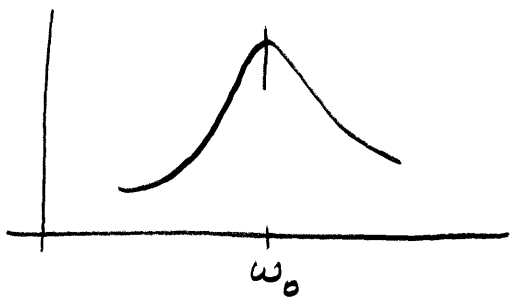


$$Z_{11} = \frac{1}{j\omega C} \,||\, j\omega L = \frac{j\omega C \frac{1}{j\omega L}}{\frac{1}{j\omega C} + j\omega L} = \frac{C/L}{j\left(\omega L - \frac{1}{\omega C}\right)}$$

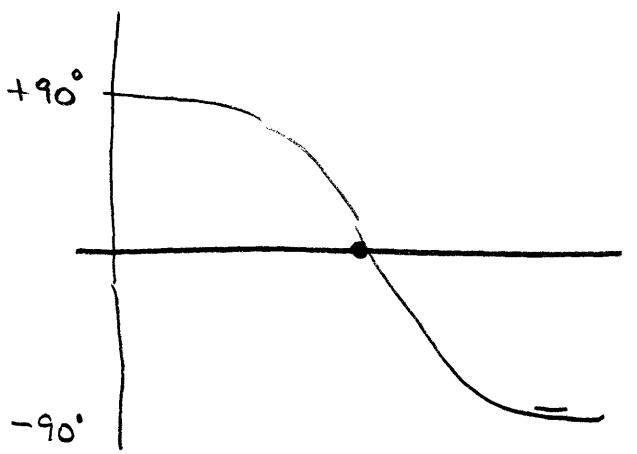
$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{11}}{Z_{11} + R} = \frac{C/L \frac{1}{j\left(\omega L - \frac{1}{\omega C}\right)}}{C/L \frac{1}{j\left(\omega L - \frac{1}{\omega C}\right)} + R}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{C/L}{C/L + Rj\left(\omega L - \frac{1}{\omega C}\right)} = \frac{C/LR}{C/LR + j\left(\omega L - \frac{1}{\omega C}\right)}$$

$\left|\frac{V_{OUT}}{V_{IN}}\right|$

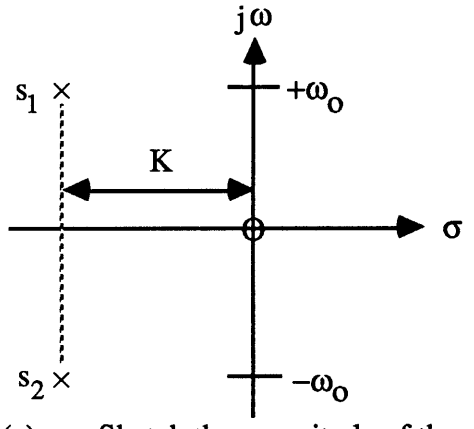


$\angle \frac{V_{OUT}}{V_{IN}}$



measure L, RC using digital LRC meter

A system has the pole-zero diagram shown below.



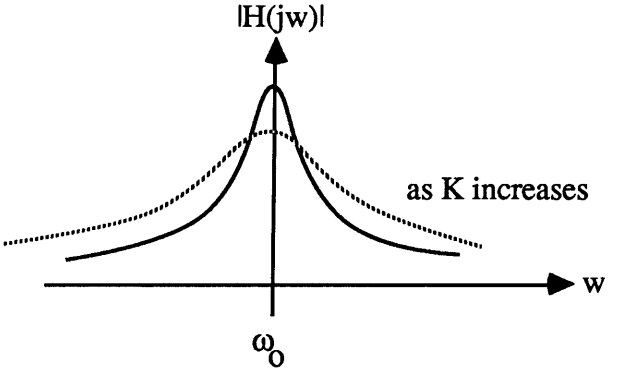
(a) Sketch the magnitude of the system frequency response for K very small, i.e. near the jω axis.

(b) Indicate what happens to your answer for (a) as K becomes larger, i.e. the poles move away from the jω axis.

Solution:

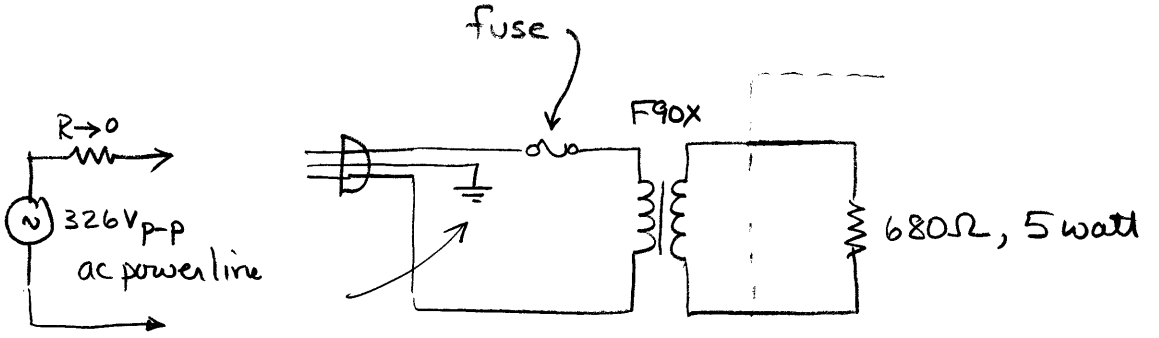
(a)

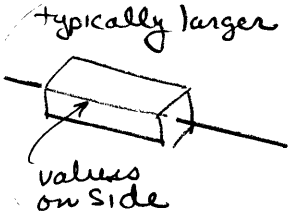
$$H(j\omega) \approx K\frac{j\omega-0}{(j\omega-s_1)(j\omega-s_2)} \rightarrow K\frac{\omega}{(\omega_o+\omega)(\omega_o-\omega)} = K\frac{\omega}{\omega_o^2-\omega^2}$$



(b) as K increases the peak diminishes and broadens

real transformers





can deliver hundreds of amperes

Triad F90X

Secondary 10-20CT-40CT@100mA

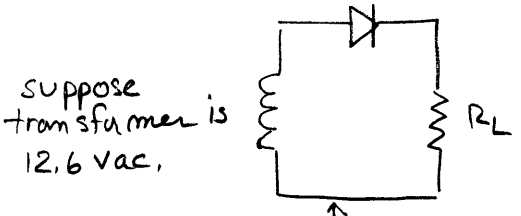
dc voltage | half-wave | bridge

typically only specified as rms ac voltage for a given secondary current.

→ what is color code?

- RED
- YELLOW (CT)
- GREEN
-
-

half-wave rectifier



$$\text{average value} = \frac{1}{\pi}\int_0^{T} \sin t\, dt$$

over one half cycle

$$= \frac{1}{\pi}$$

$$\therefore V_{dc} = \frac{\sqrt{2}}{\pi}\, 12.6$$

$$\approx 5.66 \text{ volts}$$

peak secondary voltage is $\sqrt{2}\ 12.6 = 17.8$ volts

diode characteristics

max. current diode can handle

I_{dc} = average load current = $\frac{V_{DC}}{R_L}$ (usually listed as I_o on datasheet)

IN4001 has an I_o of 1A.

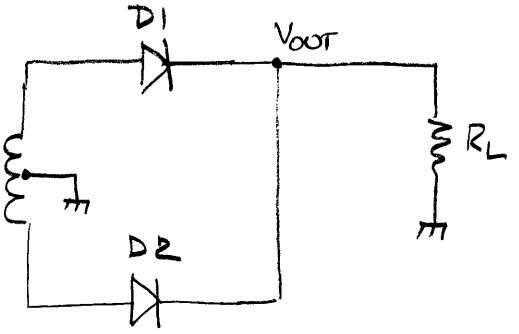
If $R_L = 10\Omega$ in above bridge rectifier, $I_{dc} = \frac{5.66}{10\Omega} \approx 0.56$ A which is Ok

Sections 1.25 – 1.28 in Horowitz

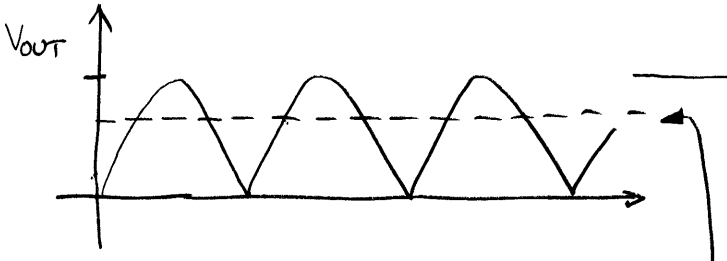
on negative half cycle diode is off and must withstand the peak voltage without conducting current.

maximum reverse voltage is called PIV or PRV.

Full-wave rectifier



When D1 is on, D2 is off and vice verse.



——— $= \frac{1}{2} V_{peak}$ (due to center tap)

$\frac{\sqrt{2}}{2}(12.6) \approx 8.91$ volts.

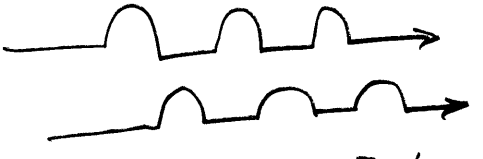
dc is now $\frac{2}{\pi} V_{peak}$ since twice as much dc to average.

$\frac{2}{\pi}\left(\frac{\sqrt{2}\cdot 12.6}{2}\right) = 5.67$ volts.

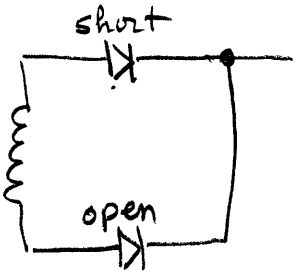
(peak across each diode is only $\frac{1}{2}$ as much)

if $R_L = 10\Omega$ as before $I_{dc} = \frac{5.67}{10\Omega} = 0.567A$

but each diode need only be $\frac{1}{2}$ this since each diode's current looks like



how about PIV of each diode $PIV = \sqrt{2}(12.6)$

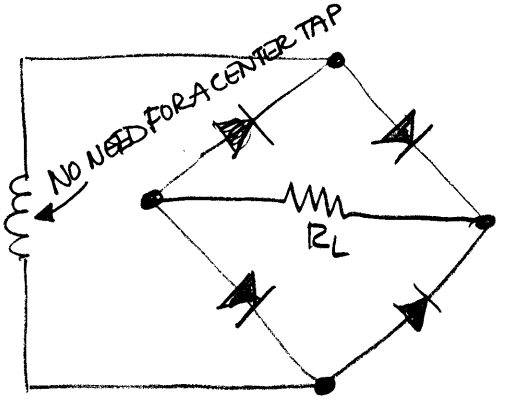


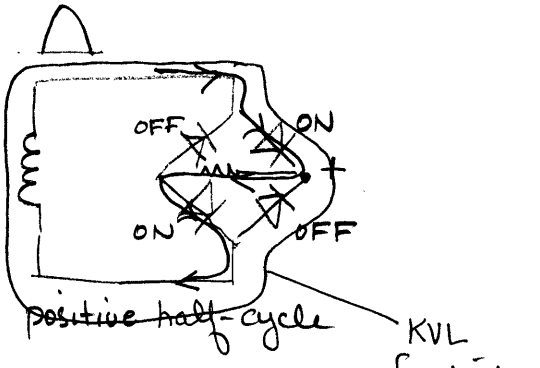
apply KVL around this loop!

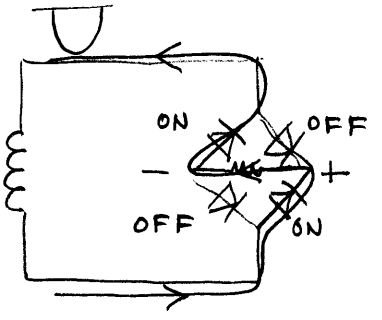
most popular rectifier circuit — bridge rectifier

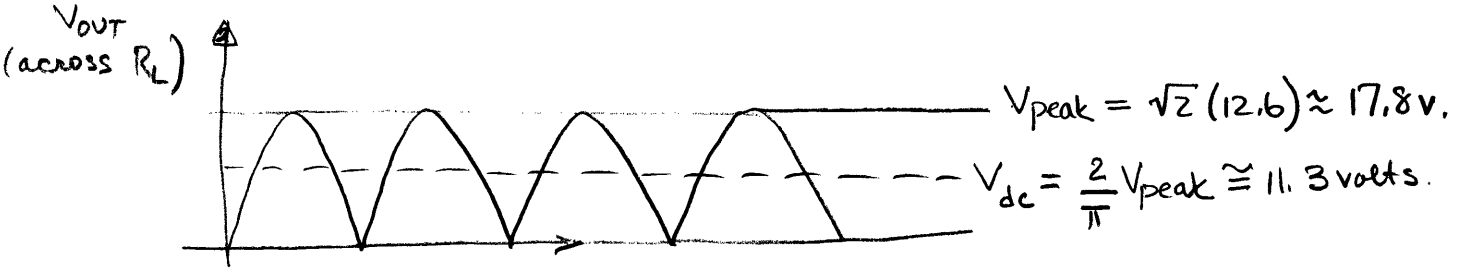
full peak voltage of half-wave rectifier

higher average value of full wave.









If $R_L = 10\Omega$ $\quad I_{dc} = \dfrac{11.3 \text{ volts}}{10\Omega} = 1.13$ A.

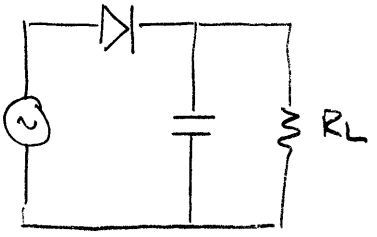
but <u>each</u> diode only conducts $\frac{1}{2}$ cycle so its ratings drop to $\frac{1.13}{2}$ A.

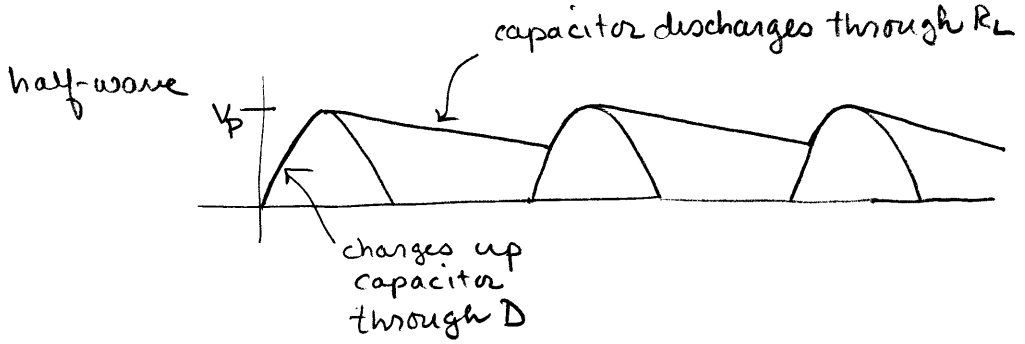
use KVL around loop shown above

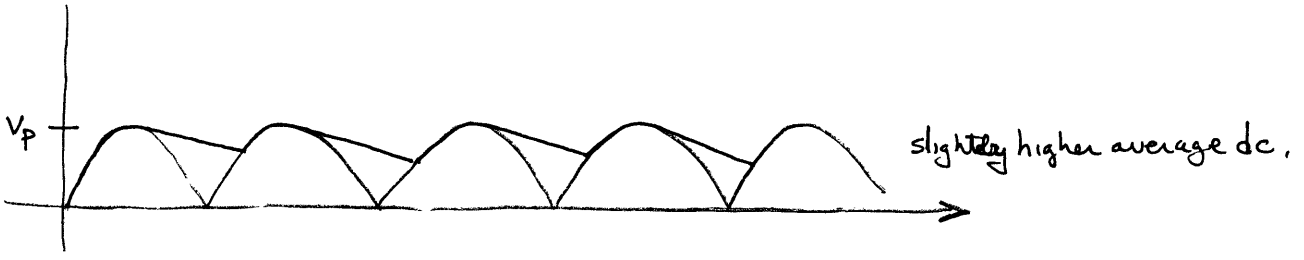
$$V_{peak} - PIV - 0 = 0$$

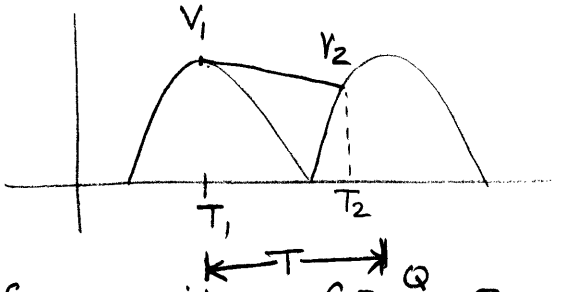
$$\therefore \quad PIV = V_{peak}.$$

capacitor input filter









for a capacitor $C = \frac{Q}{V}$ or $V = \frac{Q}{C}$.

from the graph $V_{ripple} = V_1 - V_2 = \frac{Q_1}{C} - \frac{Q_2}{C} = \frac{Q_1 - Q_2}{C}$

C does not change

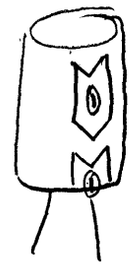
Now: $\frac{V_1 - V_2}{T_1 - T_2} = \frac{1}{C}\frac{Q_1 - Q_2}{T_1 - T_2}$

if $R_L C$ is very large $T_1 - T_2 \approx T$, the period of the ripple.

$$\frac{V_1 - V_2}{T} = \frac{1}{C}\frac{Q_1 - Q_2}{T} = \frac{1}{C} I$$

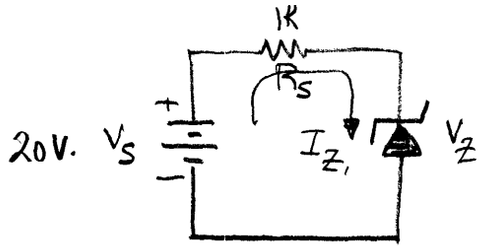
$$\therefore V_{ripple} = V_1 - V_2 \cong \frac{I}{C} I = \frac{I}{fC}$$

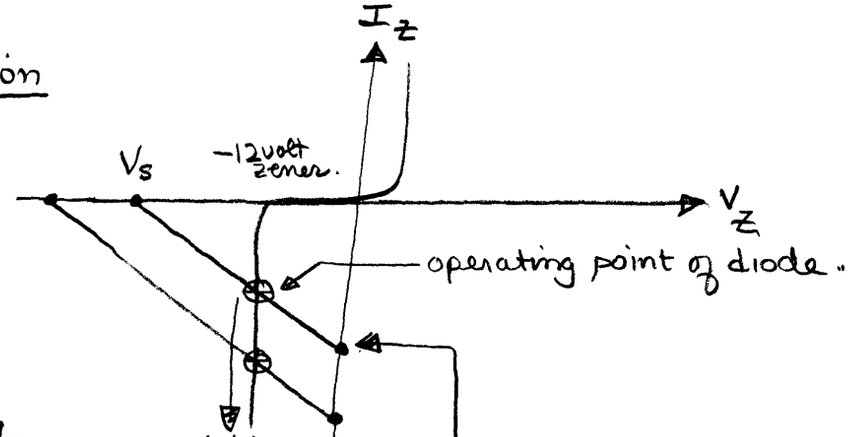
capacitors



capacitors can explode if polarity is reversed!

Zener diode regulation



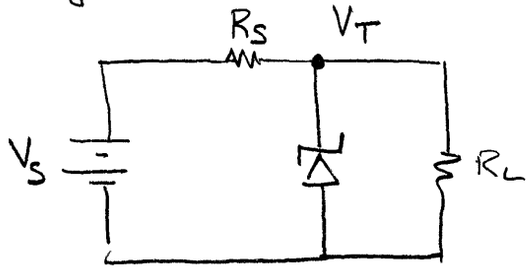


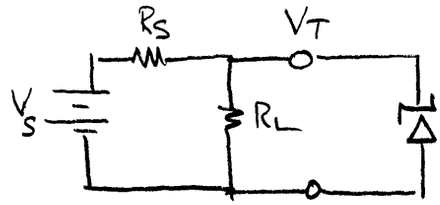
(equals I_Z) $I_S = \dfrac{V_S - V_Z}{R_S}$ (negative as drawn).

if $V_Z = 0$ $I = \dfrac{V_S}{R_S}$

if $I_Z = 0$ $V_Z = V_S$

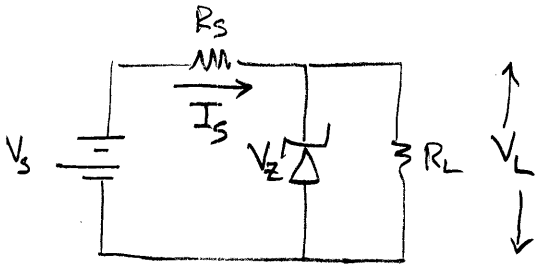
Zener regulator.





$V_T = \dfrac{R_L}{R_S + R_L} V_S$

$R_T = R_S \parallel R_L$.



assume diode is working.
(broken down)

R_S is for current limiting

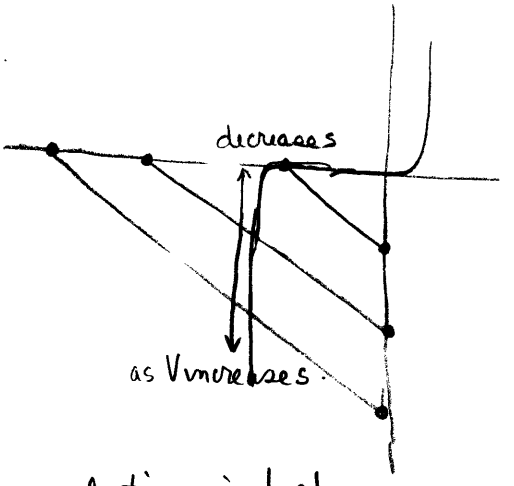
$$I_S = \frac{V_S - V_Z}{R_S}$$

$$I_L \approx \frac{V_Z}{R_L}.$$

$$\therefore \quad I_Z = I_S - I_L$$

Zener dropout point

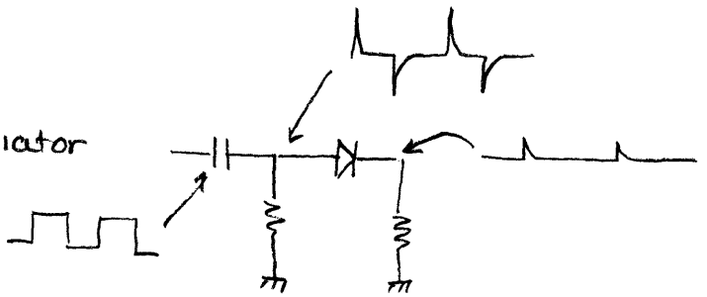
(see section 2.04 of Horowitz)



whenever $I_Z \to 0$ regulation is lost.

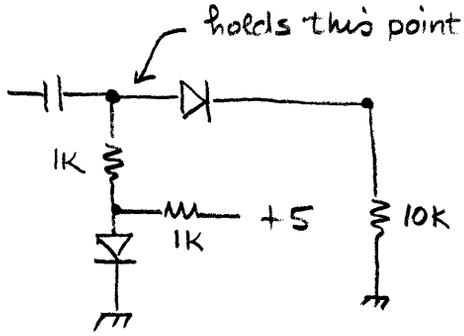
1.30 diode clamps

rectifying differentiator

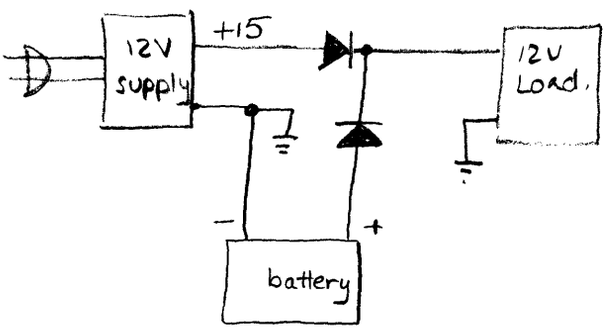


has a 0.6 volt loss !

bias diode

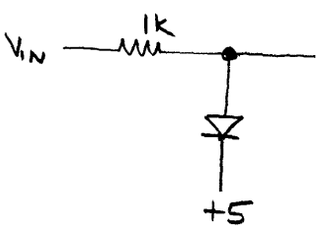


diode switching.

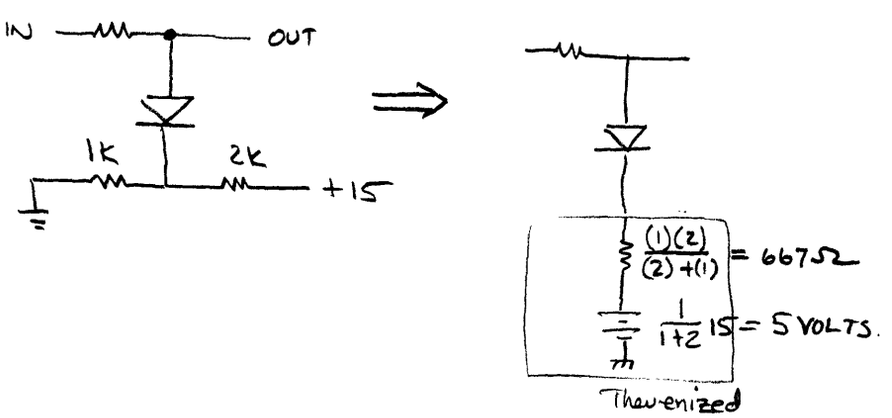


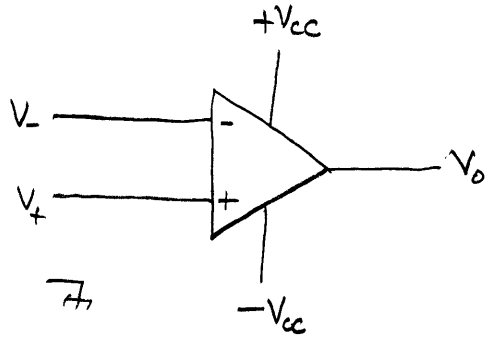
diode clamps.

standard for all cmos circuits



if $V_{IN} > 5.0 + 0.7$ volts output saturates at 5.7 volts.





most op-amps require + and − power supplies

$$V_{OUT} = A(V_+ - V_-)$$

or $$\frac{V_o}{A} = V_+ - V_-$$

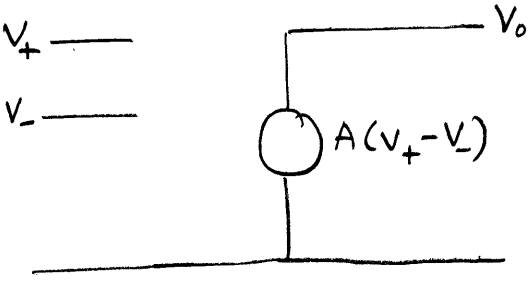
normal assumptions

these are related to Horowitz's golden rules.

$A \rightarrow \infty$

$I_{os} \rightarrow 0$

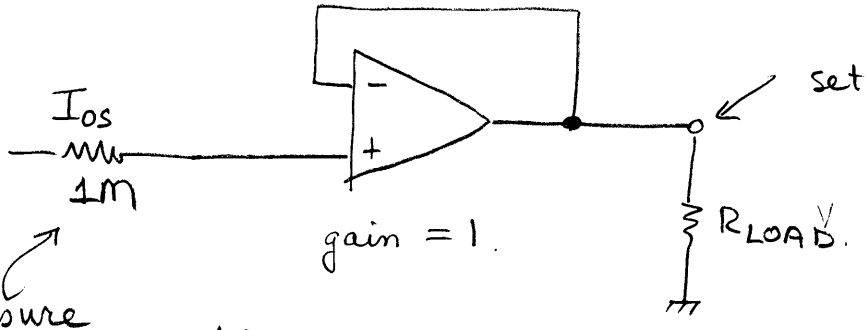
$V_{os} \rightarrow 0$



Analyzed in 3.04 Horowitz

<u>with unity feedback</u>

unity gain voltage follower



measure dc drop across 1M resistor

if $I_L = \frac{V_o}{R_L}$ is not large

the output voltage = V_+

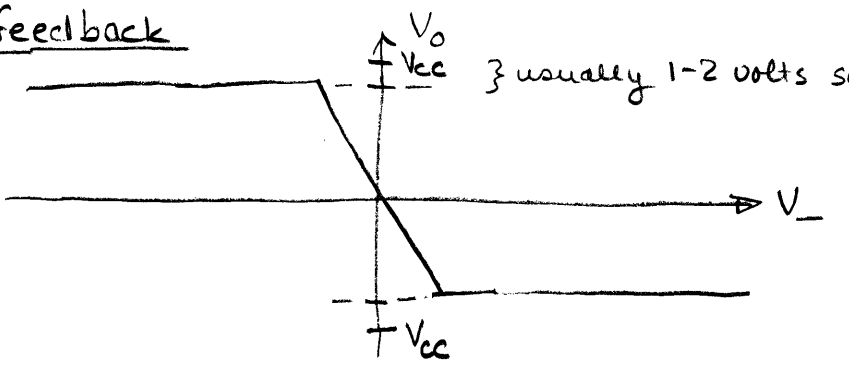
$$V_{OUT} = A(V_+ - V_-) \quad \text{but } V_- = V_{OUT}$$

$$V_{OUT} = A(V_+ - V_{OUT})$$

$$V_{OUT} + A V_{OUT} = A V_+$$

$$\frac{V_{OUT}}{V_+} = \frac{1+A}{A} \approx 1 \quad \text{if } A \text{ is large.}$$

without feedback



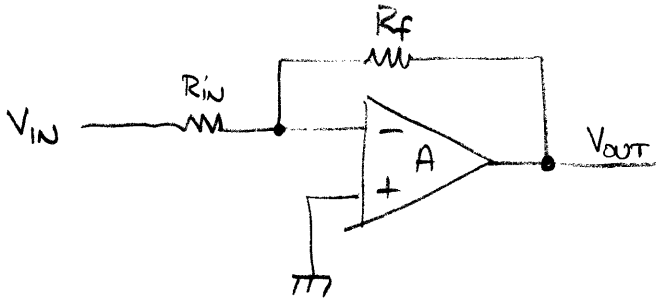
} usually 1-2 volts saturation difference

ΔV_{in} linear region may be only a few milli volts.

if $A = 10^5$ and $V_{OUT} = 30$ VOLTS

then $\Delta V_{IN} = \frac{30}{100 \times 10^3} = 0.3$ mV (and usually less)

with feedback



in this circuit

$$V_{OUT} = A(V_+ - V_-)$$

, using superposition

$$V_- = \frac{R_{IN}}{R_{IN}+R_f} V_{OUT} + \frac{R_f}{R_{IN}+R_f} V_{IN}$$

$$\therefore \quad V_- = \frac{R_{IN} V_{OUT} + R_f V_{IN}}{R_{IN} + R_f}$$

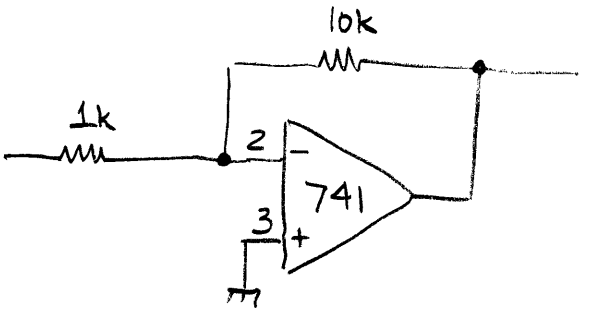
but $V_{OUT} = A(V_+ - V_-) = -AV_-$ since $V_+ = 0$

$$\frac{V_{OUT}}{-A} = \frac{R_{IN}}{R_{IN}+R_f} V_{OUT} + \frac{R_f V_{IN}}{R_{IN}+R_f}$$

$$\therefore \quad V_{OUT}\left(-\frac{1}{A} - \frac{R_{IN}}{R_{IN}+R_f}\right) = \frac{R_f}{R_{IN}+R_f} V_{IN}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A R_f}{(R_{IN}+R_f) + R_{IN} A} \rightarrow -\frac{R_f}{R_{IN}}$$

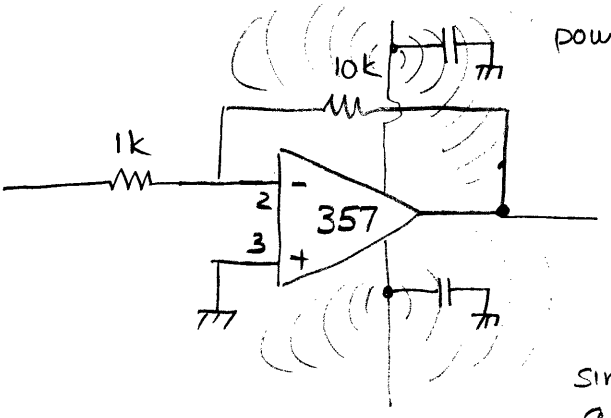
Figure 2:



AC: $2V_{p-p}$
DC: 0

AC: 20 V_{p-p}
DC: 0 (supposedly).

Figure 3:



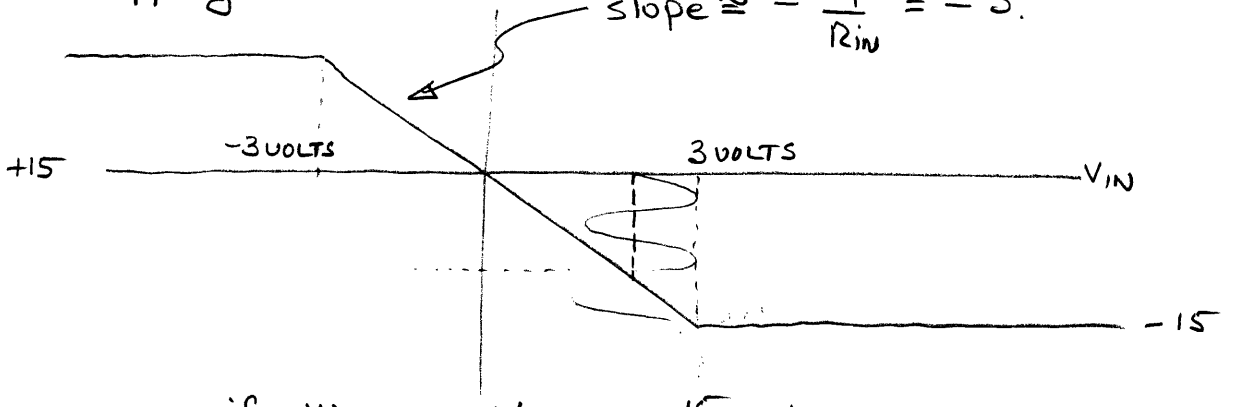
power lines radiate

unstable w/o decoupling capacitors. for LF357 due to large input impedance

simply want an ac short to ground.

3.08 precautions with op-amps

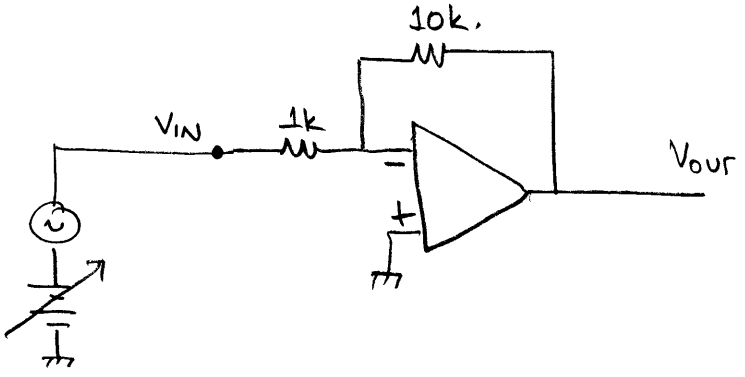
clipping



if $V_{IN} = +10$ $V_{OUT} = -15$, etc.

suppose $V_{IN} = 2V\,DC + 1V \cos \omega t$. OK

but if either ac or dc component increases clipping occurs.



① Vary V_{DC} to see V_{OUT}

② set $V_{DC} = 0$ increase V_{AC} to see what happens.

③ record for $V_{IN} = 5V$ p-p.

problems with real op-amps

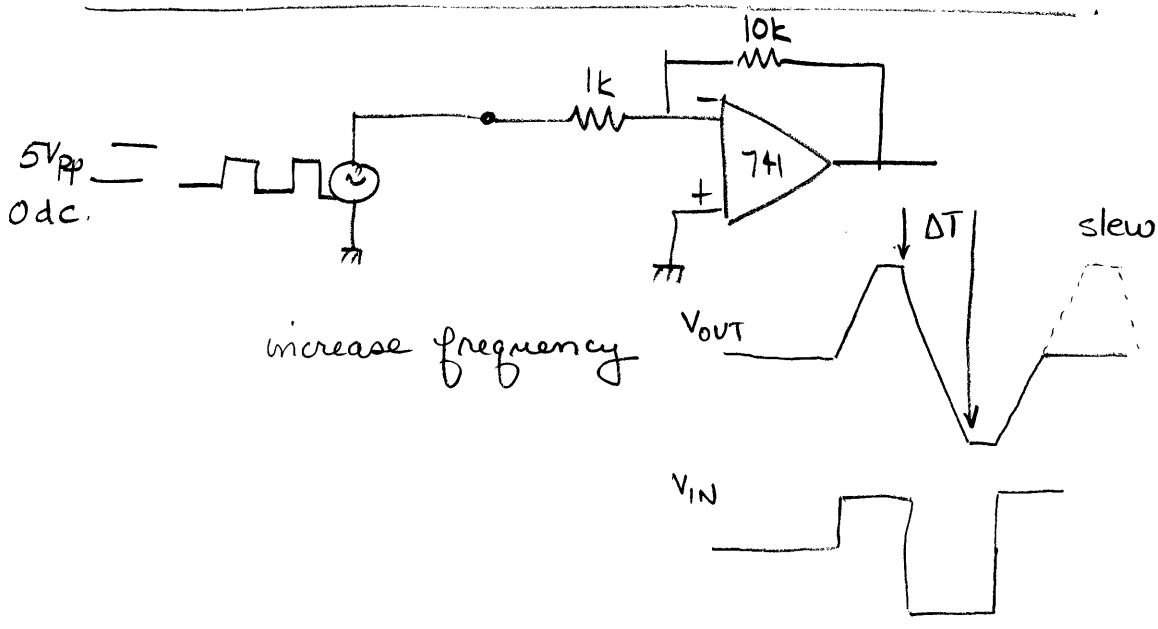
p.113 1. $I_{os} \neq 0$ already saw this

p.107 2. finite slew rate $\left|\frac{dV}{dt}\right| <$ constant

p.107 3. finite GBW

p.112. 4. $V_{os} \neq 0$

slew rate p. 107.



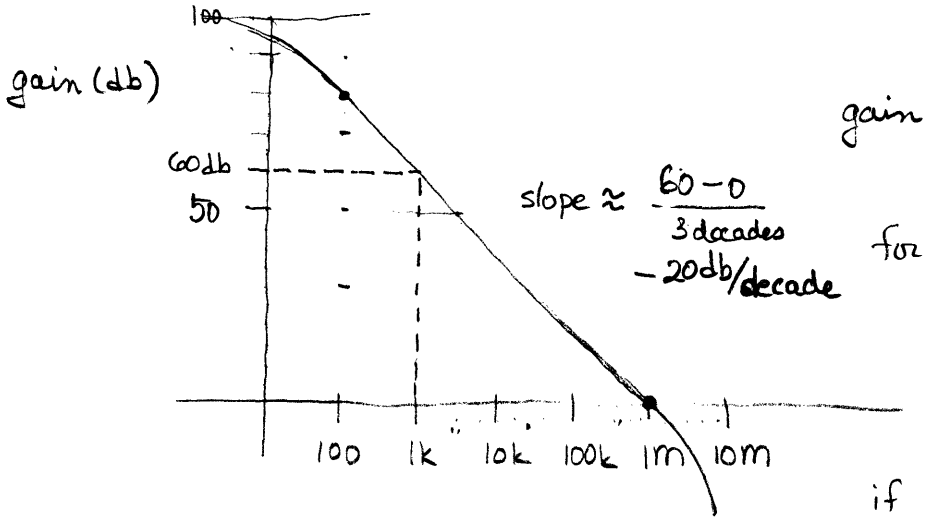
Interesting problems with real op-amps

1. $V_{os} \neq 0$
2. $I_{os} \neq 0$ ← already saw this.
3. finite GBW
4. finite slew rate

finite GBW

p. 107

mc1741 data sheet.



$$\text{slope} \approx \frac{60-0}{3 \text{ decades}} = -20 \text{db/decade}$$

$$\text{gain}_{db} = 20 \log_{10}\left(\frac{V_{OUT}}{V_{IN}}\right)$$

for example. x1000 gain

$$G. = 20 \log_{10}(10^3) = 60 \text{ db.}$$

→ about 1kHz BW.

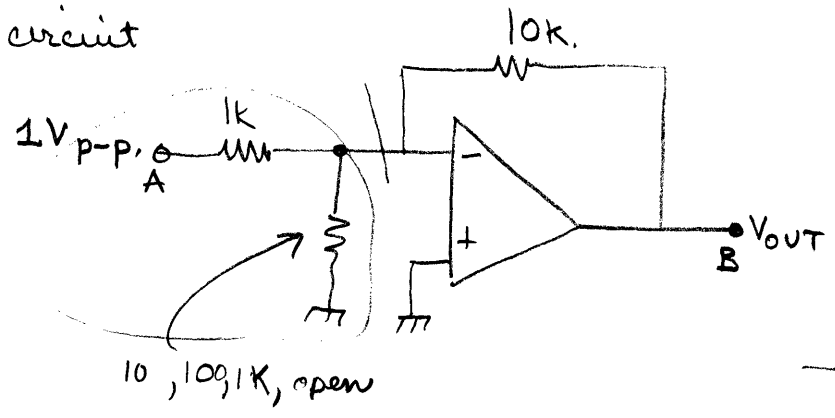
if G = 40 db (x100 gain)

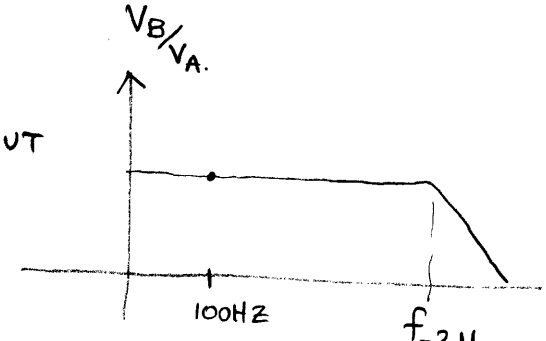
→ about 10kHz BW

G = 20 db (x10)

→ about 100kHz BW.

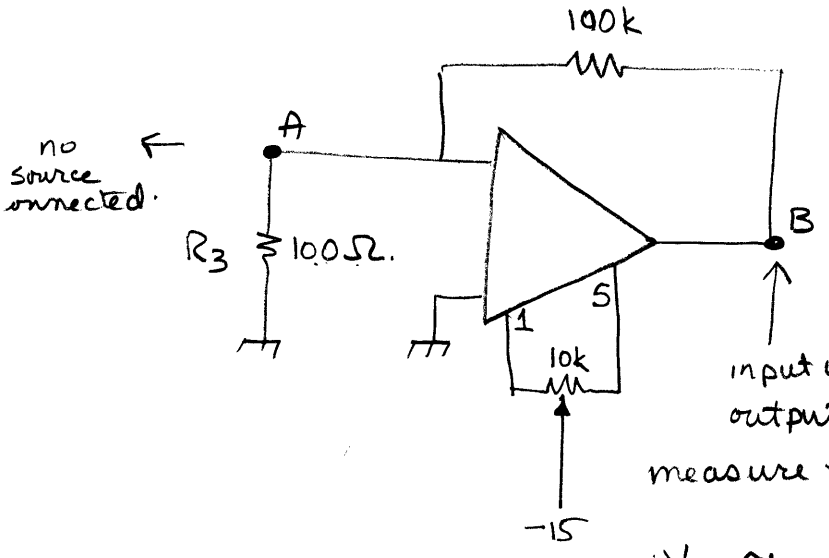
circuit





find this for 10, 100, 1k, open for LM741 and LF357

Thevenize input:



$$\text{gain} = \frac{100\,k}{0.1\,k} = 1000$$

input is zero
output ≠ 0.

measure for both LM741 and LF357

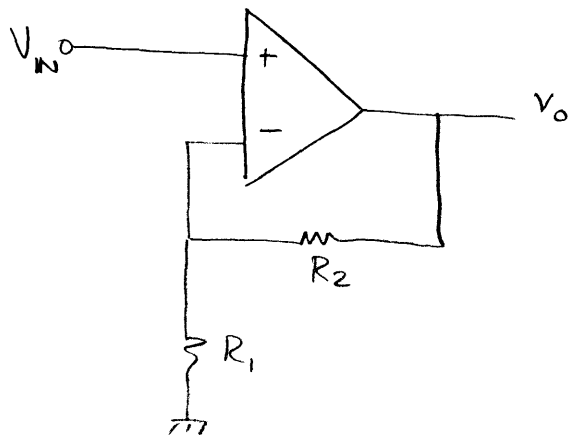
$$V_{os} \cong \frac{V_B\,(dc)}{1000}$$

trim to zero using special circuit

---

read history of op-amp on p.115.

non-inverting amplifier



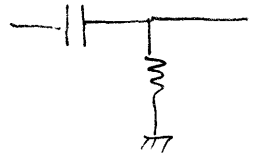
$$V_o = A(V_+ - V_-) = A\left(V_{in} - \frac{R_1}{R_1+R_2} V_o\right).$$

$$V_o\left(1 + \frac{AR_1}{R_1+R_2}\right) = A\,V_{in}$$

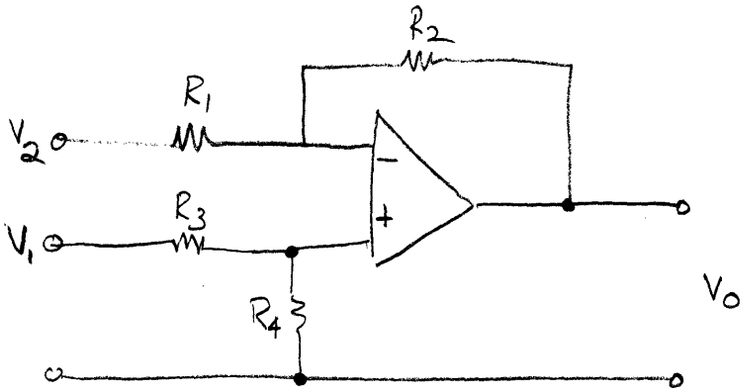
$$\frac{V_o}{V_{in}} = \frac{A}{1 + \frac{AR_1}{R_1+R_2}} \rightarrow \frac{R_1+R_2}{R_1} \quad \text{as} \quad A \rightarrow \infty$$

$$\cong 1 + \frac{R_2}{R_1}$$

see p. 95 Horowitz



if source is ac coupled you must provide a resistance to ground for I_{os}, otherwise the amp will not work.



We can use superposition to analyze this circuit

If $V_1 = 0$ then we have an ordinary inverting op-amp given by

$$V_o = -\frac{R_2}{R_1} V_2$$

The analysis for $V_2 = 0$ is a little more complex.

If $V_2 = 0$, then $V_- = \frac{R_1}{R_1 + R_2} V_o$

$$V_+ = \frac{R_4}{R_4 + R_3} V_1$$

$$V_o = A\,(V_+ - V_-)$$

$$V_o = A\left(\frac{R_4}{R_4 + R_3} V_1 - \frac{R_1}{R_1 + R_2}\right) V_o$$

$$V_o + \frac{A R_1}{R_1 + R_2} V_o = \frac{A R_4}{R_3 + R_4} V_1$$

$$\left(\frac{R_1 + R_2 + A R_1}{R_1 + R_2}\right) V_o = \left(\frac{A R_4}{R_3 + R_4}\right) V_1$$

$$V_o = \frac{A R_1 + A R_2}{A R_1 + R_1 + R_2} \frac{R_4}{R_3 + R_4} V_1$$

and as $A \to \infty$

$$V_o = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_1$$

by superposition

$$V_o = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_1 - \frac{R_2}{R_1} V_2$$

$$V_o = \frac{R_2}{R_1}\left[\frac{R}{R_2}\left(\frac{R_1+R_2}{R}\right)\frac{R_4}{R_3+R_4}V_1 - V_2\right]$$

$$V_o = \frac{R_2}{R_1}\left[\left(\frac{R_1+R_2}{R_2}\right)\left(\frac{R_4}{R_3+R_4}\right)V_1 - V_2\right].$$

Now, if the coefficient of V_1 is 1

$$V_o = \frac{R_2}{R_1}\left[V_1 - V_2\right]$$

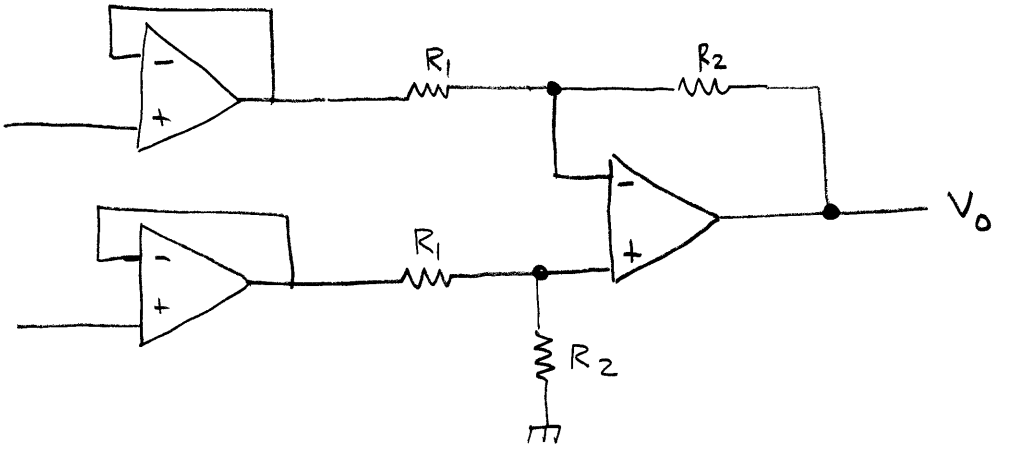
this is a differential amplifier whose output depends upon the difference between the inputs. For $\frac{R_1+R_2}{R_2}\frac{R_4}{R_3+R_4} = 1$

we get $\frac{R_1+R_2}{R_2} = \frac{R_3+R_4}{R_4}$

or $\frac{R_1}{R_2}+1 = \frac{R_3}{R_4}+1$

The requirement is that $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

The input current at the non-inverting input depends upon R_3 and R_4. (Assuming I_{os} is very small). On the other hand the input current at the inverting input is dependent upon R_1 and V_1. This is undesirable in high-performance systems where we want R_{IN} to be always very large. Consequently we will usually precede each input by a non-inverting amplifier.



Experimental procedures

Ideal amplifier only responds to $(V_2 - V_1)$

<u>real</u> amplifiers <u>also</u> have a small dependence on the individual input voltages

A_{cm} common-mode

A_{DM} difference-mode

$V_{icm} \triangleq$ average of the two inputs $= \frac{V_1 + V_2}{2}$

$V_{idm} =$ difference of the inputs $= V_1 - V_2$

An amplifiers output is thus given by

$$V_o = A_{cm} V_{icm} + A_{dm} V_{idm}$$

$$= A_{cm} \frac{V_1 + V_2}{2} + A_{dm} (V_1 - V_2)$$

$$= \left(\frac{A_{cm}}{2} + A_{dm}\right) V_1 + \left(\frac{A_{cm}}{2} - A_{dm}\right) V_2$$

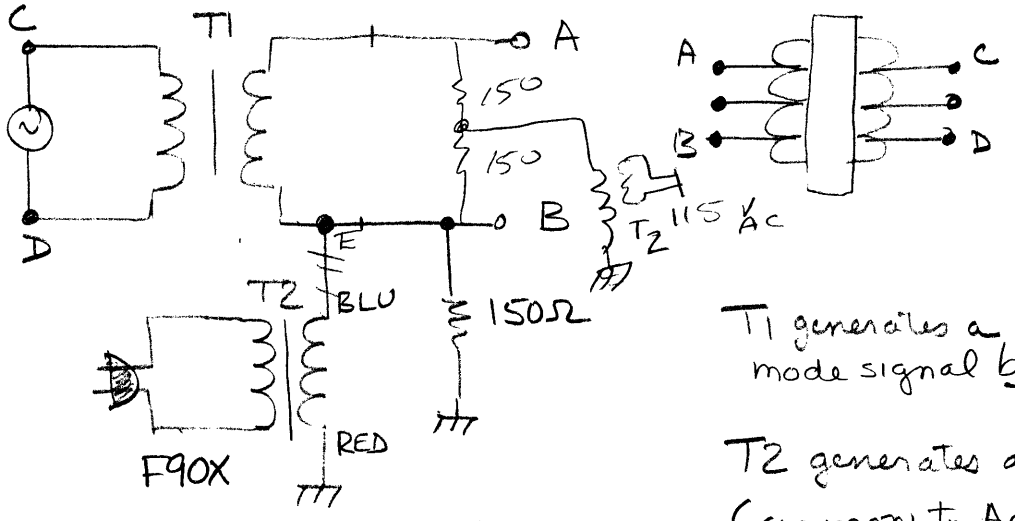
With two constants we can represent any two coefficients

In a real-application we want A_{cm} to be as small as possible

$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$$

A very good amp will have CMRRs greater than 100db.

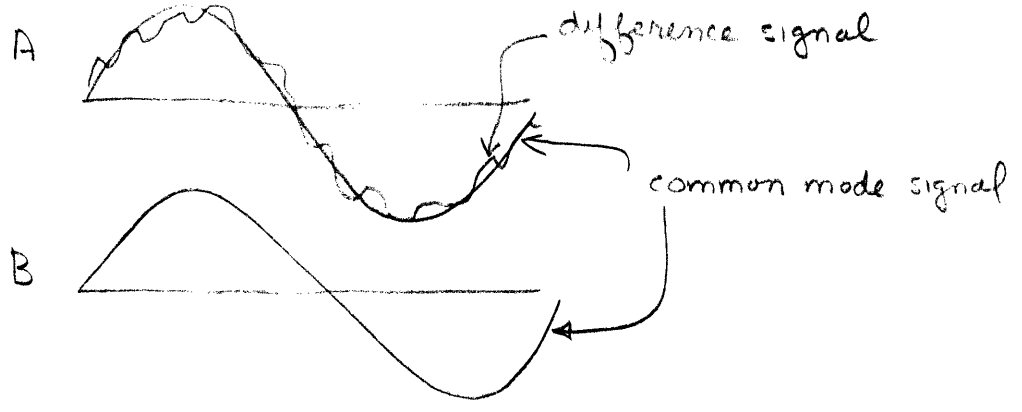
how to generate differential and common mode signals.



T1 generates a differential mode signal <u>between</u> A and B.

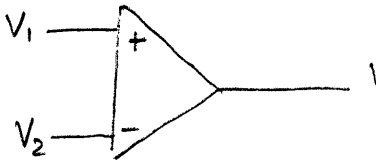
T2 generates a common mode (common to A and B) voltage <u>at</u> A and B; The 150Ω resistor provides a ground path for T2.

technically



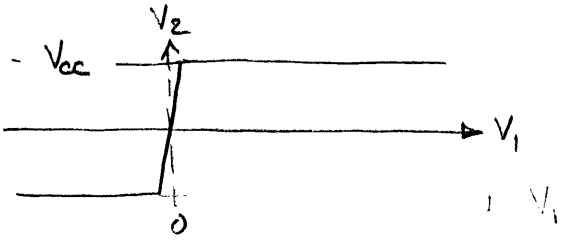
comparator — determine which of two signals is larger
— knows when a signal exceeds a given threshold.

simplest comparator — high gain differential amplifier



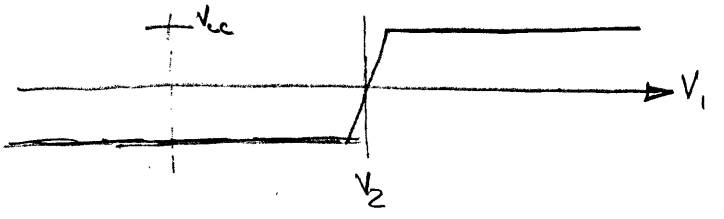
$V_{out} = A(V_1 - V_2)$

if $V_2 = 0$

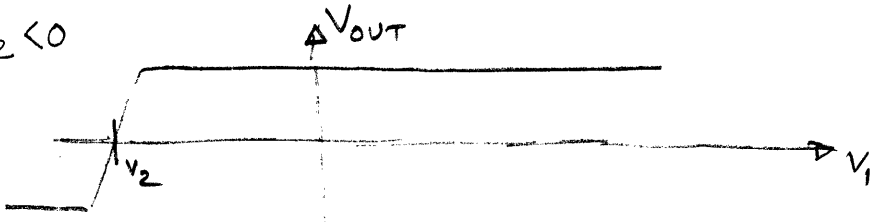


$V_1 - 5$

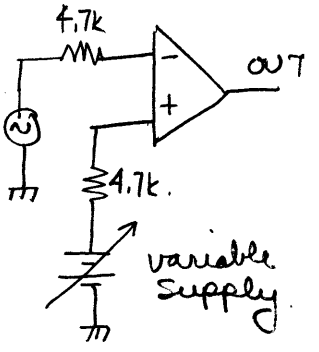
$V_2 \neq 0$, $V_2 > 0$



$V_2 < 0$



lab circuit

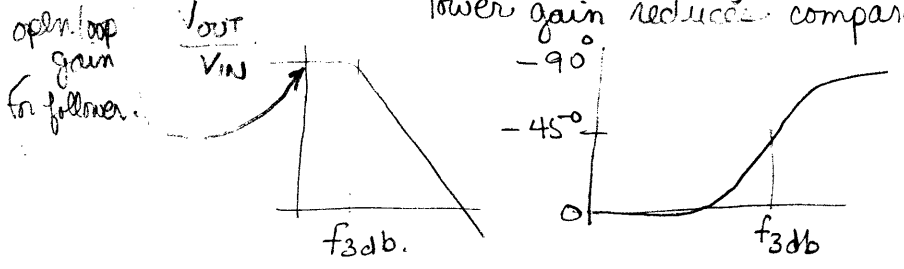


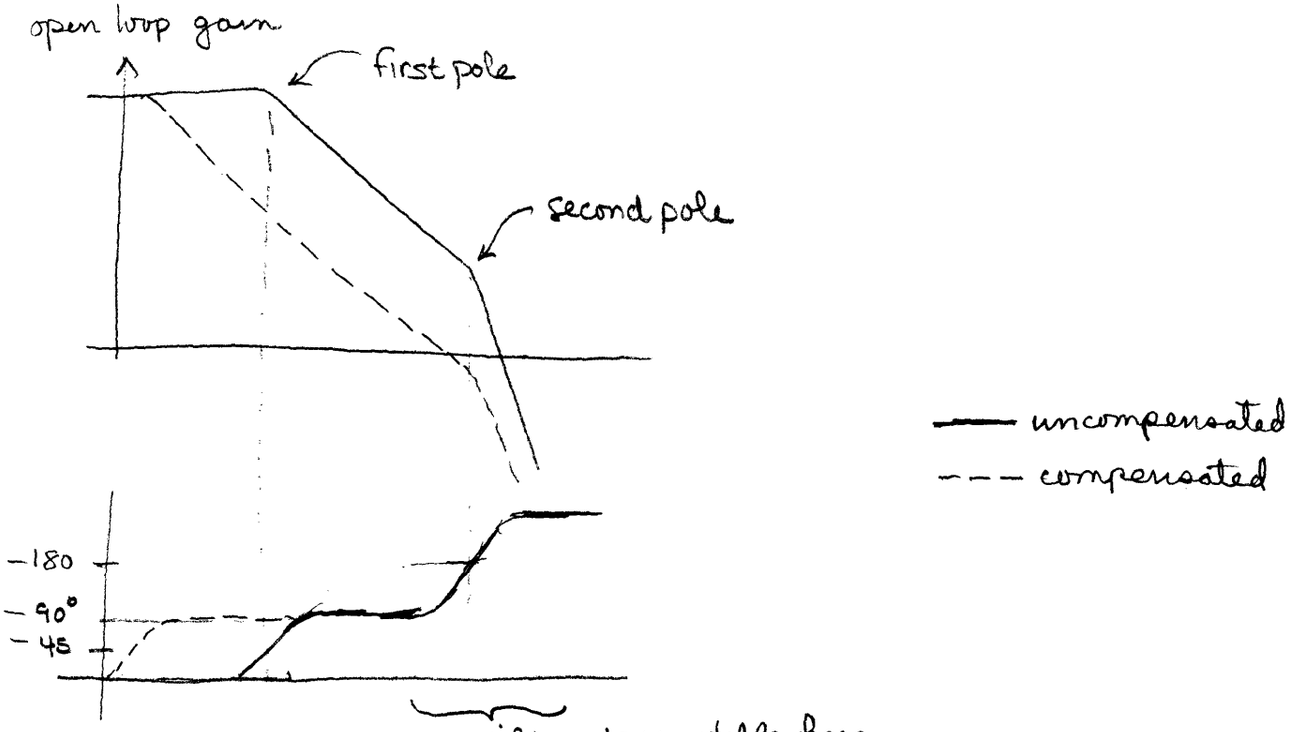
excellent for alarms!

op-amps are usually not good — use specialized IC chips instead
i.e. LM311
with better output circuits

Never use negative feedback — unstable with negative feedback.

need high gain for comparator
lower gain reduces comparator action.

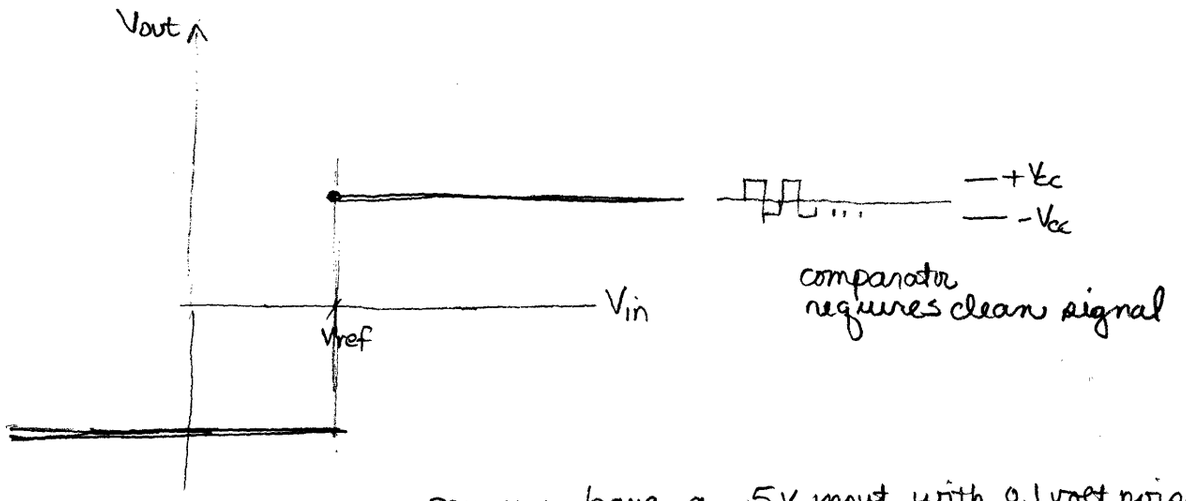




amplifier gets unstable here
since 180° feedback point has positive gain

compensate to reduce gain

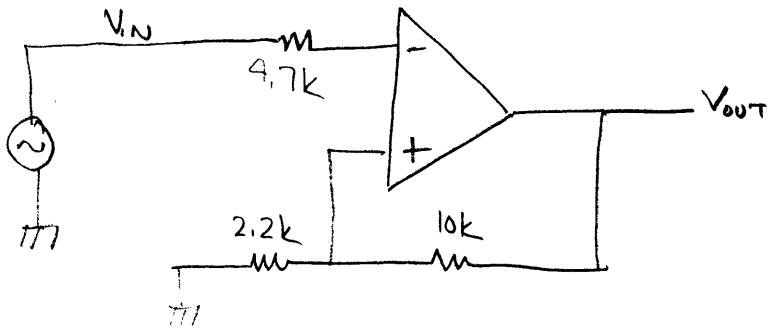
problems with noise:



comparator requires clean signal

say you have a 5V input with 0.1 volt noise

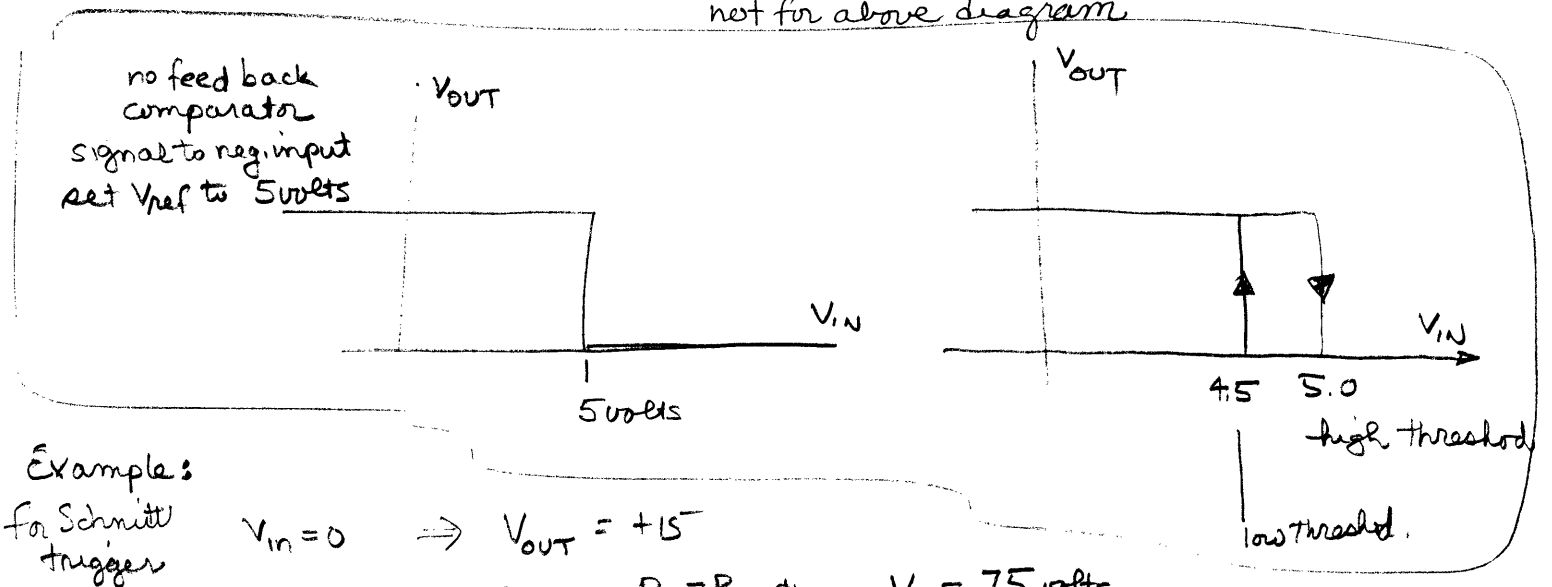
How to elimate noise – feedback to get hysteresis



POSITIVE FEEDBACK!

Figures 3.54, 3.55, 3.56 are very good.

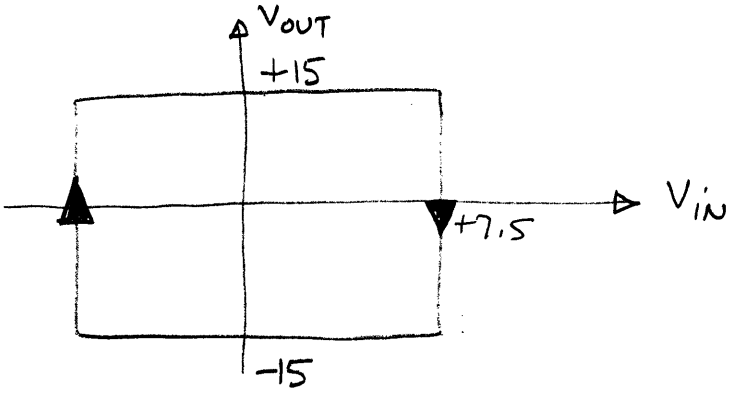
not for above diagram



Example: for Schmitt trigger $V_{in} = 0 \Rightarrow V_{OUT} = +15$

Suppose $R_2 = R_3$ then $V_+ = 7.5$ volts, forcing $V_{OUT} = +15$

If the input voltage rises to +7.5 no change in V_{OUT} when input rises to +7.50015 output switches to −15V and V_+ changes to −7.5 volts, voltage must drop to below −7.5 volts, i.e. −7.50015 before the output switches.

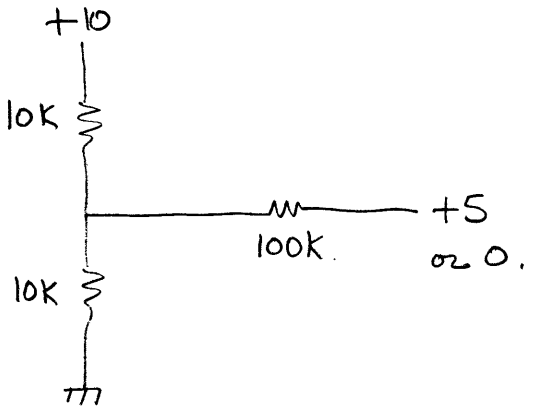


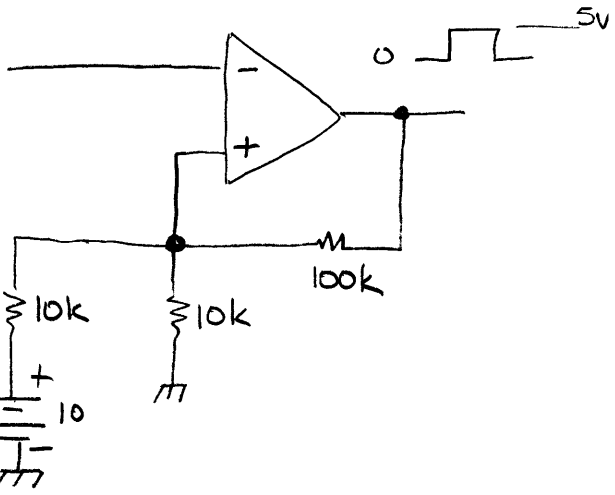
What are the upper and lower trigger points set by?

$$\left(\frac{2.2}{10+2.2}\right)15 = \frac{2.2}{12.2}\,15$$

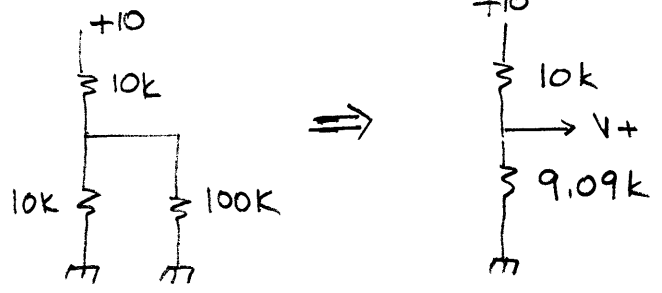
≈ 2.7 volts.

Sample calculation

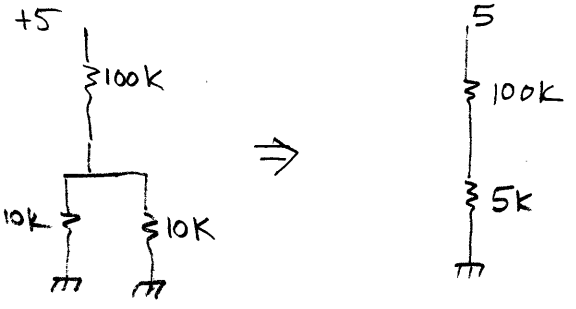




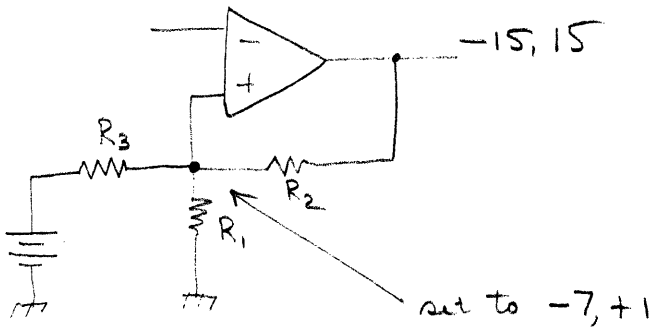
use superposition

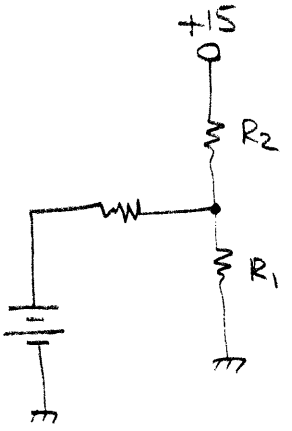


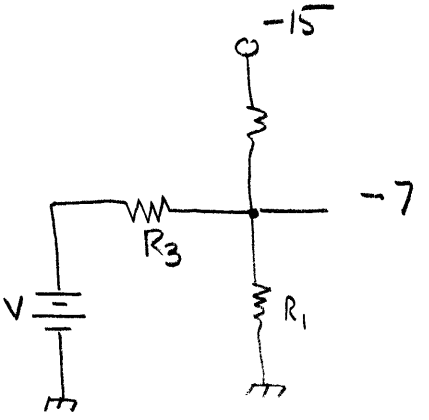
$$V_+ = \frac{9.09}{10+9.09}(10) = 4.76$$



$$V_+ = \frac{5}{100+5}(5) = \frac{5}{105}(5) = 0.24V.$$







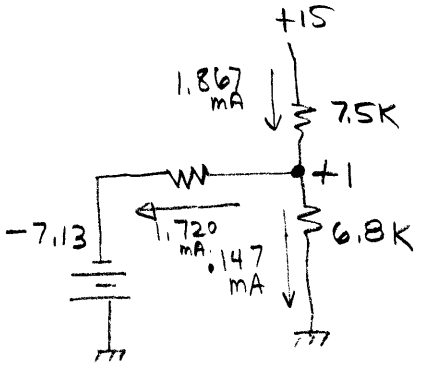
pick $R_1 = 6.8\,K$

Then $\left(\frac{6.8}{6.8+R_2}\right)15 = 7$

$R_2 = \frac{(6.8)(15)}{7} - 6.8 = 14.57 - 6.8 = 7.7k$

$\Rightarrow$ pick $R_1 = 6.8K$

$R_2 = 7.5K$

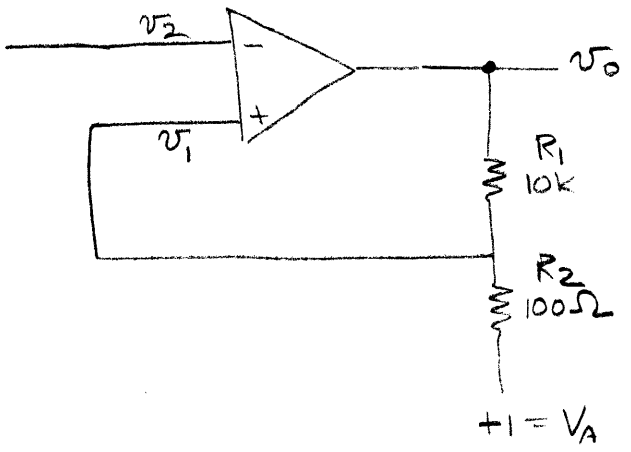


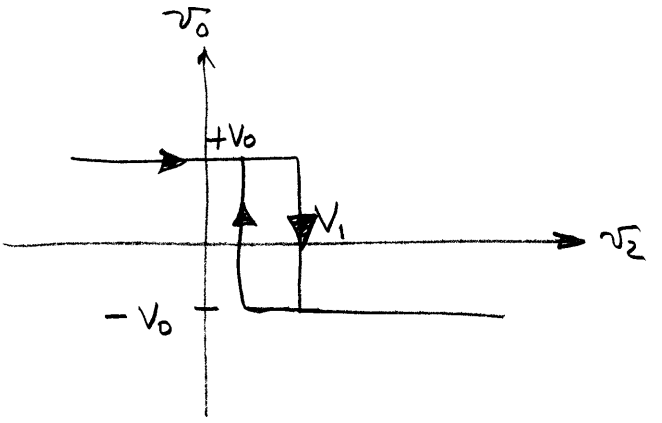
This gives $\frac{6.8}{6.8+7.5}15 = 7.13$ volts.

Set $V = -7.13$ volts

$$R_3 = \frac{+1-(-7.13)}{1.720\,mA}$$

$$= \frac{8.13}{1.720\,mA} = 4.73k$$





$$v_o = A\, v_i$$

feedback gain $\quad T = -\dfrac{R_2 A v}{R_1 + R_2}$

---

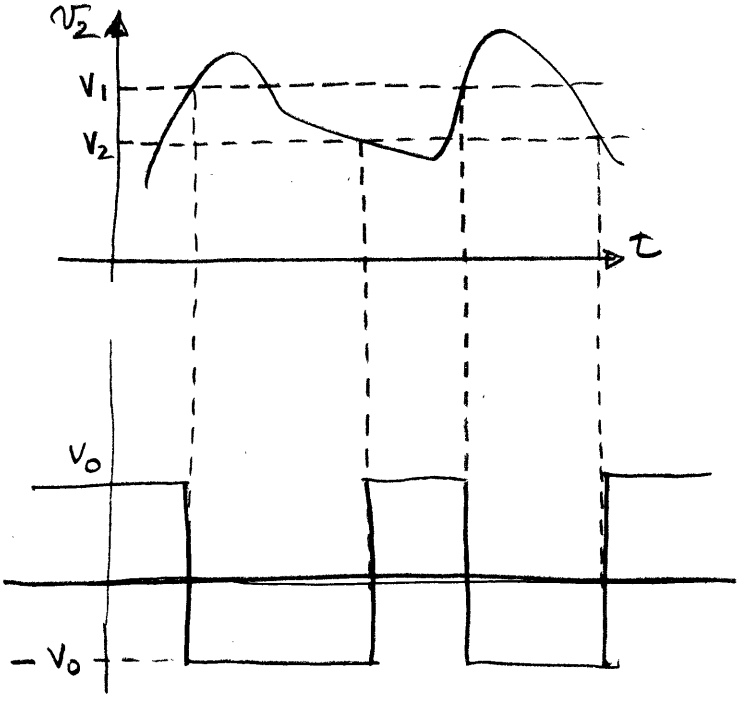
let $\quad v_o = +V_o$

$$v_1 = V_A + \frac{R_2}{R_1 + R_2}(V_o - V_A) \equiv V_1$$

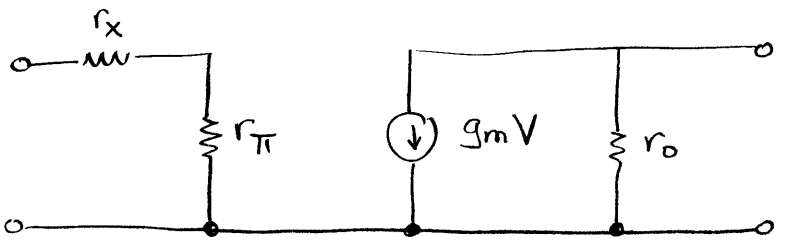
notice that if v_2 is increased v_o remains constant at V_o and $v_1 = V_1$ until $v_2 = V_1$.
At this threshold, the output switches to $v_o = -V_o$

$$v_1 = V_A - \frac{R_2}{R_1 + R_2}(V_o + V_A) \equiv V_2 < V_1$$

difference between V_2 and V_1 is the hysteresis:



Hybrid-π transistor model.



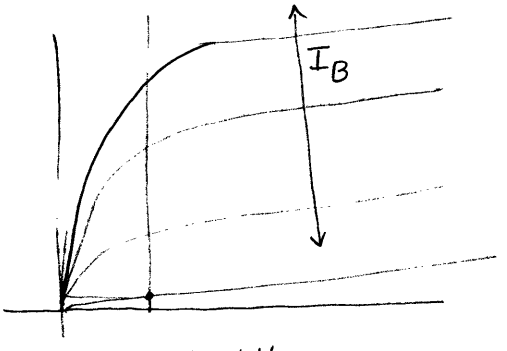
β_{dc} dc beta

β_o ac beta

r_π input resistance

$$g_m = \frac{|I_c|}{25\,mV}$$

$\beta \approx$ independent of I_c.

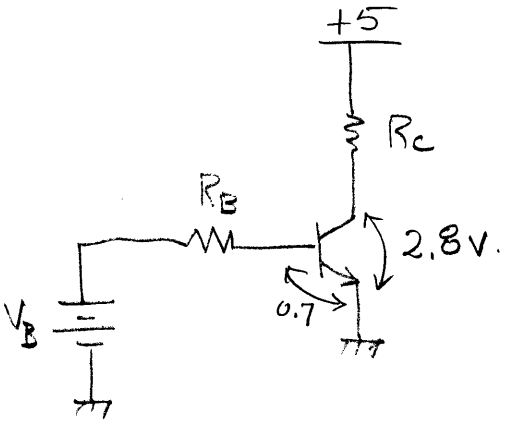


$$\beta_{dc} = \frac{I_c}{I_B}.$$

depends upon where Q-point is located.

$$\beta_o = \beta_{AC} = \frac{\Delta I_c}{\Delta I_B}$$

DC analysis

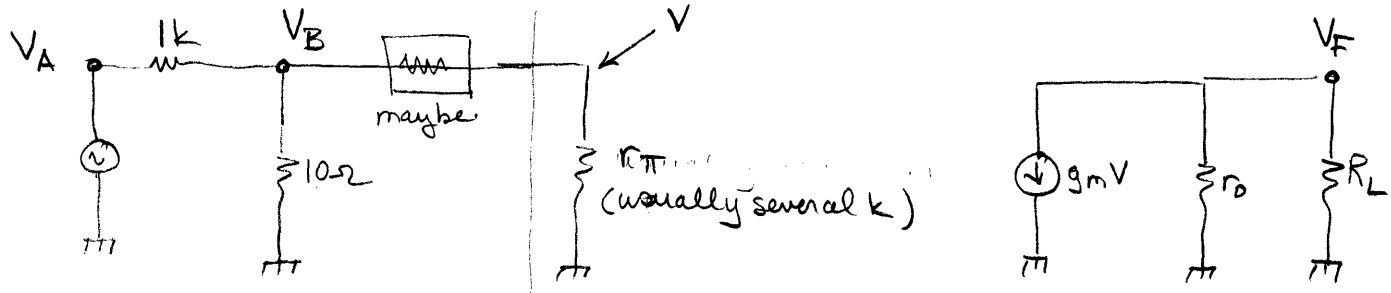


$I_c = 1mA$ or $I_c = 100mA$.

$$I_B = \frac{V_B - 0.7}{R_B}$$

$$\therefore \beta_{DC} = \frac{I_c}{I_B} = \frac{I_c R_B}{V_B - 0.7}$$

AC analysis:



dc bias does not change so r_π does not change.

dc bias circuit not shown.

$V_B \approx \frac{10}{1010} V_A$ irregardless of R_S or R_B or r_π since 10Ω is so small.

$V_B = \frac{V_A}{101}$

If $R_S = 0$

$V = V_B$

$V_F = -(g_m V)(r_o \| R_L)$

$\approx R_L$ since $r_o >> R_L$

$V_F \approx -g_m \frac{V_A}{101} R_L = -g_m r_\pi \left(\frac{V_A}{101}\right) \frac{R_L}{r_\pi} = -\beta_{AC} \left(\frac{V_A}{101}\right) \frac{R_L}{r_\pi}$

If $R_S = 4.7K$. $\quad V = V_B \frac{r_\pi}{r_\pi + 4.7K}$

$V_F \approx -(g_m) \frac{V_A}{101} \left(\frac{r_\pi}{r_\pi + 4.7k}\right) R_L = -\beta_{AC} \left(\frac{V_A}{101}\right) \frac{R_L}{r_\pi + 4.7k}$

$\therefore$ $\boxed{\frac{V_F}{V_A} = -\frac{\beta_{AC}}{101} \frac{R_L}{r_\pi + R_S}}$ unknowns are β and r_π.

$$\underbrace{-\frac{101}{R_L}\frac{V_F}{V_A}}_{\text{call this } K} = \frac{\beta_{AC}}{r_\pi + R_S}$$

$$K_1 = \frac{\beta_{AC}}{r_\pi}$$

$$K_2 = \frac{\beta_{AC}}{r_\pi + 4.7K.}$$

solve for β_{AC} $\quad r_\pi K_1 = \beta_{AC} = K_2 (r_\pi + 4.7K)$

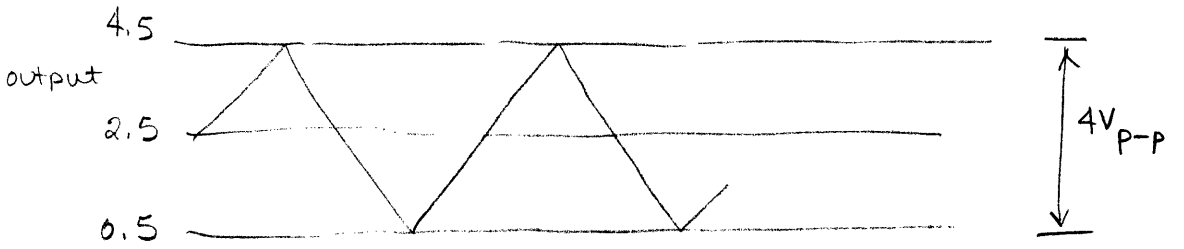
$$r_\pi K_1 = r_\pi K_2 + (4.7K) K_2 ,$$

$$r_\pi (K_1 - K_2) = (4.7K) K_2$$

$$r_\pi = \frac{(4.7K)\, K_2}{K_1 - K_2} .$$

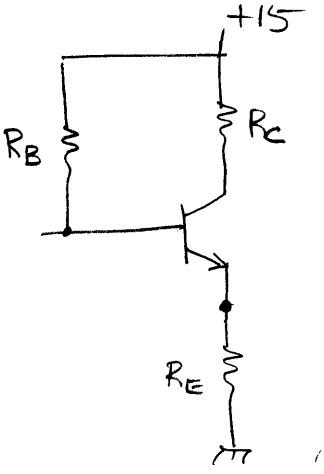
Part 2

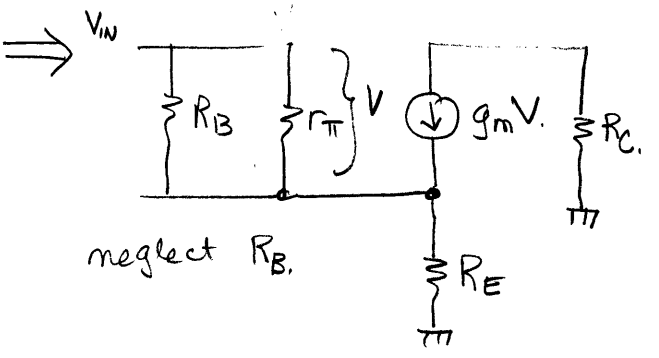
distortion , adjust V_{Gen} to get V_T shown below



adjust the scale factor and variable sensitivity so that both waveforms have identical amplitudes. subtract the waveforms and record.

Part 3

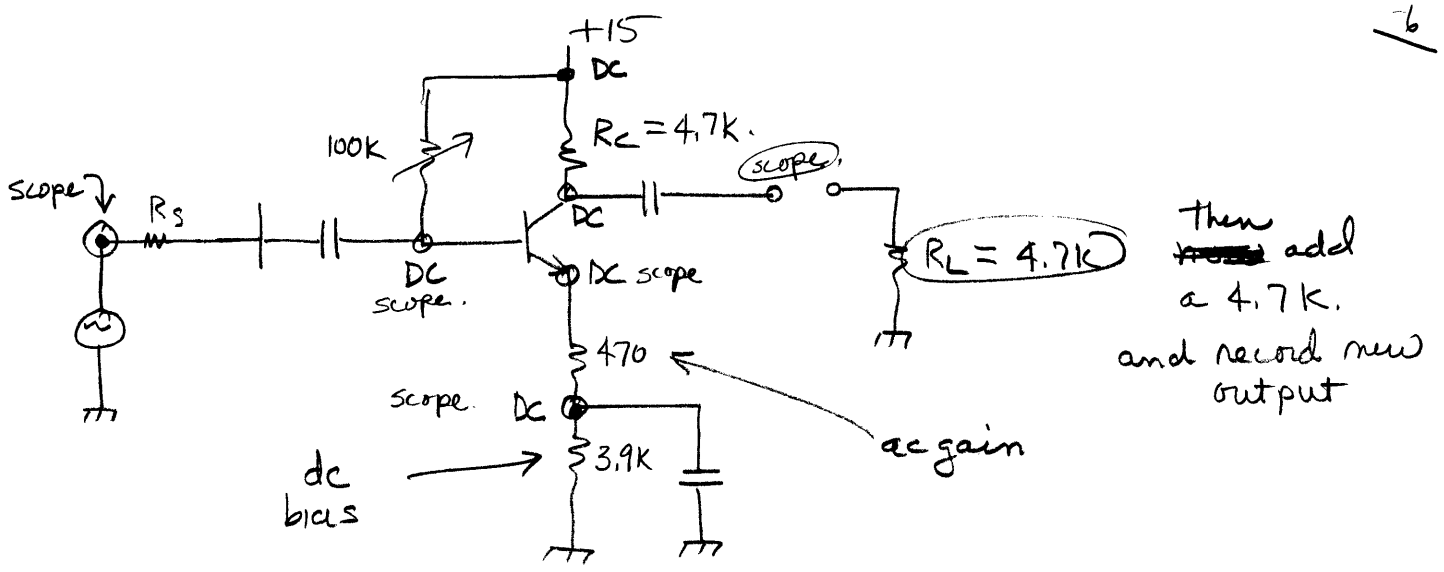




simple ac analysis $V = V_{IN} \dfrac{r_\pi}{(\beta+1)R_E + r_\pi}$

$$V_{OUT} = (g_m V)R_c = \frac{g_m V_{IN} r_\pi}{(\beta+1)R_E + r_\pi} \cdot R_c = \frac{\beta R_c}{(\beta+1)R_E + r_\pi} V_{IN}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\beta R_c}{(\beta+1)R_E + r_\pi} \approx \frac{R_c}{R_E}$$



(1) do dc measurements, no ac } $R_S = 0$
(2) do ac measurements } $R_L = \infty$

(3) now $R_L \rightarrow 4.7k$ measure ac out.

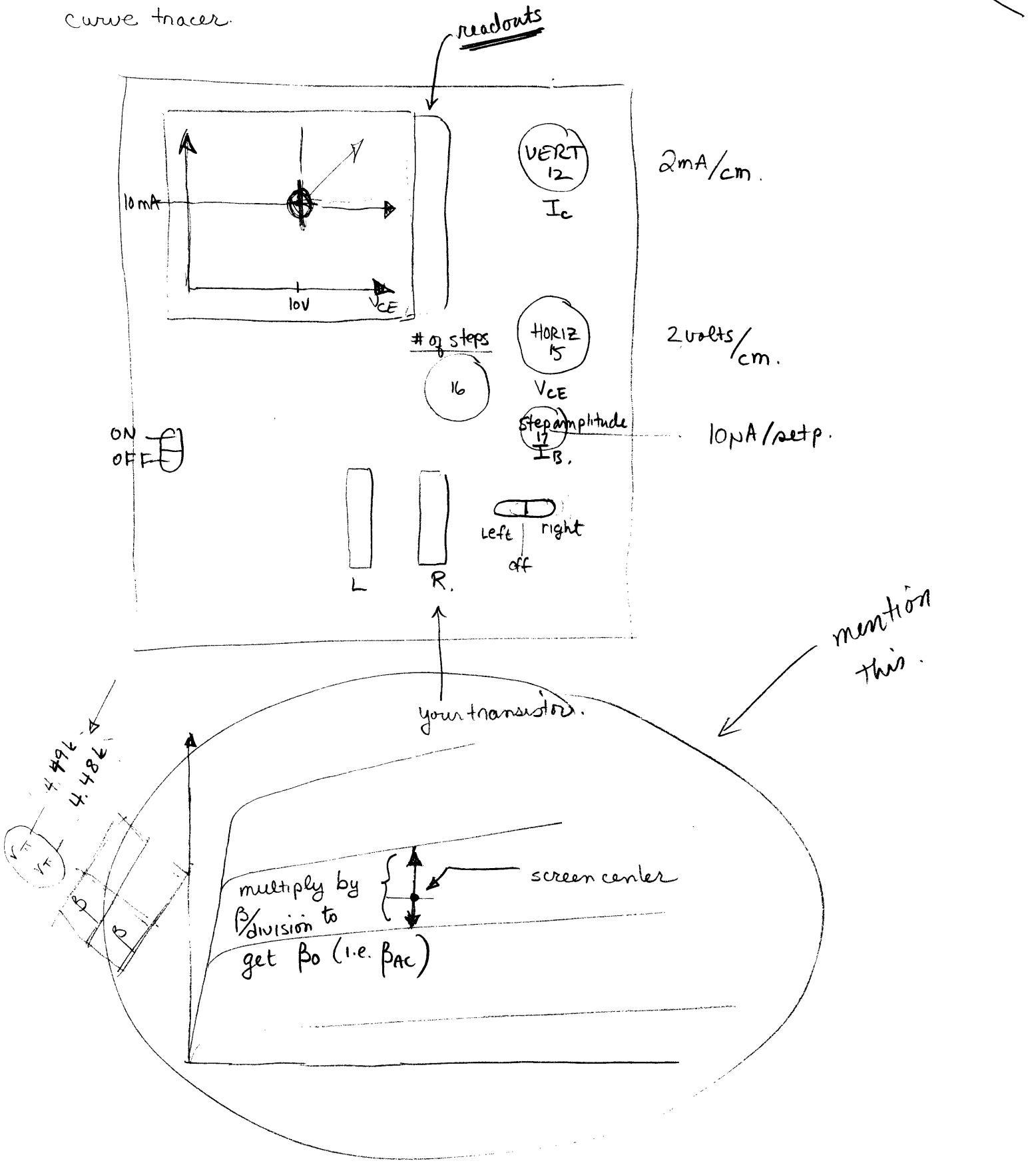
(4) $R_L \rightarrow \infty$, $R_S \rightarrow 27k$ measure at point H

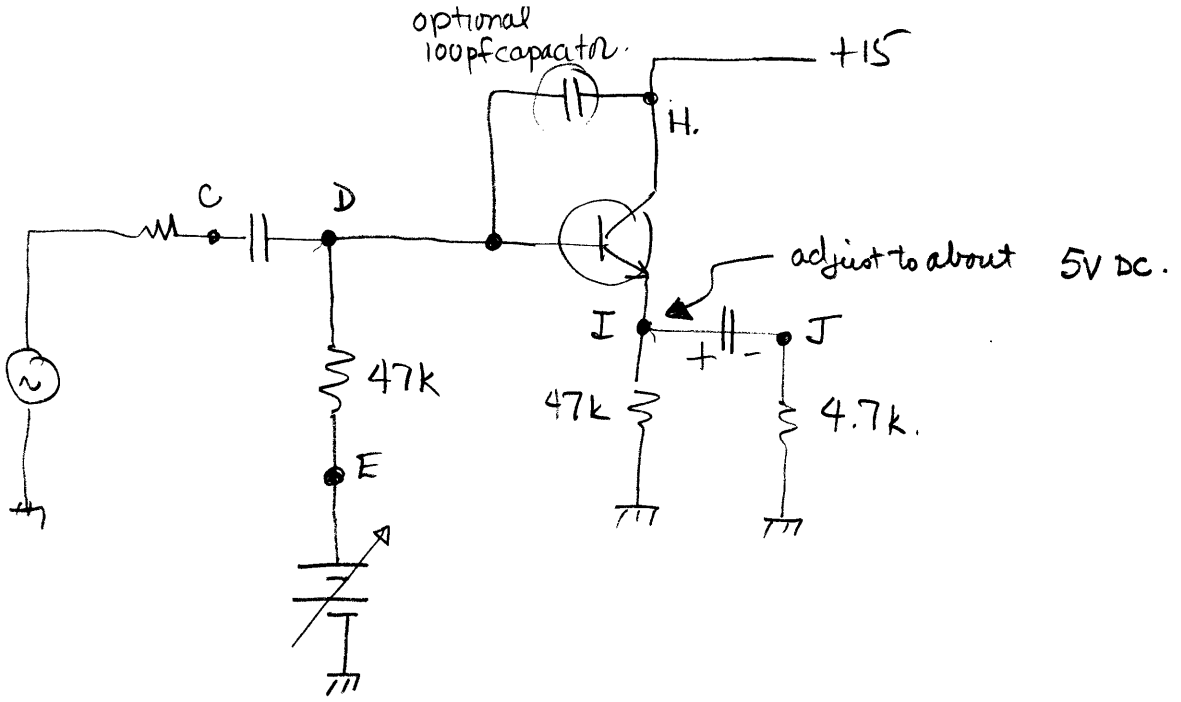
(5) measure $\frac{V_{OUT}}{V_{IN}}$ for $V_{IN} = 1, 2, 3, 4\ V_{p\text{-}p}$.

---

cutoff & saturation

curve tracer.





FIRST bad method

measure C, D, I, J. resistance to ground — BAD, pick up power supply voltages.

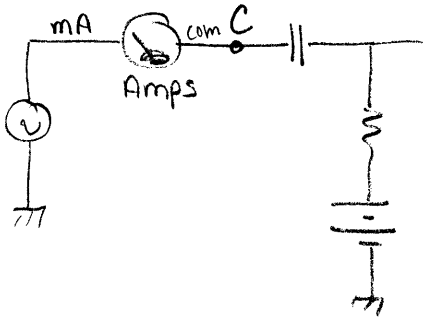
dc characteristics

disconnect power supplies and ground H and E — re-measure.

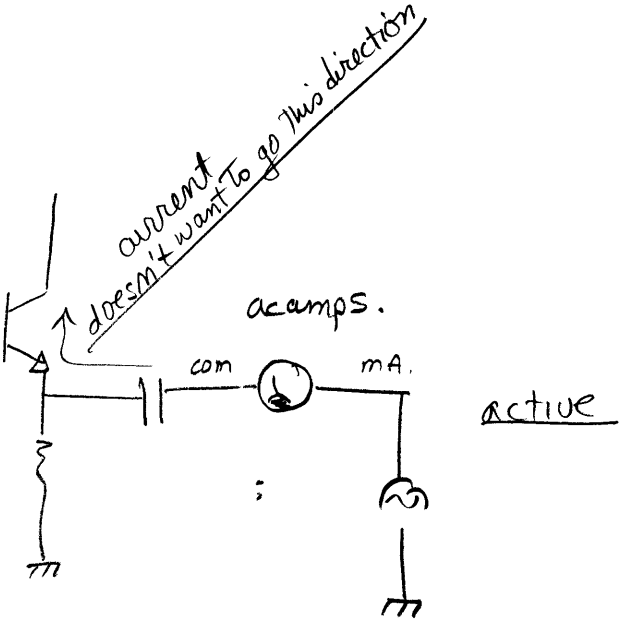
ac characteristics

SECOND bad method

(a) TOO SMALL To measure ac current

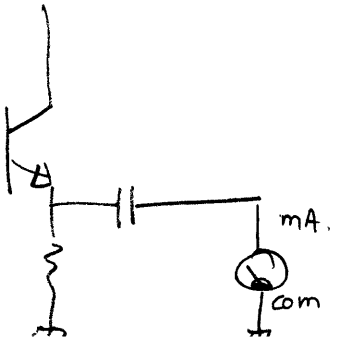


(b)

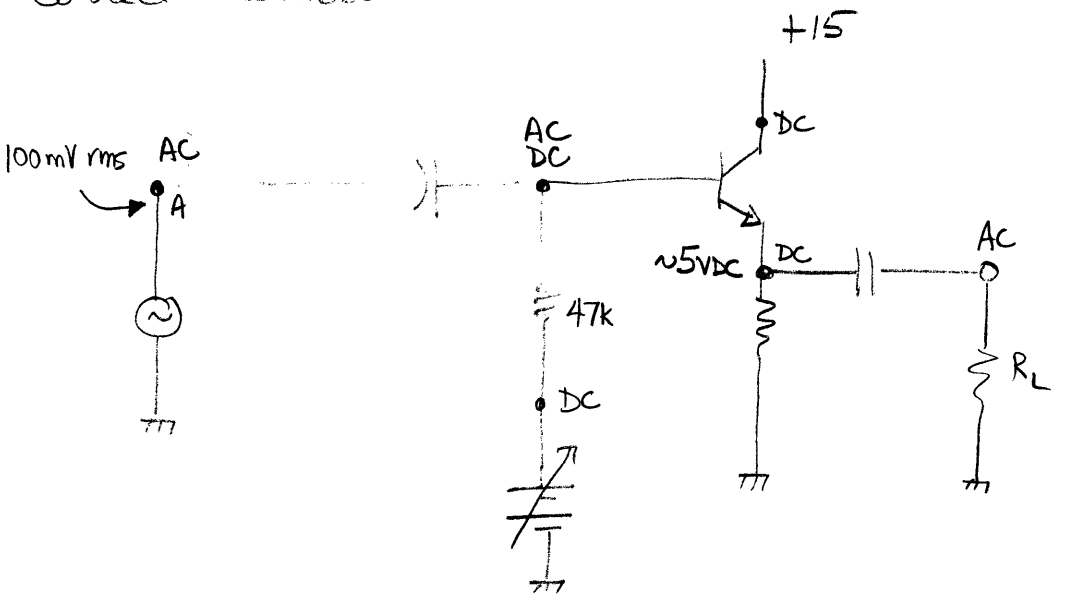


active

THIRD bad method (passive)



correct method.

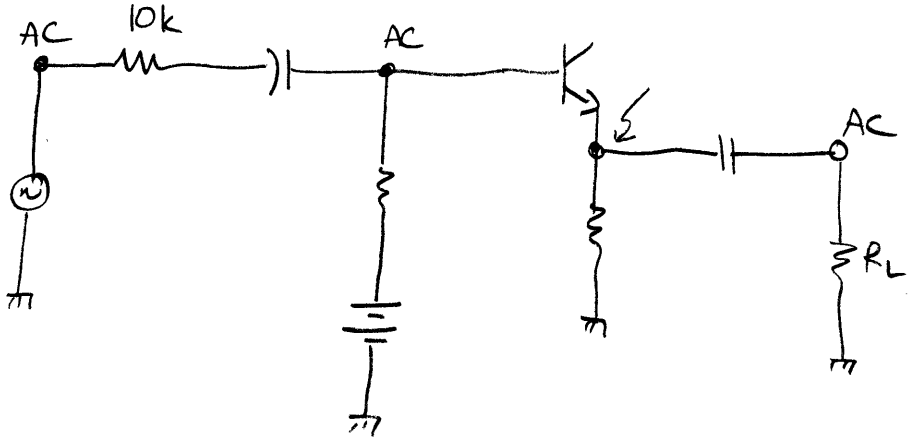


measure dc values once

measure ac values
for R_L = ∞
4.7k
470
47

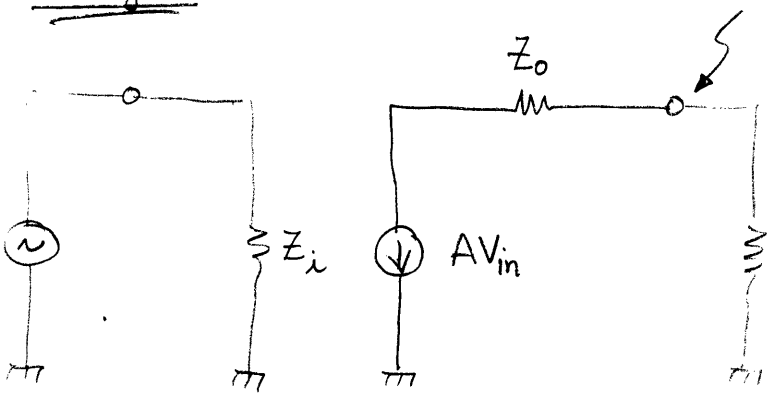
---

now add a 10k input resistance and repeat all ac procedures.



R_L = ∞
4.7k
470
47.

analysis



works best when $Z_L > Z_o$

for output.

measure V_{oc}

$V_{4.7k}$

V_{470}

V_{47}

$$V_{OUT} = \frac{Z_L}{Z_L + Z_o} AV_{in}.$$

if $Z_L = \infty$ $V_{OUT} = AV_{in} = V_{oc}$

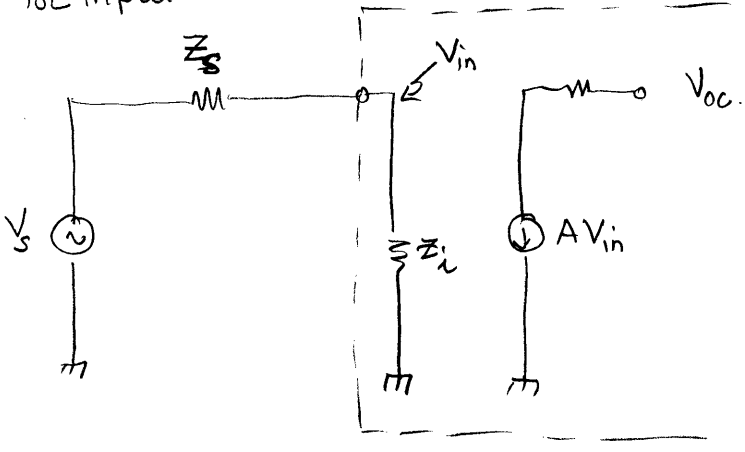
$Z_L = 4.7k$ $V_{OUT} = \frac{4.7k}{4.7k + Z_o} V_{oc}.$

$Z_L = 470$ $V_{OUT} = \frac{470}{470 + Z_o} V_{oc}$

$Z_L = 47$ $V_{OUT} = \frac{47}{47 + Z_o} V_{oc}.$

test to see how consistent these are.

for input.



$V_{oc} = AV_{in}$

by inspection if $Z_s = 0$ $V_{oc} = AV_s$

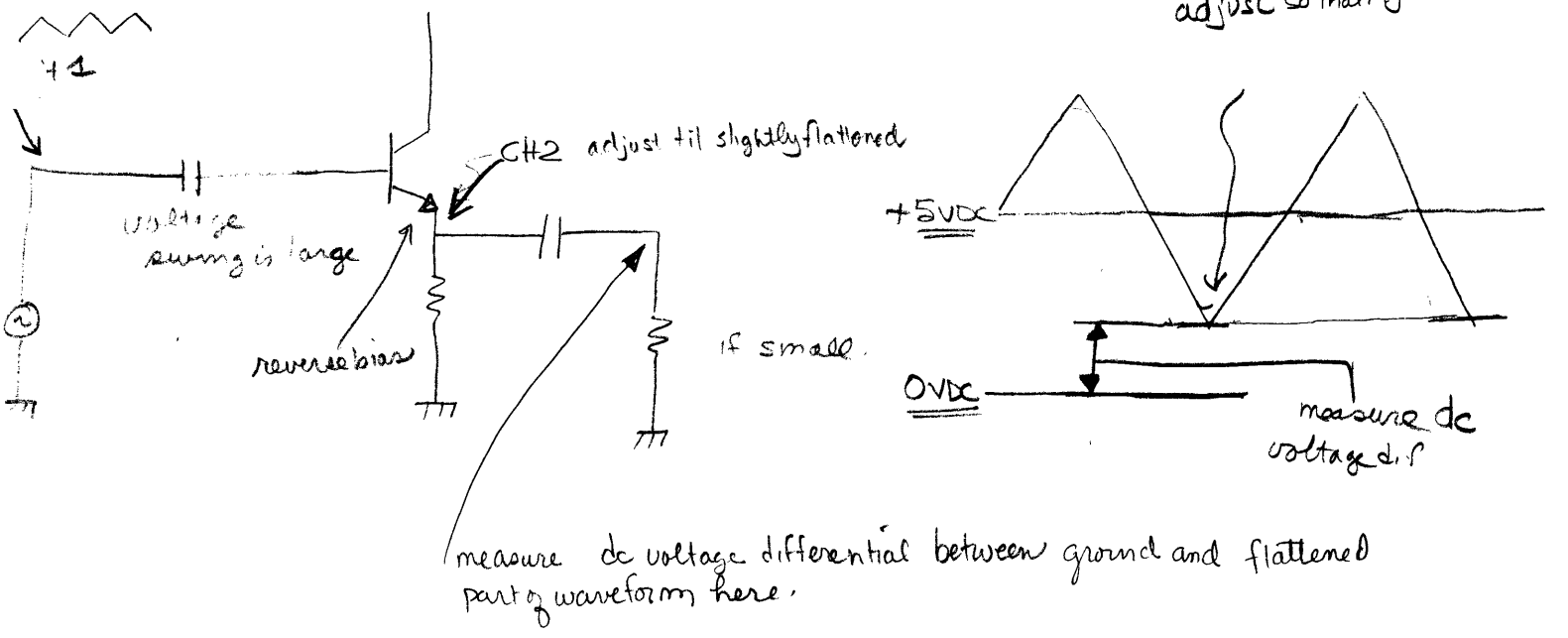
if $Z_s \neq 0$ $V_{in} = \frac{Z_i}{Z_i + Z_s} V_s$

$$V_{OUT} = AV_{in} = \frac{AZ_i}{Z_i + Z_s} V_s.$$

$$\frac{V_{OUT,\, Z_s = 0}}{V_{OUT,\, Z_s}} = \frac{Z_i}{Z_i + Z_s}$$

and solve for Z_i

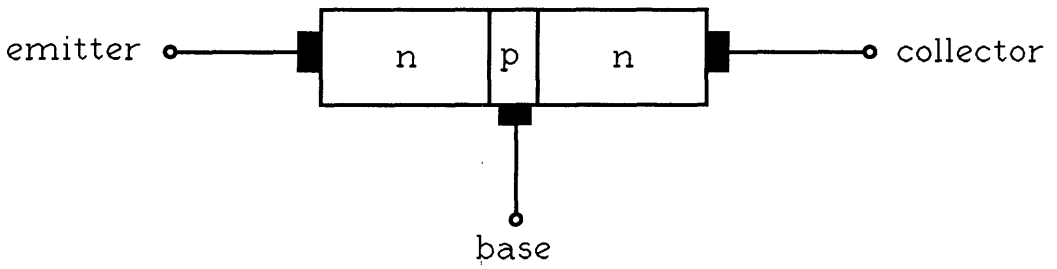
part 3



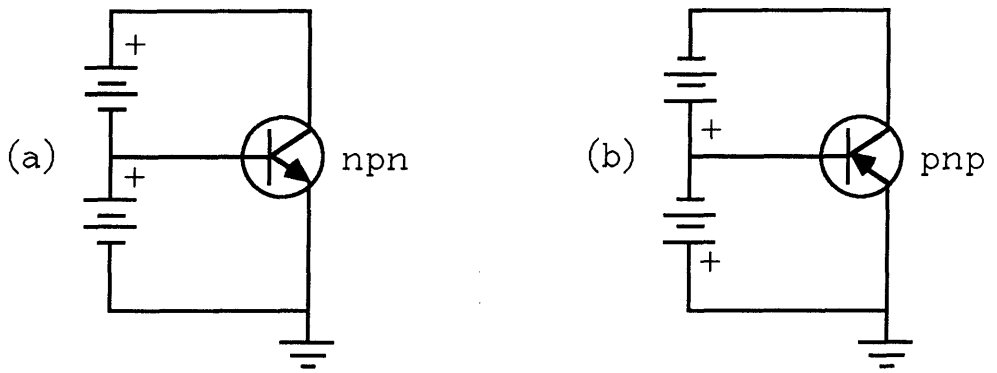
measure dc voltage differential between ground and flattened part of waveform here.

DC CHARACTERISTICS OF BJTs AND FETs

Before we can understand how to design circuits usings BJTs and FETs we must review their basic properties. These basic properties are functions of the operational mechanisms of these devices, i.e. the solid state physics which is covered in other courses. The bipolar transistor, or BJT, comes in two types: npn and pnp referring to the physical construction of the device. The npn transistor is a thin slice of p-type material sandwiched between two slabs of n-type material as shown below.



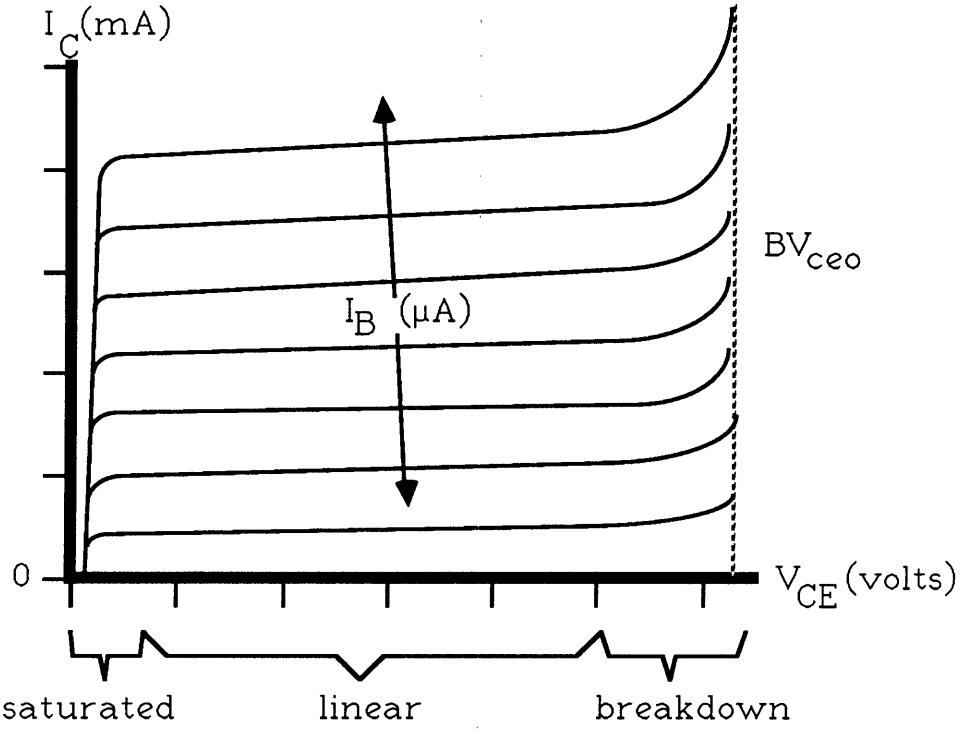
The middle layer is called the base; the substrate (or base upon which the entire structure is fabricated) is called the collector; and the top layer is called the emitter. The net result of this construction is that two diode junctions are formed: one between the collector and base and the other between the base and emitter. In practice, both transistor junctions (the diodes referred to above) are forward biased. Proper bias for npn and pnp transistors are shown below.



The net result of this bias is that current continuously flows through the junctions of the transistor; however, it is the relative magnitudes of these currents and the relationships between these currents that make the transistor an amplifier. For an npn transistor we can regard current as entering the

transistor at both the base and collector and exiting at the emitter. This makes the emitter current the sum of the collector and base currents. The base current is quite small, however, and controls the collector current. The ratio of collector current to base current is the dc beta of the transistor and is denoted by β_{DC}. This ability to amplify current is what makes the bipolar transistor so useful, and even though the primary mode of operation of the BJT is current based, it can usefully function as a voltage and power amplifier when placed in a proper circuit.

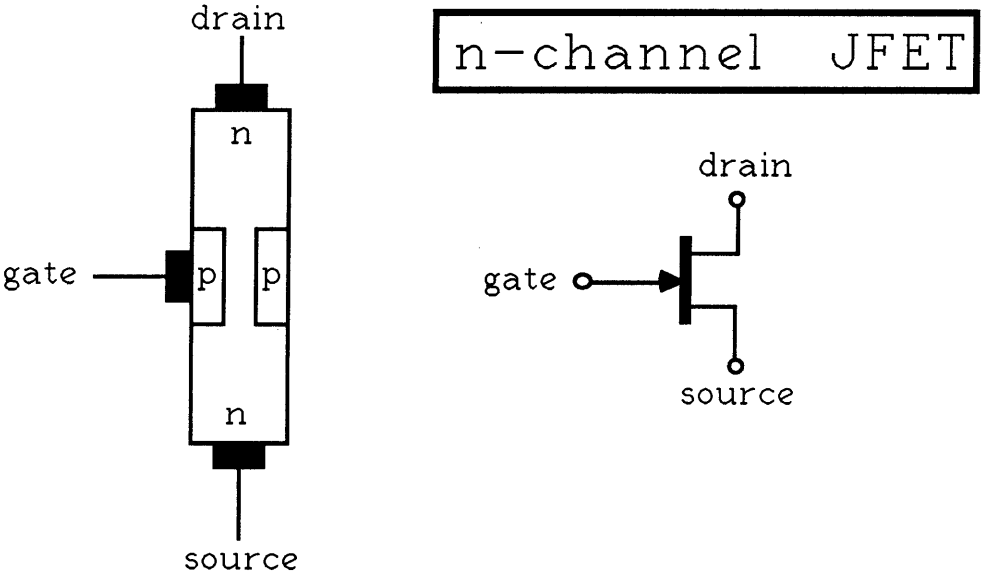
The operation of the BJT can be summarized in the relationship between the base current I_B, the collector current I_C and the collector-emitter voltage V_{CE}. The exact relationship can be derived only after a fair digression into physical electronics. Suffice it to say that all bipolar junction transistors have characteristics similar to those shown in the graph below.



For amplifier operation the BJT is used in the "linear" region where the slope of the I_C-V_{CE} curve is almost constant. This linear region makes possible an amplifier with very little distortion as will be discussed later. One wants to avoid operation, for amplifiers, in the saturated region characterized by small V_{CE} (typically 0.2 volts or less). Similarly, one

wants to avoid operation in the region to the far right of the graph. This is the region in which large electric field strengths from the large V_{CE} can destroy the transistor junction.

Field effect transistors, or FETs, are voltage-biased rather than current biased like BJTs. The basic structure of the FET is a thin connection between two terminals of similar semiconducting material. For example, the p-type material is used to connect two pieces of n-type material through a narrow n-type gate region as shown below. The two pieces of n-type material are known as the drain and source with current flow from the drain to the source for the FET shown below. The p-type/n-type connecting region is known as the channel region and the p-type material is called the gate.

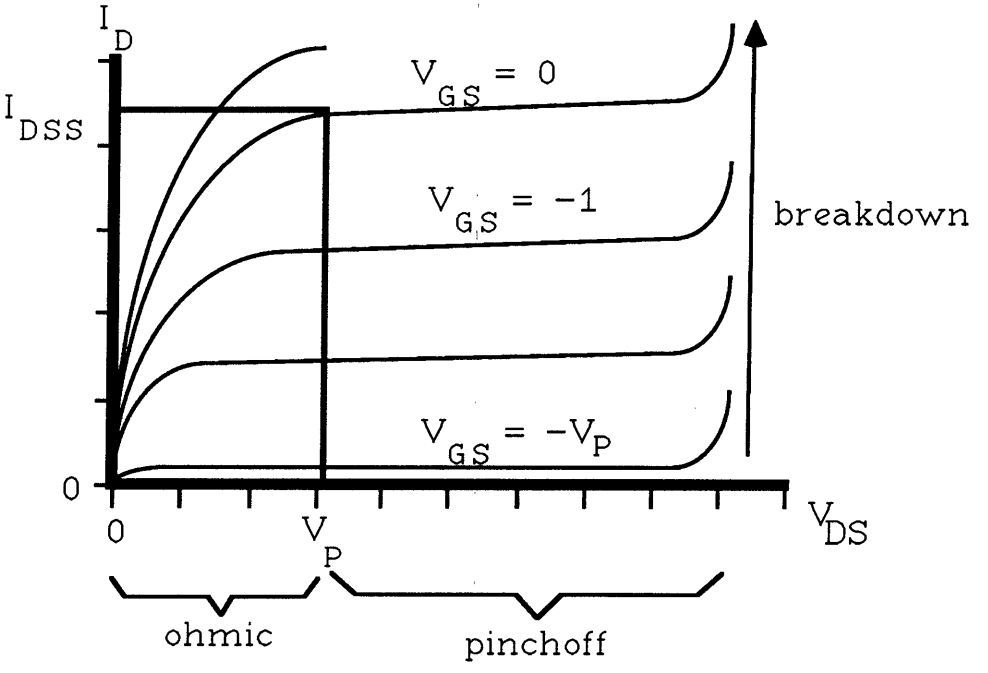


The drain current is at its maximum value I_{DSS} when the gate-source voltage is zero. The precise definition of I_{DSS} is that it is the short circuit drain current, i.e. the drain current that flows when the gate is shorted to the source. For operation of the FET as a control device the gate-source voltage must be negative. This creates a reverse biased diode and produces a depletion region in the neighborhood of the gate. This depletion region reduces the amount of free carriers and consequently reduces the current flow between the source and drain. As the gate-source potential becomes more negative it eventually reaches a point called the pinchoff voltage V_P where the gate depletion regions close together and the source-drain

current becomes essentially zero. The exact relationship between the drain current and V_{GS} is an exact square-law relationship:

$$I_D = I_{DSS}(1 - \frac{|V_{GS}|}{V_P})^2$$

The pinchoff voltage (actually $-V_P$) is also the drain-source voltage which marks the boundary between the ohmic and pinch-off regions of operation of the FET. Essentially, the FET behaves like a variable (but non-linear) resistance in the ohmic region and then remains essentially constant for $V_{DS} > V_P$. For amplifiers it is this linear or pinch-off region that is of interest. In the pinch-off region the drain current is almost linearly proportional to the V_{GS} and independent of V_{DS} (see graph below).



The ratio of change in I_D to the corresponding change in V_{GS} is known as the device transconductance g_m and is of fundamental concern when using the FET as an amplifier. The transconductance when the gate-source voltage is zero is denoted by g_{mo} and is often specified by the transistor manufacturer. The transconductance g_{mo}, the drain

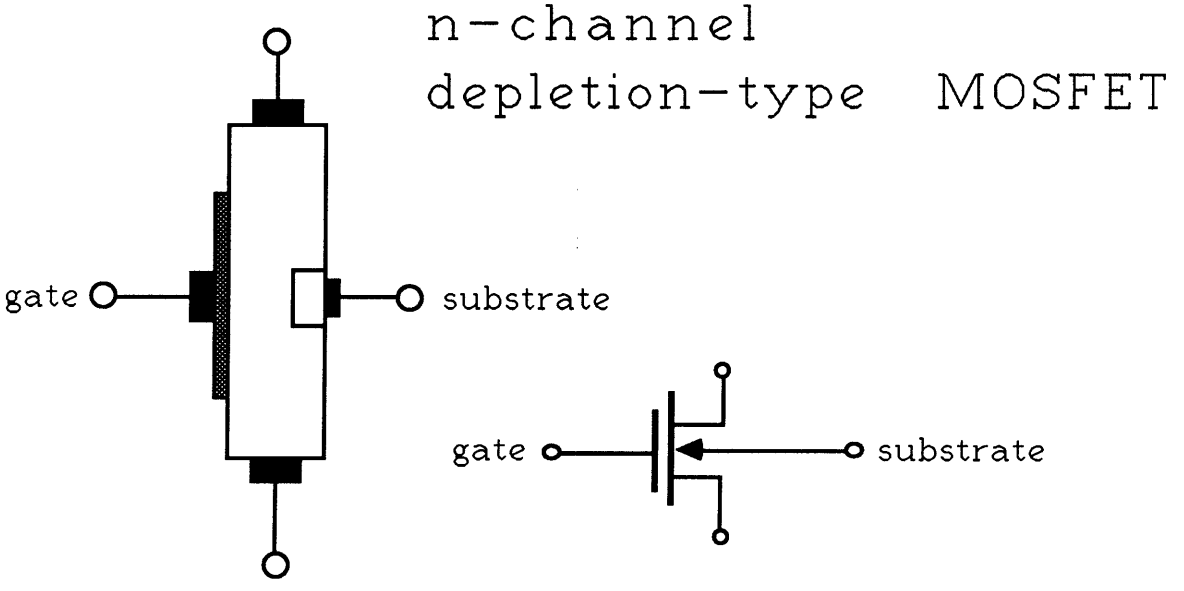
saturation current I_{DSS} and the pinch-off voltage V_P are all related by the relationship

$$g_{mo} = \frac{2I_{DSS}}{|V_p|}$$

where $|V_P|$ is the absolute value of the pinch-off voltage.

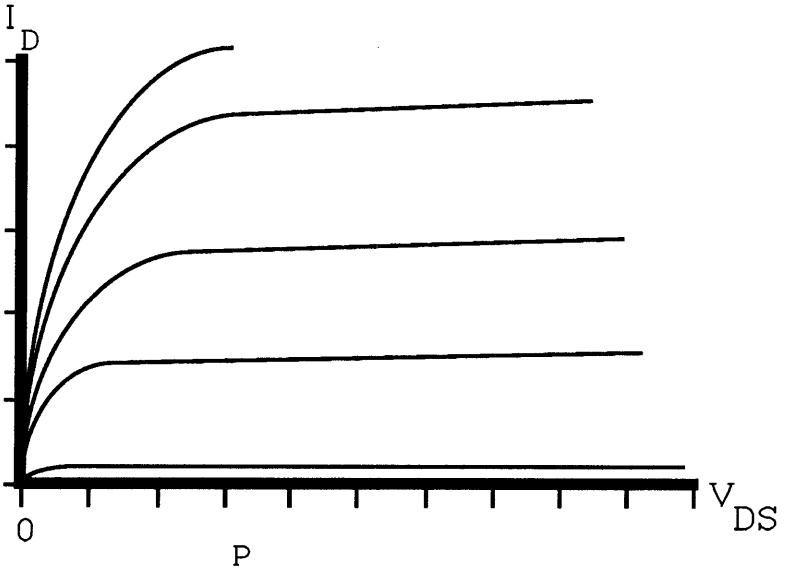
The above discussion was for a n-channel junction FET, or JFET for short. The same device with the semiconductor materials reversed is known as a p-channel JFET.

There is a special version of the JFET known as the MOSFET which is of particular interest in this course. The MOSFET or Insulated Gate FET, is a FET in which a silicon dioxide layer electrically insulates the gate electrode from the rest of the transistor. The internal structure of a MOSFET is shown below.



Since the FET operates by the electrode field created between the gate and the drain and source regions the insulated gate FET also functions in the same manner as an ordinary FET. However, the insulated gate now shifts the gate-source voltages and effectively reduces any already small gate currents to effectively zero.

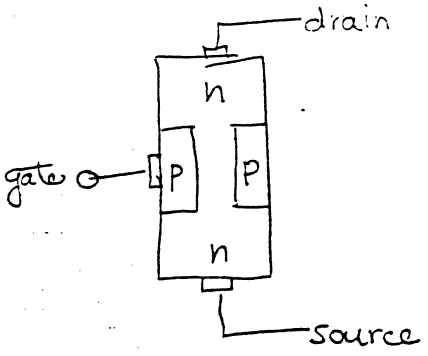
MOSFETs are characterized as enhancement or enhance/depletion mode devices depending upon the properties of the channel. In enhancement mode MOSFETs the drain current increases as V_{GS} increases; however, the channel only exists when V_{GS} is greater than a certain threshold voltage V_T. In enhancement/depletion mode MOSFETs the drain current increases as V_{GS} increases and the FET will continue to operate for $V_{GS} > 0$. Note that enhancement mode MOSFETs are the only type of FET which can operate with a forward biased gate. It must be pointed out that the polarity of V_{GS} is determined by the type of the bulk semiconducting material. Characteristic curves for n-type (not n-channel) enhancement and enhancement/depletion MOSFETs are shown below.

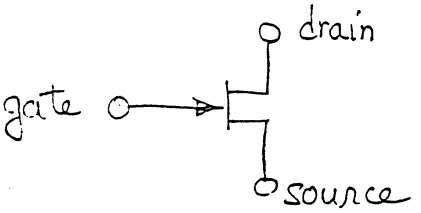


V_{GS} enhancement	enhancement /depletion
+5	+2
+4	+1
+3	0
+2	−1
+1	−2
0	

The structure of the MOSFET is such that multiple gates can be fabricated for a common drain-source geometry. This allows the MOSFET to be used for logic circuits and active devices such as mixers where it is important to keep the device inputs electrically isolated from each other.

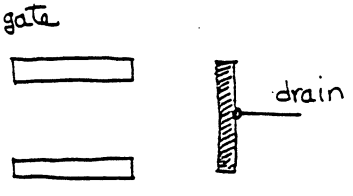
Field effect transistors — voltage amplifiers



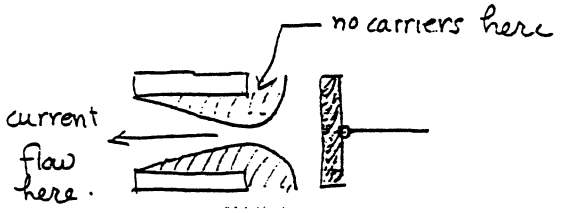


the drain current is at a maximum when $V_{GS}=0$
we call this maximum current I_{DSS}
specifically I_{DSS} is the drain current when the gate is shorted circuited to the source.

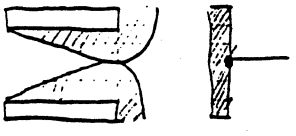
Without going into a lot of detail a FET operates like a voltage controlled resistor. Suppose $V_{GS}=0$. For small values of V_{DS} we have a typical resistor's linear i-v relationship. As V_{DS} increases the gate-drain junction becomes more reverse biased and a larger depletion region, i.e. an area with few mobile charges appears. As V_{DS} increases the depletion region increases increasing the resistance of the junction and lowering the slope (conductance) of the i-v curve.



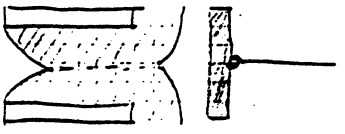
V_{DS} very small.



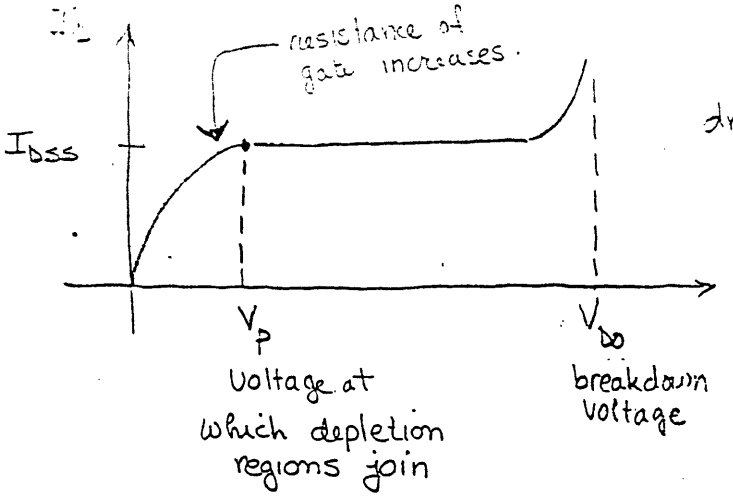
V_{DS} increasing



$V_{DS}=V_P$

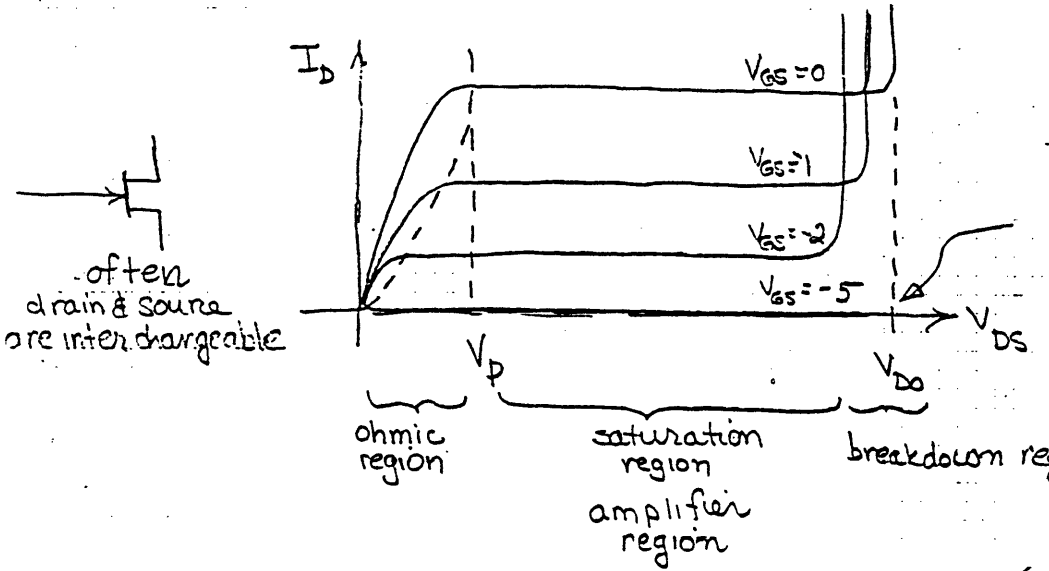


$V_{DS}>V_P$



drawn for $V_{GS} = 0$

As we vary V_{DS} we can generate a family of device curves



If $V_{GS} > 0$ junction is not reverse biased so transistor will not wo

for a constant V_{DS} as V_{GS} becomes more negative it eventually cutsoff the FET.

at cutoff (or pinchoff) for a constant V_{DS} (V_p decreases as V_{GS} decreases

$$V_{DS}(\text{pinchoff}) \approx V_{po} + V_{GS} = V_P$$

V_{po}: pinchoff for zero V_{GS}

V_P: pinchoff voltage

The operation of the junction FET can be mathematically summarized as

1. ohmic region

$$I_D = I_{DSS}\left[2\left(1+\frac{V_{GS}}{V_{po}}\right)\frac{V_{DS}}{V_{po}} - \left(\frac{V_{DS}}{V_{po}}\right)^2\right]$$

for V_{DS} small $\quad I_D \approx \frac{2I_{DSS}}{V_{po}}\left(1+\frac{V_{GS}}{V_{po}}\right)V_{DS}$

looks like a resistor with

$$\frac{1}{r_{DS}} \approx \frac{2I_{DSS}}{V_{po}}\left(1+\frac{V_{GS}}{V_{po}}\right)$$

2. saturation region

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_{po}}\right)^2$$

note: $V_{GS} < 0$

$V_{po} > 0$

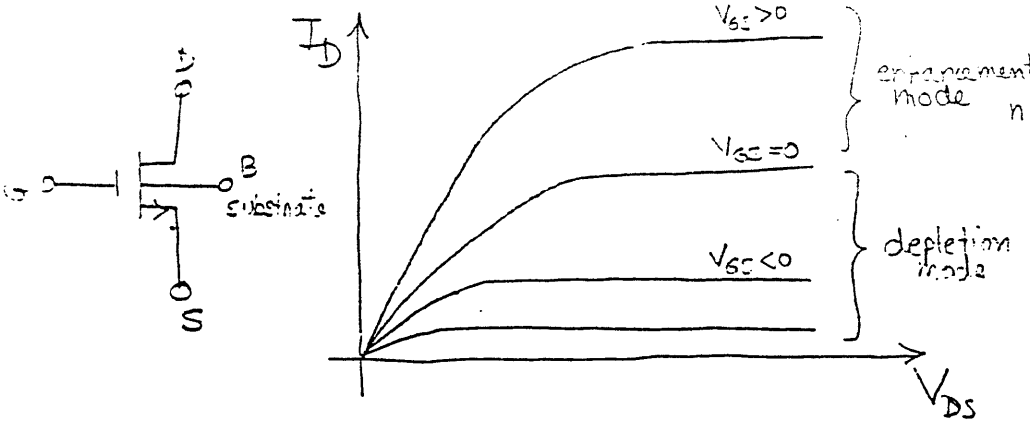
3. cutoff region $\quad I_D = 0$

A transistor manufacturer will often specify the transconductance g_{mo} defined by

$$g_{mo} = \frac{2\, I_{DSS}}{|V_{po}|}$$

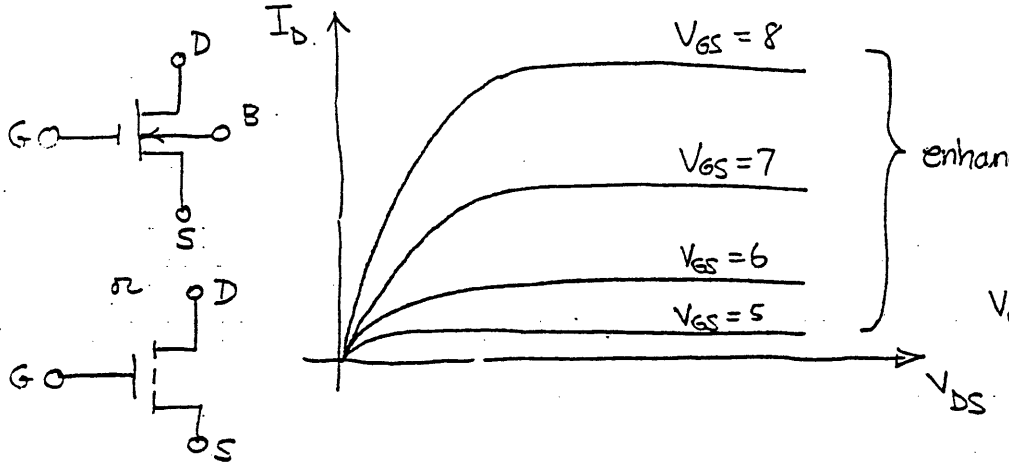
MOSFET

The MOSFET is a special version of the JFET in which a silicon dioxide layer electrically insulates the gate electrode from the rest of the transistor. Basically the MOSFET behaves identically to a JFET. As V_{GS} becomes more negative the minority carriers become depleted and the MOSFET behaves exactly like a JFET. However, because the gate is insulated from the rest of the transistor no p-n junction is formed at the gate and even if V_{GS} becomes <u>POSITIVE</u> no gate current can flow. If V_{GS} becomes positive negative charges are induced in the channel creating an "effective" larger majority carrier concentration. This increases the conductivity of the channel and increases I_D. When $V_{GS} > 0$ the MOSFET is operating in the enhancement mode.



n-channel depletion MOSFET

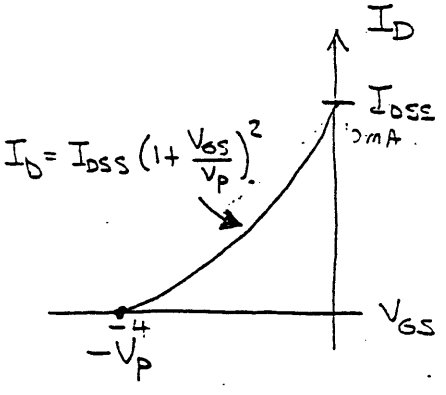
Certain MOSFET's can only operate in the enhancement mode. This is because a channel is formed by the applied field (adding majority carriers) and does not exist when $V_{GS} \leq 0$.



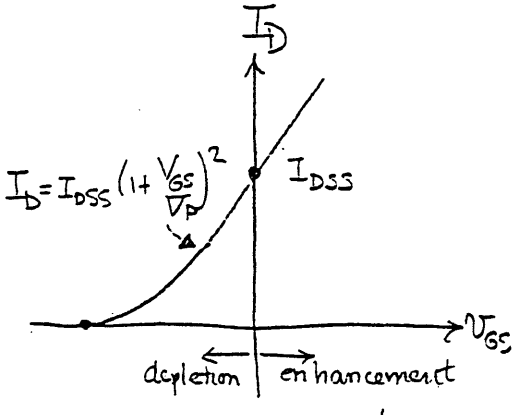
enhancement mode.

V_{GS} at which the channel form is called V_T, the thresho voltage.

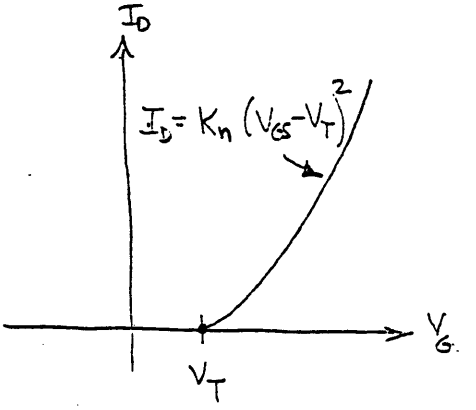
A very common way of displaying FET characteristics is the transfer characteristic curve which plots I_D as a function of V_{GS}, i.e. the output versus the input for a FET.



JFET



enhancement/ depletion MOSFET



enhancement MOSFET

V_T is the threshold voltage

all are n-channel.

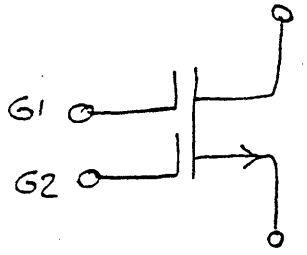
Why use FET's? Their transfer characteristics

A square-law relationship is good for mixers, amplifiers and gain-controlled stages.

$$g_m \triangleq \frac{\Delta I_D}{\Delta V_{GS}}$$ so this is the parameter that will be important.

g_{mo} is also the slope of the transfer characteristic.

Specialized MOSFET – dual gate

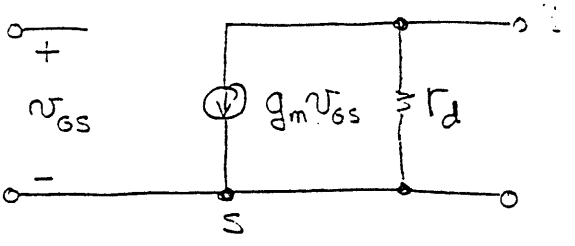


common substrate

very useful for mixers:

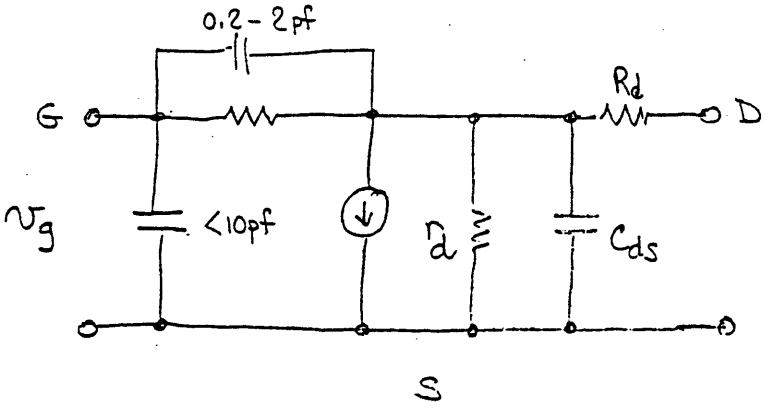
FET small signal model

circuits II (midband) model:

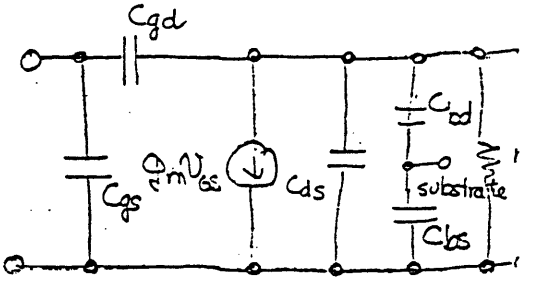


high frequency models:

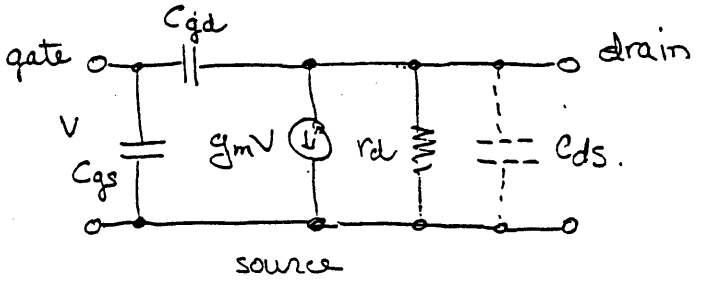
JFET



MOSFET



simplified high frequency π model



C_{gd} feedback capacitance
0.05 − 5 pf

C_{gs} input capacitance
0.1 − 10 pf

r_d effective channel resistance
500 − 5000 Ω

C_{ds} is usually small enough to be neglected.

In general, a FET is NOT better than a BJT at high frequencies

① The input impedance drops rapidly with frequency and quickly becomes reactive for a FET. (Even though the FET still has a somewhat higher impedance this can be made up for by a matching circuit for a B

② A BJT usually has a better power gain.

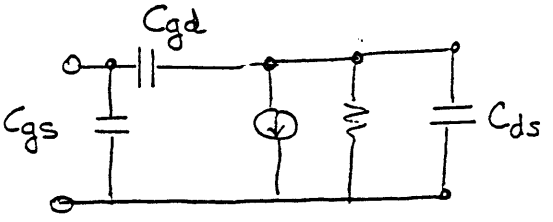
③ The BJT has a larger gain bandwidth product.

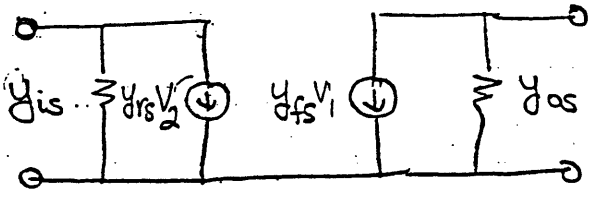
FET data sheets

transconductance $g_{mo} = \frac{2 I_{DSS}}{|V_p|}$

C_{iss}	common source	short-circuit input capacitance
C_{rss}		reverse transfer capacitance
C_{ds}		output capacitance

use π-model



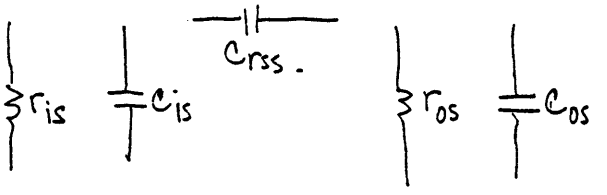


$C_{gd} \approx C_{rss}$ corresponds to C_p.

$C_{gs} \approx C_{iss} - C_{rss}$ input || feedback

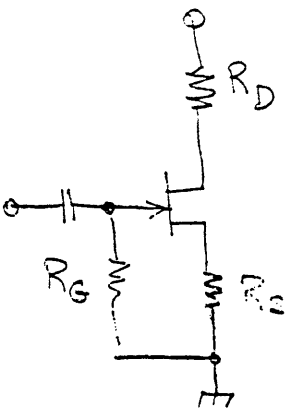
$C_{ds} \approx C_{oss} - C_{rss}$ output || feedback.

i.e.



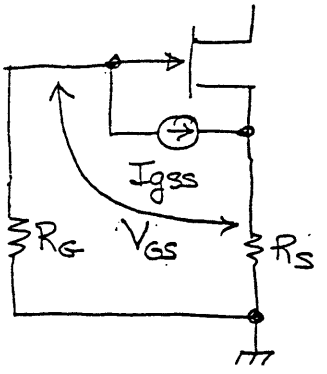
Biasing FET's (p. 19)

simple self-bias circuit



Why does this work?

leakage current I_{gss} thru gate.



use KVL on gate bias circuit.

$$0 = I_{gss} R_G + V_{GS} + (I_{gss} + I_D) R_S$$

usually $I_{gss} \ll I_D$

$$V_{GS} = -\left(I_{gss} R_G + R_S I_D\right)$$

differentiate with respect to I_{gss}

$$\frac{\partial V_{GS}}{\partial I_{GSS}} = -R_G - R_S \frac{\partial I_D}{\partial I_{GSS}}$$

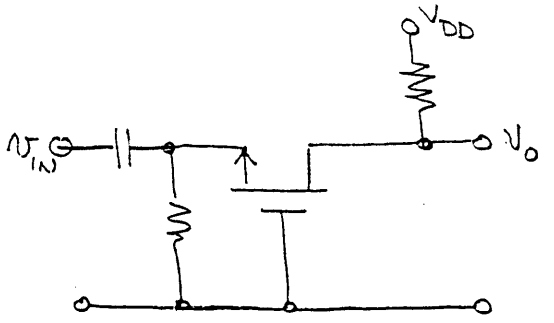
equivalent to stability criteria except for FET's.

$$\text{pick } R_G \leq -R_S \left.\frac{\partial I_D}{\partial I_{gss}}\right|_{max} + \left.\frac{\partial V_{GS}}{\partial I_{DSS}}\right|_{min}$$

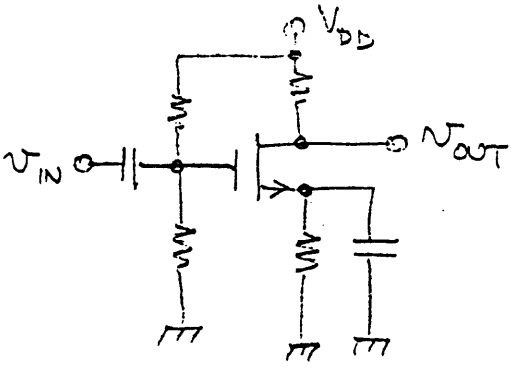
usually $R_G \sim 1 - 1.5 M\Omega$

FET amplifier topologies

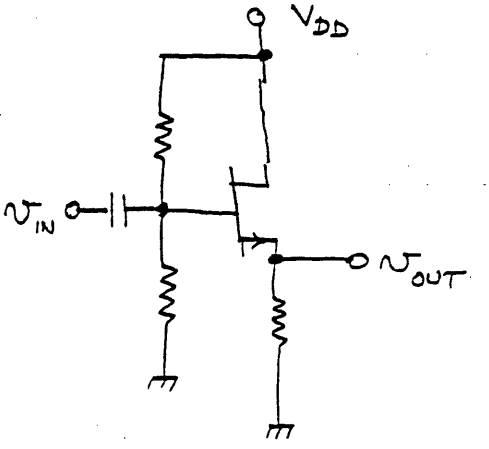
common gate



common source



common drain (source follower)

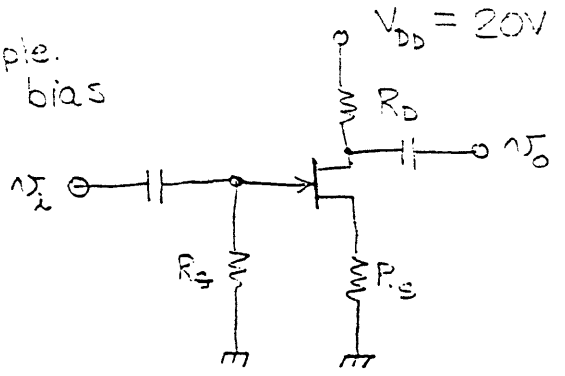


properties of a FET amplifier

	common gate	common source	common drain
R_{IN}	500Ω	∞	∞
R_{OUT}	∞	20kΩ	500Ω
A_v	4	-4	0.80

($g_m = 2 \times 10^{-3}$ ℧, $r_d = 20k\Omega$, $r_L = 2k\Omega$)

Example.
JFET bias



For the JFET shown
$I_{DSS} = 8\,mA$
$V_p = -6V$

Bias at $I_D = 2.0\,mA$, $V_{DS} = 10V$

① Find V_{GS} from transfer characteristic

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_p}\right)^2$$

$$2 = 8\left(1 + \frac{V_{GS}}{+6}\right)^2$$

$$\frac{1}{4} = \left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\pm\frac{1}{2} = 1 + \frac{V_{GS}}{6}$$

$$\frac{1}{6}V_{GS} = -1 + \frac{1}{2}, -1 - \frac{1}{2} = -\frac{1}{2}, -\frac{3}{2}$$

$$V_{GS} = -3, -9$$

↖ beyond Pinchoff

$\Rightarrow V_{GS} = -3$ volts

② Pick $R_G \approx 0.5\,M\Omega$

③ Use KVL at input

$$V_{GS} = -I_G R_G - I_D R_S \approx -I_D R_S$$

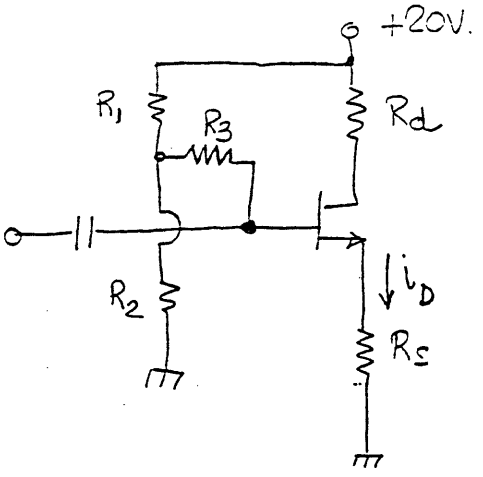
$$R_S \approx -\frac{V_{GS}}{I_D} = \frac{+3}{2\,mA} = 1.5K$$

④ use KVL at output

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

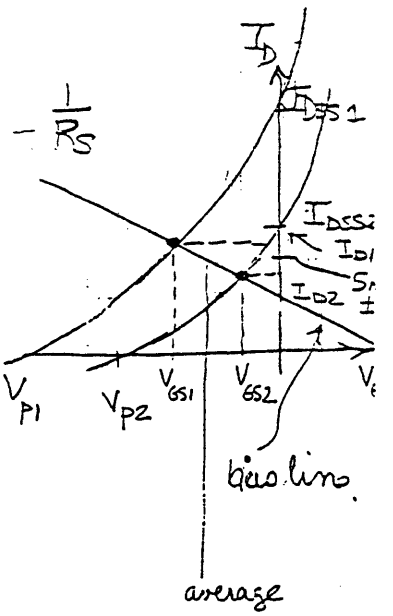
$$R_D = \frac{V_{DD} - V_{DS} - I_S R_S}{I_D} = \frac{20 - 10 - 1.5(2mA)}{2mA} = 3.5K$$

Example: depletion type MOSFET



$4 < V_p < 6$ volts

$8 < I_{DSS} < 10mA$



bias at $I_D = 5mA$, $V_{DS} = 8V$ with ±10% variation in I_D

① use transfer characteristic to get V_{GS}

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

$$\pm\left(1 + \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$V_{GS} = V_P\left(\mp\sqrt{\frac{I_D}{I_{SSS}}} - 1\right)$$

V_{GS} will be a maximum when V_p is a maximum, I_D is a maximum

$$V_{GS} = 6\left(\mp\sqrt{\frac{5.5}{10}} - 1\right) = 6(\mp .74 - 1) = \begin{cases} -1.56 \\ -10.44 \leftarrow \text{below pinch} \end{cases}$$

use 10% variation in I_D.

V_{GS} will be a minimum when V_p is a minimum, I_D is a minimum

$$V_{GS} = 4\left(\mp\sqrt{\frac{4.5}{8}} - 1\right) = 4(\mp .75 - 1) = \begin{cases} -1.0 \\ -7.0 \leftarrow \text{below pinch} \end{cases}$$

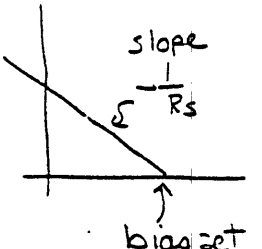
?? ~~volts~~ volts due to parameter variation

② small signal analysis

$$-V_{GS} = V_G - R_S I_D$$

$$I_D = \frac{V_G}{R_S} - \frac{1}{R_S} V_{GS}$$

$\frac{1}{R_S}$ ↖ slope.



$$\therefore \quad R_S = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{-1.55+1.0}{5.5mA-4.5mA} = \frac{-0.55}{1mA} = 550\Omega$$

③ find V_G

$$V_G = V_{GS} + I_D R_S$$

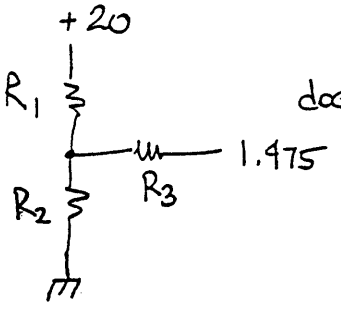
use average $V_{GS} = \frac{-1.55-1.0}{2} = -1.275$

$$V_G = -1.275 + (5\times10^{-3})(550) = +1.475$$

nominal value

④ pick simple voltage divider

pick $R_3 = 500K$ for leakage current



doesn't really matter

pick $R_1 = 100K$

$$\frac{R_2}{R_1+R_2}\,20 = 1.475$$

$$20R_2 = 1.475R_1 + 1.475R_2$$

$$R_2 = \frac{1.475R_1}{18.525} = .0796\,(100K)$$

$$= 7.9K$$

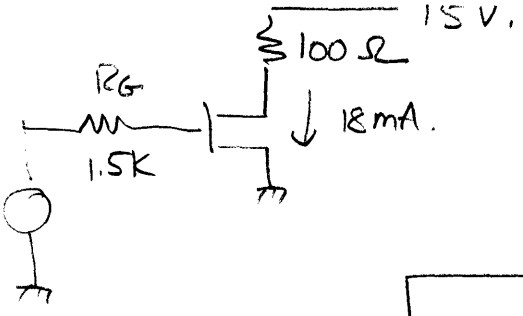
⑤ use KVL at output

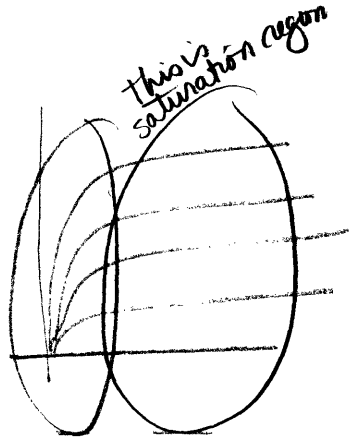
$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

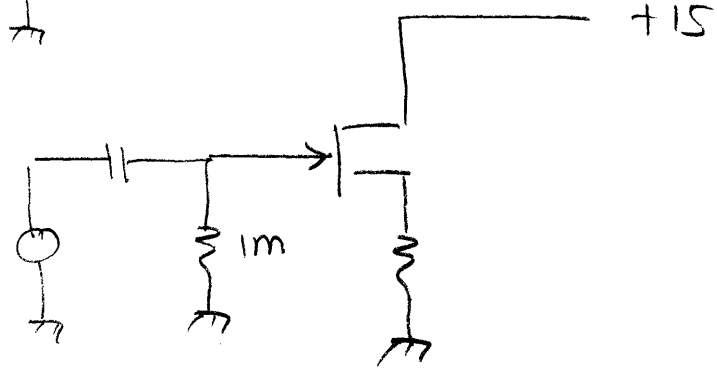
$$20 = (5)R_D + 8V + (5)(550)$$

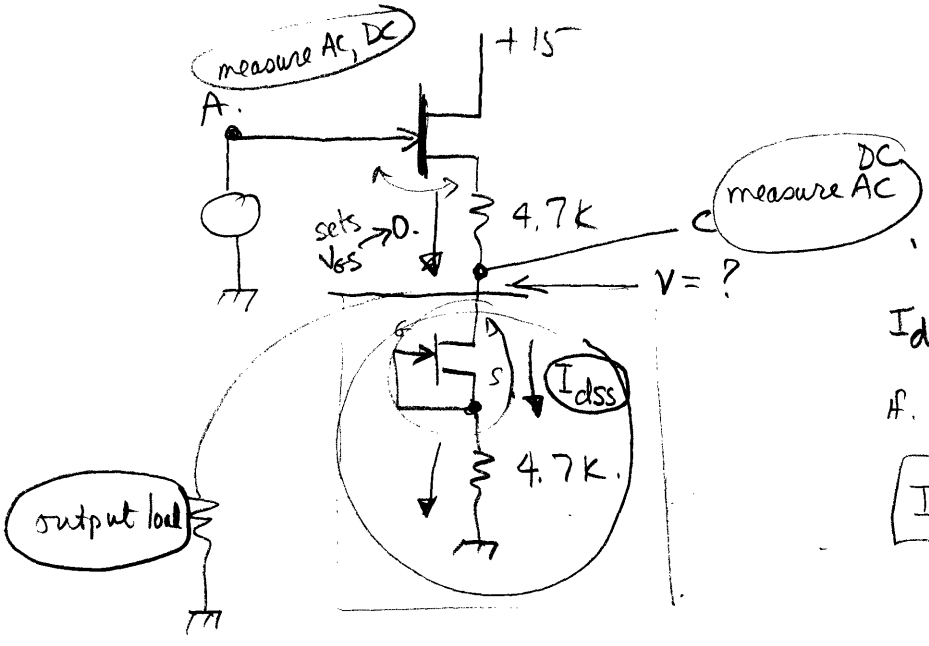
$$R_D = \frac{20-8}{5mA} - 550\Omega = 1850\Omega.$$

part 1.







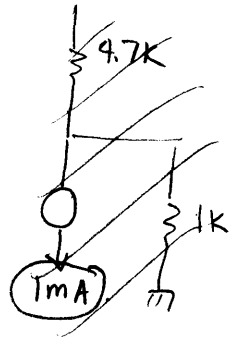


$$I_d = I_{dss}\left(1 - \frac{V_{GS}}{V_p}\right)^2.$$

If $V_{GS} \to 0$.

$$\boxed{I_d = I_{dss}}$$

if the transistors are identical



if $I_d = I_{dss}$
then $V_{GS} \Rightarrow 0$

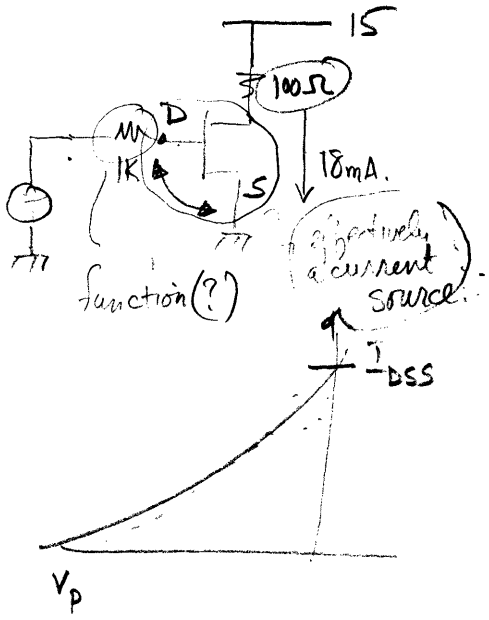
as I_d increases above I_{dss}.

then

$$I_{dss}\left(1 - \frac{V_{GS}}{V_p}\right)^2 I_d > I_{dss}$$

Then $\left(1 - \frac{V_{GS}}{V_p}\right)^2 > 1$

$1 - \frac{V_{GS}}{V_p} > 1$ $\quad \therefore |V_{GS}| > |V_p|$.



$$I_d = I_{dss}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\boxed{I_{dss} = \quad 12 - 18\ mA.}$$

$$g_{fs} = \frac{\text{CS forward transfer conductance.}}{1 - 6.5\ m\ \mho}$$

$$P_d = (.1k)(15) = 1.5 \text{ watts.}$$

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2$$

$$\frac{I_D}{I_{DSS}} = \left(1 - \frac{I_D R_S}{V_p}\right)^2$$

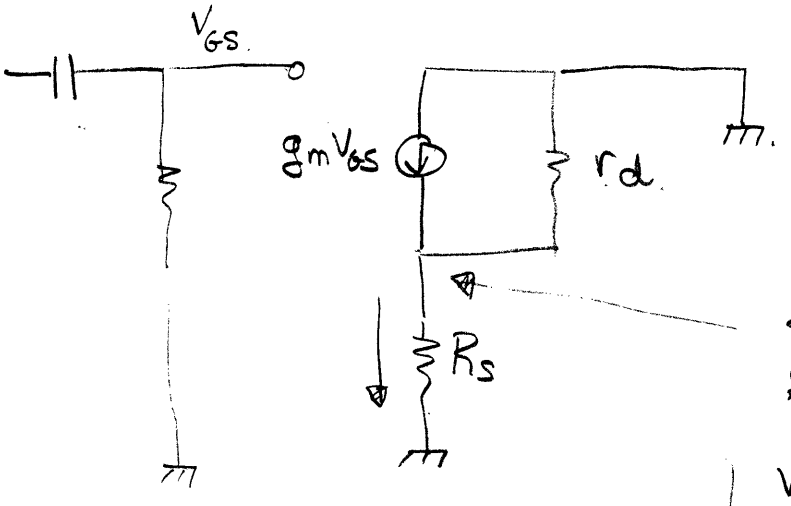
$$\frac{I_D}{I_{DSS}} = 1 - 2\frac{I_D R_S}{V_p} + \frac{I_D^2 R_S^2}{V_p^2}$$

$$I_D^2\left(\frac{R_S}{V_p}\right)^2 - 2\frac{I_D R_S}{V_p} - \frac{I_D}{I_{DSS}} + 1 = 0.$$

$\frac{-b \pm \sqrt{b^2-4ac}}{2a}$

$$I_D = \frac{\left(\frac{2R_S}{V_p} + \frac{1}{I_{DSS}}\right) \pm \sqrt{\left(\frac{2R_S}{V_p} + \frac{1}{I_{DSS}}\right)^2 - 4\left(\frac{R_S}{V_p}\right)^2}}{2\left(\frac{R_S}{V_p}\right)^2}$$

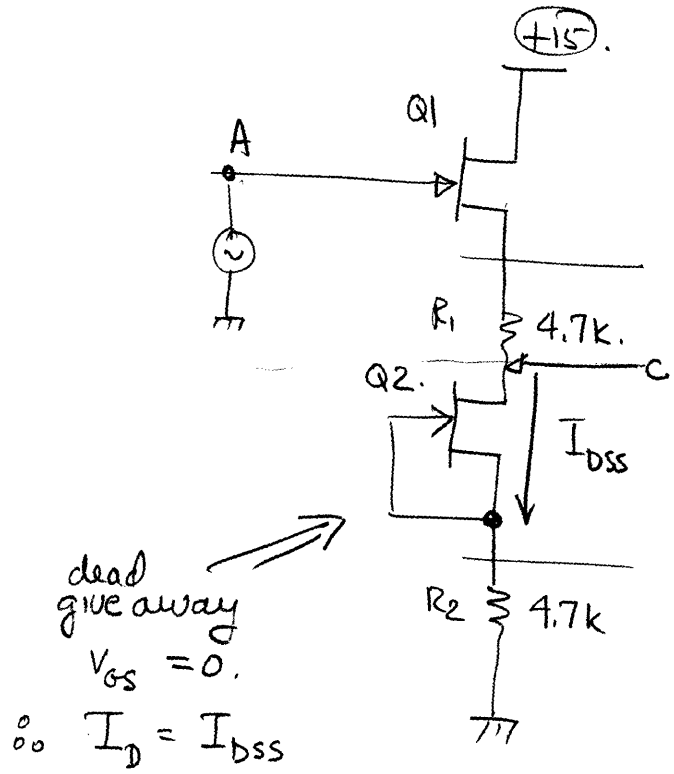
know R_S, V_p and I_{DSS} from transistor characteristics otherwise measure I_D and solve for I_{DSS} or V_p.



$Z_{OUT} \approx R_S$

$Z_{IN} \approx \infty$

$V_{OUT} \approx + g_m R_S$

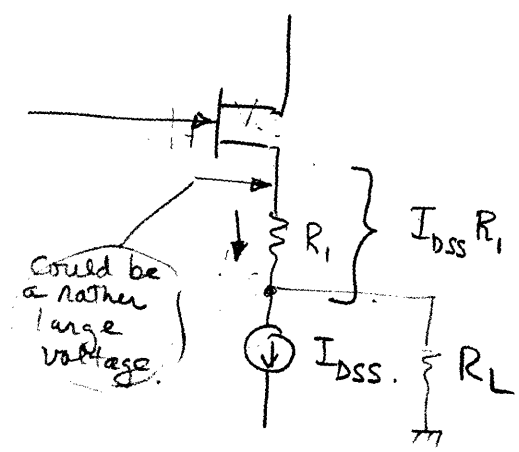


dead give away

$V_{GS} = 0.$

$\therefore I_D = I_{DSS}$

$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

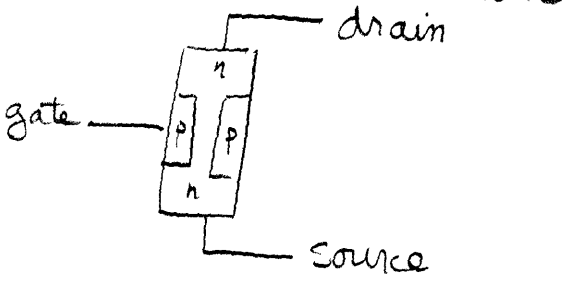


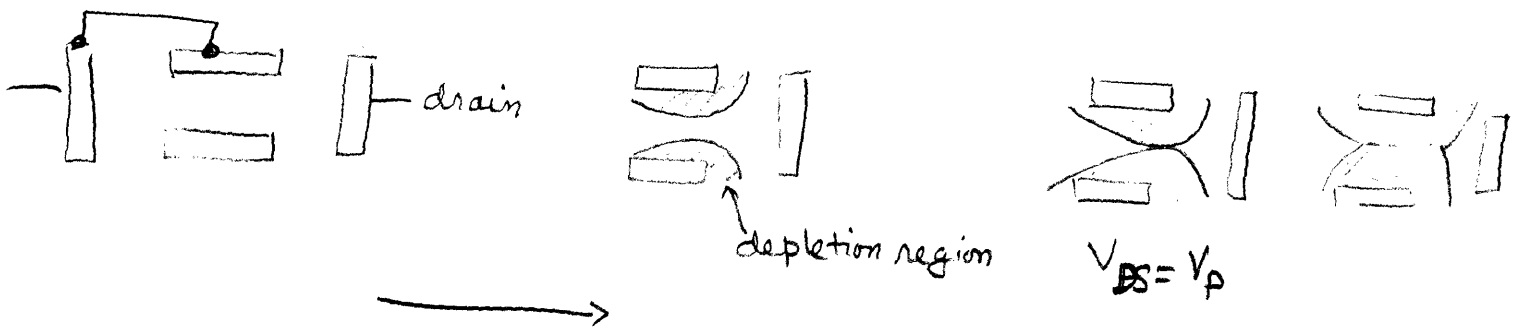
As I add a load resistor

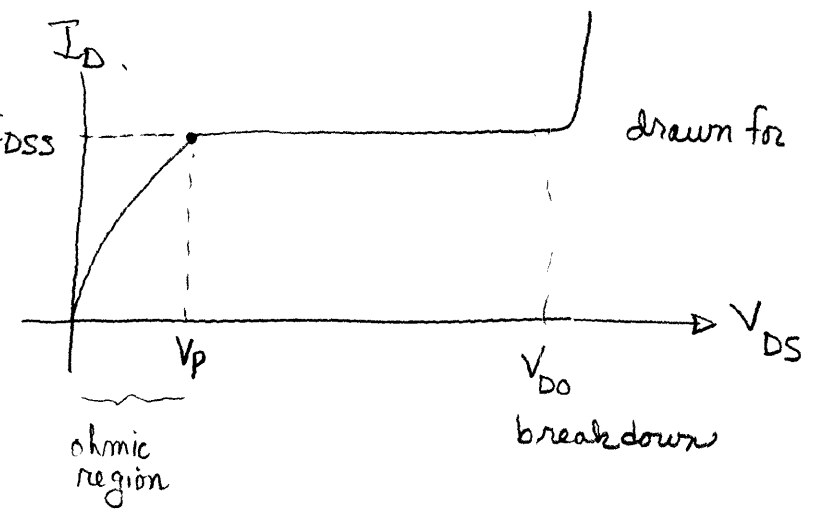
$I_D > I_{DSS}$. for Q2

V_{GS} changes

basic ~~FET~~ characteristic







$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

$$g_m = \frac{2 I_{DSS}}{V_P}$$

V_p & g_{mo} measured at $V_{GS} = 0$.

small signal model.

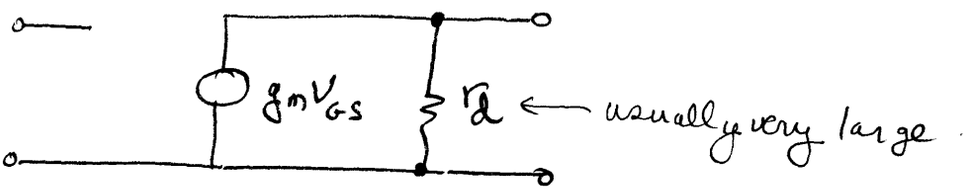
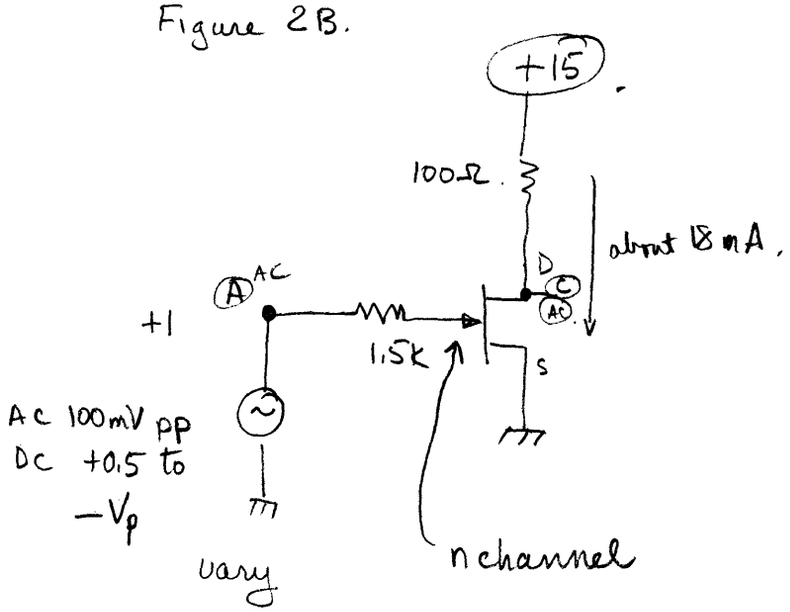
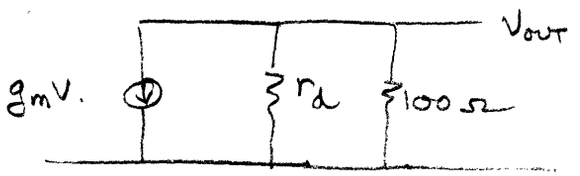


Figure 2B.

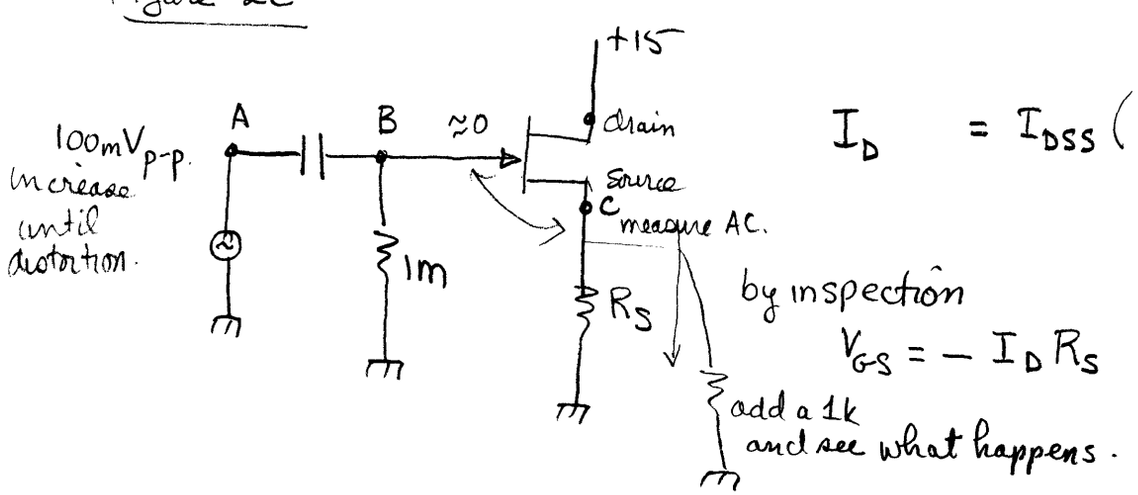




$$V_{out} = -(g_m V_{GS})(100\Omega)$$

$$\frac{V_{out}}{V_{in}} = -g_m R_L$$

Figure 2c



$$I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$$

by inspection

$$V_{GS} = -I_D R_S$$