We report on the experimental investigation and modeling of electrical breakdown in multilayer (a few to tens of nanometers thick) molybdenum disulfide (MoS2) field-effect transistors (FETs). By measuring MoS2 devices ranging from 5.7 nm to 77 nm in thicknesses, we achieve a breakdown current of 1.2 mA, mobility of 42 cm² V⁻¹ s⁻¹, and on/off current ratio I_on/I_off ~ 10⁴. Through measurements and simulations, we find the dependence of the breakdown current limit on MoS2 thicknesses, channel lengths and conductivities. We also explore, both experimentally and analytically, the effects of different device parameters upon carrier mobility, which is directly related to the current carrying capacity. The results suggest that, compared to single-layer devices, multilayer MoS2 FETs could be advantageous for circuit applications requiring higher carrier mobility and power handling capacities.

Ultrathin molybdenum disulfide (MoS2) isolated from its layered bulk material has recently emerged as a new two-dimensional (2D) semiconducting crystal with a wide spectrum of attractive properties – such as lack of dangling bonds, high thermal stability, and thickness-dependent bandgap and band structure. These have led to strong promises for creating new nanodevices beyond graphene, ranging from ultrathin field-effect transistors (FETs) and optoelectronic devices to 2D sensors and transducers, on both rigid and flexible substrates. While prototype single- and few-layer MoS2 FETs, circuits and memory devices have been demonstrated, multilayer (up to tens of nanometers thick) devices are more desirable for certain applications: they are expected to have higher carrier mobility and density of states under the same dielectric environment, higher current limit, and better manufacturability, while occupying similar device footprints as their single- and few-layer counterparts. To date, flexible electronics and gas sensors based on multilayer MoS2 FETs and a small-signal generator based on a multilayer MoS2/graphene heterojunction have already been reported.

The mobility of MoS2 transistors has been studied for a variety of device structures. At room temperature, the measured single-layer MoS2 transistors on the substrate show mobility of 60 cm² V⁻¹ s⁻¹ in vacuum, much less than the theoretical optical-phonon-scattering-limited mobility (410 cm² V⁻¹ s⁻¹). To approach high mobility, high-k dielectric materials (e.g., HfO2, Al2O3) have been adopted to build top-gated devices. It has also been recently noted that some of the reported mobility values from top-gated devices may have been overestimated. In contrast, multilayer MoS2 transistors (a few to tens of nanometers thick) with relatively simple back-gated configuration exhibit mobility values up to 470 cm² V⁻¹ s⁻¹ at room temperature on the PMMA substrate, close to the theoretically predicted phonon scattering limit (200–500 cm² V⁻¹ s⁻¹) for bulk molybdenum disulfide.

To further understand and utilize the unique properties offered by multilayer MoS2 transistors (a few to tens of nanometers thick), we investigate device characteristics such as electrical breakdown limit and electron mobility, focusing on their dependence on device parameters such as MoS2 thickness. Through a series of experimental measurements, analytical calculations, and finite element modeling (FEM), we find that to achieve higher electrical breakdown limit, higher device thickness and channel conductivity are desired. We further examine the difference between single-layer and...
multilayer devices, and illustrate how heat dissipation and current carrying capabilities scale with layer numbers in MoS2 FETs with different device configurations. Multilayer devices can achieve higher mobility and higher current limit than mono- or few-layer MoS2 FETs, and thus can be better suited for certain circuit applications.

The multilayer MoS2 devices are fabricated by mechanically exfoliating MoS2 crystals onto 290 nm-thick SiO2 on Si substrate and patterning electrical contacts using electron-beam lithography (EBL). Contacts are then metallized using electron-beam evaporation followed by lift-off. Fig. 1(a) shows the schematic of our MoS2 transistors and their electrode configurations. During measurements the electrodes are connected to high-precision source measurement units (SMUs) which supply the voltages and measure the currents. During measurements, SMU1 is connected to the back gate (G) and SMU2 is connected to the drain (D). The source (S) electrode is grounded. The thicknesses of the MoS2 layers are measured using an atomic force microscope (AFM). Fig. 1(b)–(d) illustrate the band diagrams of multilayer MoS2 transistors under different operation conditions. Ti (titanium) forms a Schottky contact to MoS2 with a barrier height \( q\psi_B = q\psi_{Ti} - \chi \), where \( q\psi_{Ti} \) is the work function of Ti and \( \chi \) is the electron affinity of MoS2. While the estimated Schottky barrier height for Ti to MoS2 is \( \sim 0.3 \text{ eV} \), in practice \( g\psi_B \) is lowered to around 50 meV due to Fermi level pinning.\(^\dagger\) This suggests that at room temperature, thermally assisted tunneling is the dominant conduction mechanism at the On state (compared to thermionic emission, Fig. 1(c)). When a back gate voltage \( V_G \) higher than the threshold voltage \( V_T \) is applied, the Fermi level \( E_F \) of MoS2 moves closer to the conduction band, narrowing the width of the Schottky barrier and facilitating thermally assisted tunneling between the D and S electrodes.\(^7\) In contrast, if \( V_G < V_T \), \( E_F \) moves away from the conduction band, widening the Schottky barrier, thus suppressing tunneling (the Off state, Fig. 1(d)).

Fig. 2 shows the characterization of two multilayer MoS2 transistors (devices A & B) with Ti/Ni contacts. For device A (thickness \( t \approx 70 \text{ nm} \)), current saturation is observed under a large positive drain bias \( V_D \) (Fig. 2(b)), desirable for field-effect transistors. At positive \( V_G \), the device turns on, and conductance increases with \( V_G \), confirming n-type transistor behavior (Fig. 2(c)–(d)). The off-state leakage current \( I_{off} \) is \( \sim 100 \text{ pA} \), much smaller than the on-state current \( I_{on} \), showing an on/off ratio \( I_{on}/I_{off} \) of \( \sim 10^4 \). From data in Fig. 2(c) we extract the field-effect mobility \( \mu = (dI_d/dV_G) \times [L/W_{ox}V_D] \), where \( L, W, C_{ox} \) are respectively the length, width, and the capacitance per unit area to the back gate of the MoS2 channel. For device A, \( \mu = 42 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \), comparable with other reported devices with similar structures.\(^{16,20,21,23}\) For device B (Fig. 2(e)–(h)), a much thinner device \( (t = 5.7 \text{ nm}) \) also with Ti/Ni contact, we find that \( \mu = 9.9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1} \) and \( I_{on}/I_{off} = 4 \times 10^4 \), again consistent with similar devices.\(^{19,23}\)

Fig. 3 summarizes \( \mu \) and \( I_{on}/I_{off} \) of 10 devices with different thicknesses and contact materials (also shown in Table S1\(^\dagger\)). We observe that thicker MoS2 transistors, in general, exhibit higher mobilities (Fig. 3(a)), consistent with the literature.\(^{18,19,21}\) We model the \( \mu-t \) relation using the Boltzmann transport equation.\(^{12}\) We consider scattering from phonons, charged impurity, boundary, lattice defects, and thickness steps, with phonon scattering including contributions from...
acoustic, polar optical (POP), and homopolar optical (HOP) phonons (effect from surface optical phonon is expected to be negligible in our devices with SiO₂ gate dielectric\textsuperscript{35}). To date, only phonon and impurity scatterings have been analyzed for MoS\textsubscript{2} FETs,\textsuperscript{32,35,36} as the other mechanisms were deemed negligible for single layer devices, which does not necessarily hold for multilayer devices. All these mechanisms have different scattering strengths and thickness dependences. Among them, phonon is the most common scattering source at room temperature, and is expected to be independent of MoS\textsubscript{2} thickness.\textsuperscript{19,32,35,37} Charged impurity scattering is also important, and is thickness dependent.\textsuperscript{36} Electron-boundary, generating less scattering than charged impurity, is also thickness dependent.\textsuperscript{38} Lattice vacancy is the most common (and a native) defect in MoS\textsubscript{2},\textsuperscript{39} and vacancy scattering does not depend on thickness. The calculated vacancy scattering rate is comparable with other scattering mechanisms.\textsuperscript{40} We also include scattering due to thickness steps created in the mechanical exfoliation process, and find it also important.\textsuperscript{41}

Combining contributions from all the mechanisms above, we calculate the total scattering rate ($\tau_{\text{total}}^{-1}$) using the empirical expression:

\[
\frac{1}{\tau_{\text{total}}} = \frac{1}{\tau_{\text{phonon}}} + \beta \frac{1}{\tau_{\text{imp}}} + \frac{1}{\tau_{\text{bdr}}} + \frac{1}{\tau_{\text{va}}} + \frac{1}{\tau_{\text{step}}}
\]

Fig. 2 (a)–(d) Measurement of MoS\textsubscript{2} device A (contact: 3 nm Ti/50 nm Ni). (a) Optical image, AFM image, and the height profile. (b) Transport characteristics. (c) & (d) Transfer curves in linear and logarithmic scales measured at $V_G = 0.1$ V. Red line: field-effect mobility extracted from the slope of the $I_D$–$V_G$ curve. (e)–(h) Measurement of MoS\textsubscript{2} device B (contact: 2 nm Ti/150 nm Ni). The contents of (e)–(h) are in the same sequence as in (a)–(d). The inset of (f) shows linear behavior at small $V_D$. Data in (g) are taken at $V_D = 1$ V.

Fig. 3 Extracted (a) mobility and (b) on/off ratio of devices with different MoS\textsubscript{2} thicknesses and with Ni (solid circles) and Ti/Ni contact (half-filled circles: 290 nm SiO\textsubscript{2}; half-filled squares: 3.5 μm SiO\textsubscript{2}). Magenta, olive and orange lines in (a) show the calculated thickness dependence of mobility from multiple scattering terms with fitting parameters $\beta = 2, 4,$ and 6, respectively.
where the 5 terms represent contributions from phonon, impurity, boundary, vacancy, and step, respectively, with the phonon term further consisting of multiple mechanisms:

\[
\frac{1}{\tau_{\text{phonon}}} = \frac{1}{\tau_{\text{acoustic}}} + \frac{1}{\tau_{\text{POP}}} + \frac{1}{\tau_{\text{HOP}}},
\]

and \(\beta\) is an empirical fitting parameter (see ESI† for details). We find that at small thickness, charged impurity scattering is the main scattering mechanism, and at larger thickness, vacancy scattering and thickness step scattering become dominant. Mobility calculated from this model \(\mu_n = \frac{q\tau_{\text{total}}}{m^*}\) (\(q\): elementary charge, and \(m^*\): electron effective mass) shows good agreement with our data, with thicker devices exhibiting higher mobilities (Fig. 3(a)). Fig. 3(b) shows that typically thinner devices have higher \(I_{\text{on}}/I_{\text{off}}\). Our results illustrate the tradeoff between mobility and on/off ratio in MoS\(_2\) devices, suggesting that choosing proper device thickness can be helpful for achieving the desired performance.

While mobility and on/off ratio are important device parameters for logical circuits, the current carrying limit is critical for applications requiring high current/power. Here, we study electrical breakdown in multilayer MoS\(_2\) devices with different thicknesses (Fig. 4). All the measured devices have 50 nm Ni (nickel) contacts, and we perform annealing in N\(_2\) at 350 °C in vacuum (1 Torr) to improve the MoS\(_2\)–metal contact. We first calibrate the transfer characteristics of the devices, and then perform transport measurements at \(V_G \approx 50\) V to turn on the device, while gradually increasing the range of drain voltage sweeps. As shown in Fig. 4(a), an \(\sim 70\) nm thick MoS\(_2\) device breaks down when \(V_D\) is swept from 0 to 30 V for the second time, at the breakdown current \(I_{\text{BD}} = 1.2\) mA. This is among

---

**Fig. 4** Electrical breakdown of multilayer MoS\(_2\) FETs. AFM images and height profiles are shown for all the devices. (a) \(I_D-V_D\) curve of a 70 nm thick device, showing breakdown at \(I_D \approx 1.2\) mA. (b)–(d) Measurement of three other devices with different thicknesses. Insets: maximum \(I_D\) in subsequent \(V_D\) sweeps with increasing ranges prior to breakdown.
the highest current values reported to date for MoS$_2$ transistors, corresponding to a breakdown current density $J_{BD} = 4.9 \times 10^9$ A m$^{-2}$ (device width $W = 3.5$ μm). In three other devices tested (Fig. 4(b)–(d)), we observe discrete decreases in device conductance after each $V_D$ sweep (Fig. 4(b)–(d), insets). This is consistent with Joule-heating-induced oxidation which has been observed in graphene nanoribbons.$^{29}$

We find that thicker devices exhibit higher breakdown current limit than thinner devices. This suggests that multilayer MoS$_2$ FETs are advantageous compared to single-layer devices by carrying more power while having the same device footprint. We also compare the normalized “per-layer” current-carrying capability between single-layer and multilayer devices. We find that a higher “per-layer” current limit ($1.18 \times 10^6$ A m$^{-1}$) has been reported for single-layer MoS$_2$ FETs$^{30}$ than for the multilayer devices we measure here ($1.76 \times 10^4$ A m$^{-1}$). Besides differences in detailed device structure and parameters, the decrease in “per-layer” current limit is in fact intrinsic to multilayer devices with regular device geometries due to two main reasons, both of which have important implications for designing high-performance devices. First, for devices with conventional, 2D surface contacts, the contact area remains roughly unchanged as the device layer number increases (Fig. 5(a) & (b)), thus limiting the increase in current carrying capability of the device. With such limitations on current injection into the MoS$_2$ channel, it is not meaningful to directly compare the “per-layer” current limit, because different layers do not necessarily carry the same share of electrical current (and thus do not contribute equally to the overall current carrying ability of the multilayer devices). This limitation, however, may be removed if pure 1D edge contacts$^{42}$ are used (Fig. 5(c) & (d)). Therefore, using an edge contact in multilayer MoS$_2$ FETs shall enhance device performance by improving the current injection efficiency. Second, even for devices with pure edge contacts (and each layer may carry and contribute the same amount of electrical current), multilayer devices still have lower breakdown current values than single-layer devices because the efficiency of heat dissipation to the surrounding environment does not scale with the device thickness. It has been shown that heat dissipation to the substrate is the main cooling mechanism in substrate-supported graphene devices$^{29,43}$ (and we expect similar cases in MoS$_2$ devices): while the thermal conductance may be lower at the layered material–substrate interface (compared to the in-plane value), the footprint area (length × width) of a device is usually orders of magnitude larger than its in-plane cross-section area (thickness × width); this determines that the thermal conductance to the substrate dominates (Fig. 5(e)). As a result, while

![Fig. 5 Illustration of electrical current (a–d, orange arrows) and heat flux (e–h, red arrows) in single layer (a, c, e, g) and multilayer (b, d, f, h) MoS$_2$ FETs. (a) and (b) show the electrical current injection at 2D surface contacts to MoS$_2$ channels, while (c) and (d) show the scenario for 1D edge contacts. (e) and (f) illustrate the heat flux in substrate-supported MoS$_2$ devices under Joule heating, while (g) and (h) show that in suspended MoS$_2$ channels.](image-url)
heat generation scales linearly with device layer number (assuming a constant current density), the device’s thermal conductance to its surroundings does not increase proportionally (Fig. 5(f)). This causes the temperature of the device to rise more readily for thicker devices, and is responsible for their relatively lower “per-layer” current density (note that the total breakdown current is still higher) compared with thinner devices. Finally, for fair comparison between multilayer and single-layer devices, with a normalized “per-layer” performance that would directly scale with the number of layers, both of the following conditions are needed: (i) pure 1D edge contacts are ensured in both single-layer and multilayer devices and (ii) substrate effects should be removed or made independent of device thickness. We illustrate, in Fig. 5(g) & (h), that suspended MoS2 FETs with 1D edge contacts will have both electrical conductance and thermal conductance scaling linearly with the number of layers (device thickness), in which performance can be normalized to “per-layer” measures. We note, however, that removal of the substrate in suspended devices also eliminates the large-area, efficient heat dissipation pathway;44 thus suspended MoS2 FETs (regardless of thickness) are expected to have earlier breakdown than their substrate-supported counterparts, and are hence undesirable for applications requiring higher electrical current and thermal budget.

To quantitatively understand the effect of device parameters on Joule heating, thermal dissipation, and consequently the current carrying limit, we perform FEM simulations to study the device breakdown current and voltage with varying MoS2 channel thickness, length, and conductivity (Fig. 6). While our measurements are performed in air, where the MoS2 oxidation rate increases above 400 °C, to study the ultimate device performance we model the process in vacuum, using the ideal device structure illustrated in Fig. 5(f) (substrate supported, with 1D edge contacts). Under Joule heating, MoS2 temperature rises until reaching its melting temperature $T_M$ (1458 K), at which point the device breaks down (Fig. 6(a)). In the simulation, we use a MoS2 thermal conductivity of 34.5 W (m K)$^{-1}$. Consistent with the trend observed in experiments, our FEM results show that thicker MoS2 devices break down at higher currents (Fig. 6(b)), confirming that multilayer devices are better suited for applications that require high current. Longer device channel (large $L$ value) leads to higher voltage and lower current at breakdown (Fig. 6(c)). The breakdown current can also be affected by the electrical conductivity ($\sigma$) of

![FEM simulation of breakdown of MoS2 transistors due to Joule heating. (a) Temperature profile of a 14.3 kΩ FET with MoS2 channel dimension $t = 5$ nm, $L = 5$ μm, $W = 2$ μm, with $V_D = 33$ V. Plotted in (b) & (c) is the maximum temperature in the MoS2 channel, as a function of (b) $I_D$ (for different MoS2 thicknesses), and (c) $V_D$ (for different channel lengths). Horizontal dashed line: $T_M = 1458$ K, the melting temperature of MoS2. (d) $I_{BD}$ as a function of MoS2 thickness for different channel conductivities. Blue squares: experimental data. Inset: $J_{BD}$ as a function of MoS2 conductivity for $t = 5$ nm devices in the dashed oval.](image-url)
the MoS$_2$ channel: when $\sigma$ increases, less Joule heating will be generated for a given current, resulting in higher breakdown current. In practice, both $V_g$ and temperature can affect $\sigma$. Here, we show the $\sigma$ dependence of $I_{BD}$ and $J_{BD}$ (Fig. 6(d)). We find that both $I_{BD}$ (Fig. 6(d)) and $J_{BD}$ (inset) increase with $\sigma$. This suggests that improving device conductance is an effective approach to boost the current carrying and power handling capacity of MoS$_2$ transistors.

In summary, we have studied multilayer MoS$_2$ FETs and their device performance dependence on parameters such as thickness. We have investigated the electrical breakdown of multilayer MoS$_2$ devices. Both experiments and FEM simulations show that multilayer MoS$_2$ transistors possess higher current-carrying capacities. Both experiments and analytic modeling show that multilayer devices exhibit higher mobility compared to mono- or few-layer devices, which contributes to the more conductive channel and higher current limit. Our results suggest that multilayer MoS$_2$ devices outperform their single- or few-layer counterparts in certain aspects, and their performance can be further improved by carefully engineering the devices and contacts.

Acknowledgements

We thank J. Lee, J. Shan, K. He, and I. Martin for helpful discussions and technical support and Y. Wu for help with the illustrations. We acknowledge the support from Case School of Engineering, National Academy of Engineering (NAE)’s Grainer Foundation Frontier of Engineering (FOE) Award (FOE 2013-005), and Case Western Reserve University (CWRU) Provost’s ACES+ Advance Opportunity Award.

References

5 B. Radisavljevic and A. Kis, Nat. Mater., 2013, 12, 815.
33 M. Fuhrer and J. Hone, Nat. Nanotechnol., 2013, 8, 146.
Electrical Breakdown of Multilayer MoS$_2$ Field-Effect Transistors with Thickness-Dependent Mobility

Rui Yang$^1$, Zenghui Wang$^1$, Philip X.-L. Feng$^{1,*}$

$^1$Department of Electrical Engineering & Computer Science, Case School of Engineering
Case Western Reserve University, 10900 Euclid Avenue, Cleveland, OH 44106, USA

1. Experimental Details of Electrical Breakdown Measurements

The multilayer MoS$_2$ devices experience multiple sweeping cycles in the electrical breakdown measurement (as shown in Fig. 4 in the Main Text). In the measurements, we start with smaller sweeping ranges for $V_D$, and then gradually increase the voltage range. We repeat multiple times for each $V_D$ range and observe changes in device characteristics, including breakdown. Figure S1 shows the details of $V_D$ sweeps. We observe in multiple devices (Figs. S1 (c)-(h)) that the current levels gradually decrease with subsequent sweeping cycles. Different breakdown locations on the devices are observed (Fig. S1 insets).

*Corresponding Author. Email: philip.feng@case.edu
**Fig. S1:** $V_D$ sweeps during the electrical breakdown measurement of multilayer MoS$_2$ transistors shown in Fig. 4 in the main text, with (a)-(b) for the device in Fig. 4(a), (c)-(d) for the device in Fig. 4(b), (e)-(f) for the device in Fig. 4(c), and (g)-(h) for the device in Fig. 4(d). The red curves show the final breakdown sweeps. Insets: Optical microscope images before (a,c,e,g) and after (b,d,f,h) the breakdown.
2. Scattering Mechanisms

We model the device mobility dependence on thickness with different scattering mechanisms, and the relaxation time for each scattering mechanism is plotted in Fig. S2 for MoS$_2$ thickness of 2.5nm to 86nm, which corresponds to 4 to 140 layers, using 0.615nm as the layer spacing$^1$. As phonon scattering and charged impurity scattering in MoS$_2$ has been reported elsewhere$^{1,2,3,4,5}$, here we focus on other mechanisms, including boundary scattering (assuming the electron mean free path is on the order of MoS$_2$ thickness)$^6$, vacancy scattering (in calculation we use values of vacancy defect density $n_v=10^{13}\text{cm}^{-2}$, electron density $n_e=10^{12}\text{cm}^{-2}$, and vacancy radius comparable to the lattice constant)$^7$, and thickness step scattering (assuming average step distance of $\sim 1.5\mu\text{m}$, and step height comparable to the single layer thickness)$^8$. We calculate these scattering mechanisms in MoS$_2$ and the results are shown in Fig. S2. The total relaxation time is calculated for different fitting parameters $\beta$ (2, 4, and 6) as shown in the main text.

![Fig. S2](image-url) **Fig. S2**: Relaxation time for different scattering mechanisms with different MoS$_2$ thickness.
3. Details of FEM Simulation for Electrical Breakdown

In the electrical breakdown simulation (as shown in Fig. 6 in the Main Text), we use $\sigma=35000\text{S/m}$ in Figs. 6(a)-(c). In the model we assume the MoS$_2$ extends 1$\mu$m into the contact, with 8k$\Omega$ contact resistance$^9$. The heat is generated in MoS$_2$ channel and contact region and is dissipated to the SiO$_2$ and Si substrate, using thermal conductivity of SiO$_2$ and Si of 1.4W/(m·K) and 130W/(m·K), respectively. The surface of the substrate is held at room temperature (293.15K). The cross-section view of the FEM result (Fig. S3) shows that the heat dissipation into the substrate dominates.

![Fig. S3: The cross-section view of the FEM result of the temperature profile under Joule heating. In simulation the MoS$_2$ has $t=25$nm, $L=5\mu$m, $W=2\mu$m.](image-url)
4. Summary of All the Measured Devices

Table S1: List of measured multilayer MoS$_2$ FETs and the parameters

<table>
<thead>
<tr>
<th>Device ID #</th>
<th>MoS$_2$ Thickness (nm)</th>
<th>SiO$_2$ Substrate Thickness</th>
<th>Contact Materials</th>
<th>Mobility (cm$^2$/V·s)</th>
<th>$I_{on}/I_{off}$ Ratio</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>70.3</td>
<td>290nm</td>
<td>Ti(3nm)/Ni(50nm)</td>
<td>42</td>
<td>10$^4$</td>
<td>Figs. 2(a)-2(d), Highest Mobility</td>
</tr>
<tr>
<td>2</td>
<td>5.7</td>
<td>290nm</td>
<td>Ti(2nm)/Ni(150nm)</td>
<td>9.9</td>
<td>4×10$^6$</td>
<td>Figs. 2(e)-2(h)</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
<td>290nm</td>
<td>Ni(50nm)</td>
<td>18.3</td>
<td>6×10$^4$</td>
<td>Fig. 4(d)</td>
</tr>
<tr>
<td>4</td>
<td>18.4</td>
<td>290nm</td>
<td>Ti(2nm)/Ni(150nm)</td>
<td>6.5</td>
<td>10$^6$</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>55</td>
<td>290nm</td>
<td>Ni(50nm)</td>
<td>38.7</td>
<td>7×10$^4$</td>
<td>Fig. 4(c)</td>
</tr>
<tr>
<td>6</td>
<td>76/22 Step</td>
<td>290nm</td>
<td>Ni(50nm)</td>
<td>2</td>
<td>6×10$^4$</td>
<td>Fig. 4(b)</td>
</tr>
<tr>
<td>7</td>
<td>32</td>
<td>290nm</td>
<td>Ti(5nm)/Ni(100nm)</td>
<td>36.8</td>
<td>10$^7$</td>
<td>Highest $I_{on}/I_{off}$ Ratio</td>
</tr>
<tr>
<td>8</td>
<td>12</td>
<td>290nm</td>
<td>Ti(5nm)/Ni(100nm)</td>
<td>9.8</td>
<td>10$^6$</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>39</td>
<td>3.5μm</td>
<td>Ti(5nm)/Ni(150nm)</td>
<td>31.9</td>
<td>10$^5$</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>7</td>
<td>3.5μm</td>
<td>Ti(5nm)/Ni(70nm)</td>
<td>1.6</td>
<td>10$^3$</td>
<td></td>
</tr>
</tbody>
</table>
References


