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Electrical breakdown of multilayer MoS_2 field-effect transistors with thickness-dependent mobility†

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We report on the experimental investigation and modeling of electrical breakdown in multilayer (a few to tens of nanometers thick) molybdenum disulfide (MoS_2) field-effect transistors (FETs). By measuring MoS_2 devices ranging from 5.7 nm to 77 nm in thicknesses, we achieve a breakdown current of 1.2 mA, mobility of 42 $cm^2\ V^{-1}\ s^{-1}$, and on/off current ratio $I_{On}/I_{Off} \sim 10^7$. Through measurements and simulations, we find the dependence of the breakdown current limit on MoS_2 thicknesses, channel lengths and conductivities. We also explore, both experimentally and analytically, the effects of different device parameters upon carrier mobility, which is directly related to the current carrying capacity. The results suggest that, compared to single-layer devices, multilayer MoS_2 FETs could be advantageous for circuit applications requiring higher carrier mobility and power handling capacities.

Ultrathin molybdenum disulfide (MoS_2) isolated from its layered bulk material has recently emerged as a new two-dimensional (2D) semiconducting crystal with a wide spectrum of attractive properties – such as lack of dangling bonds, high thermal stability, and thickness-dependent bandgap and band structure.[1,2] These have led to strong promises for creating new nanodevices beyond graphene,[3] ranging from ultrathin field-effect transistors (FETs) and optoelectronic devices to 2D sensors and transducers, on both rigid and flexible substrates. While prototype single- and few-layer MoS_2 FETs,[4–11] circuits[12–14] and memory devices[15] have been demonstrated, multilayer (up to tens of nanometers thick) devices[16–24] are more desirable for certain applications: they are expected to have higher carrier mobility and density of states under the same dielectric environment, higher current limit, and better manufacturability, while occupying similar device footprints as their single- and few-layer counterparts. To date, flexible electronics[25,26] and gas sensors[27] based on multilayer MoS_2 FETs and a small-signal generator based on a multilayer MoS_2/graphene heterojunction[28] have already been reported.

The maximum current and current density of a transistor determine the power it can handle, which is important for designing integrated circuits.[29] While initial exploration of electrical breakdown in single-layer MoS_2 transistors has been reported,[30] the current limit in multilayer devices remains to be investigated. A number of device parameters can affect this limit, such as the dimensions and conductivity of the transistor channel. A highly conductive channel is desirable, as it leads to less Joule heating under a given electric current. This further leads to the open challenge of obtaining high electron mobility in MoS_2 transistors.

The mobility of MoS_2 transistors has been studied for a variety of device structures.[1,3] At room temperature, the measured single-layer MoS_2 transistors on the substrate show mobility of 60 $cm^2\ V^{-1}\ s^{-1}$ in vacuum,[31] much less than the theoretical optical-phonon-scattering-limited mobility (410 $cm^2\ V^{-1}\ s^{-1}$).[32] To approach high mobility, high-κ dielectric materials (*e.g.*, HfO_2, Al_2O_3) have been adopted to build top-gated devices.[4,5,13,14,17] It has also been recently noted that some of the reported mobility values from top-gated devices may have been overestimated.[33] In contrast, multilayer MoS_2 transistors (a few to tens of nanometers thick)[34] with relatively simple back-gated configuration exhibit mobility values up to 470 $cm^2\ V^{-1}\ s^{-1}$ at room temperature[22] on the PMMA substrate, close to the theoretically predicted phonon scattering limit (200–500 $cm^2\ V^{-1}\ s^{-1}$) for bulk molybdenum disulfide.[4]

To further understand and utilize the unique properties offered by multilayer MoS_2 transistors (a few to tens of nanometers thick), we investigate device characteristics such as electrical breakdown limit and electron mobility, focusing on their dependence on device parameters such as MoS_2 thickness. Through a series of experimental measurements, analytical calculations, and finite element modeling (FEM), we find that to achieve higher electrical breakdown limit, higher device thickness and channel conductivity are desired. We further examine the difference between single-layer and

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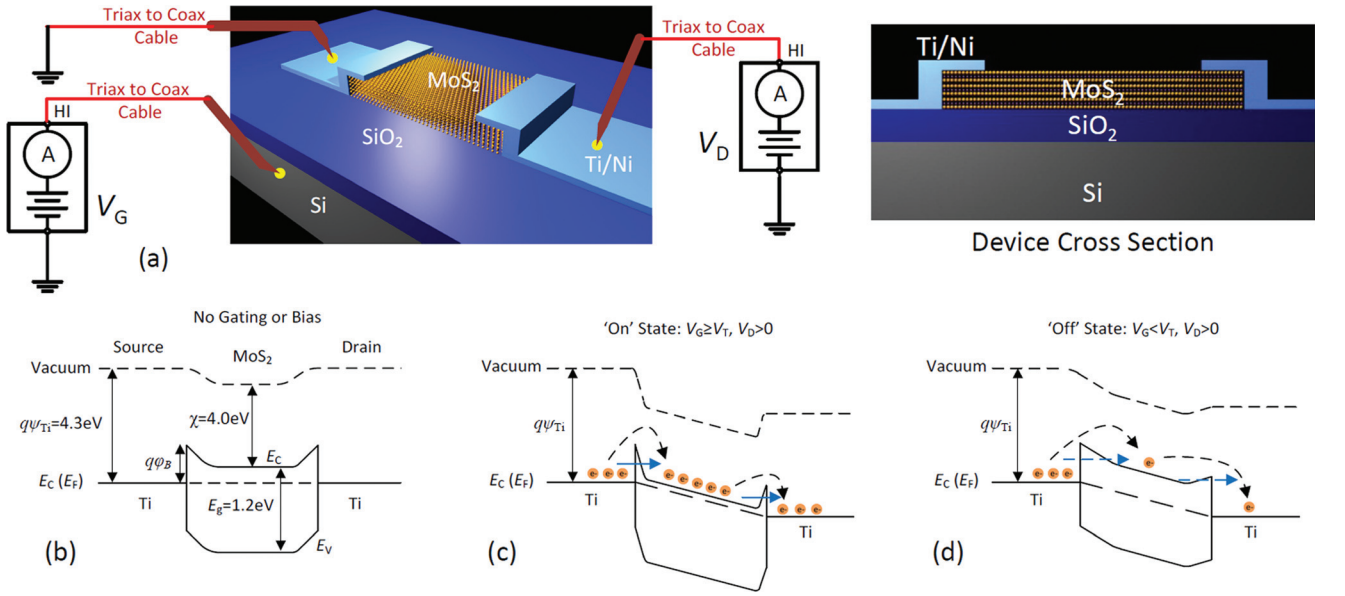

Fig. 1 Schematic of the device geometry, measurement setup, and working principle for multilayer MoS_2 FETs. (a) 3D illustration of a multilayer MoS_2 transistor with electrical connections, and cross-sectional view of the device. (b)–(d) Band diagrams of MoS_2 and contacting metal under different gate and drain biases, including (b) equilibrium, (c) 'On' state and (d) 'Off' state. *Blue arrows*: thermally assisted carrier tunneling. *Black arrows*: thermionic emission. Solid arrows indicate high-probability events, and dashed arrows show the opposite. All schematics are not drawn to scale.

multilayer devices, and illustrate how heat dissipation and current carrying capabilities scale with layer numbers in MoS_2 FETs with different device configurations. Multilayer devices can achieve higher mobility and higher current limit than mono- or few-layer MoS_2 FETs, and thus can be better suited for certain circuit applications.

The multilayer MoS_2 devices are fabricated by mechanically exfoliating MoS_2 crystals onto 290 nm-thick SiO_2 on Si substrate and patterning electrical contacts using electron-beam lithography (EBL). Contacts are then metallized using electron-beam evaporation followed by lift-off. Fig. 1(a) shows the schematic of our MoS_2 transistors and their electrode configurations. During measurements the electrodes are connected to high-precision source measurement units (SMUs) which supply the voltages and measure the currents. During measurements, SMU1 is connected to the back gate (G) and SMU2 is connected to the drain (D). The source (S) electrode is grounded. The thicknesses of the MoS_2 layers are measured using an atomic force microscope (AFM). Fig. 1(b)–(d) illustrate the band diagrams of multilayer MoS_2 transistors under different operation conditions. Ti (titanium) forms a Schottky contact to MoS_2 with a barrier height $q\phi_B = q\psi_{Ti} - \chi$, where $q\psi_{Ti}$ is the work function of Ti and χ is the electron affinity of MoS_2. While the estimated Schottky barrier height for Ti to MoS_2 is ~0.3 eV, in practice $q\Phi_B$ is lowered to around 50 meV due to Fermi level pinning.[18] This suggests that at room temperature, thermally assisted tunneling is the dominant conduction mechanism at the On state (compared to thermionic emission, Fig. 1(c)). When a back gate voltage V_G higher than the threshold voltage V_T is applied, the Fermi level E_F of MoS_2 moves closer to the conduction band, narrowing the width of the Schottky barrier and facilitating thermally assisted tunneling between the D and S electrodes.[7] In contrast, if $V_G < V_T$, E_F moves away from the conduction band, widening the Schottky barrier, thus suppressing tunneling (the Off state, Fig. 1(d)).

Fig. 2 shows the characterization of two multilayer MoS_2 transistors (devices A & B) with Ti/Ni contacts. For device A (thickness $t \approx 70$ nm), current saturation is observed under a large positive drain bias V_D (Fig. 2(b)), desirable for field-effect transistors. At positive V_G, the device turns on, and conductance increases with V_G, confirming n-type transistor behavior (Fig. 2(c)–(d)). The off-state leakage current I_{Off} is ~100 pA, much smaller than the on-state current I_{On}, showing an on/off ratio (I_{On}/I_{Off}) of ~10^4. From data in Fig. 2(c) we extract the field-effect mobility $\mu = (dI_D/dV_G) \times [L/(WC_{ox}V_D)]$, where L, W, C_{ox} are respectively the length, width, and the capacitance per unit area to the back gate of the MoS_2 channel. For device A, $\mu = 42$ cm^2 V^{-1} s^{-1}, comparable with other reported devices with similar structures.[16,20,21,23] For device B (Fig. 2(e)–(h)), a much thinner device ($t = 5.7$ nm) also with Ti/Ni contact, we find that $\mu = 9.9$ cm^2 V^{-1} s^{-1} and $I_{On}/I_{Off} = 4 \times 10^6$, again consistent with similar devices.[19–23]

Fig. 3 summarizes μ and I_{On}/I_{Off} of 10 devices with different thicknesses and contact materials (also shown in Table S1†). We observe that thicker MoS_2 transistors, in general, exhibit higher mobilities (Fig. 3(a)), consistent with the literature.[18,19,21] We model the μ–t relation using the Boltzmann transport equation.[32] We consider scattering from phonons, charged impurity, boundary, lattice defects, and thickness steps, with phonon scattering including contributions from

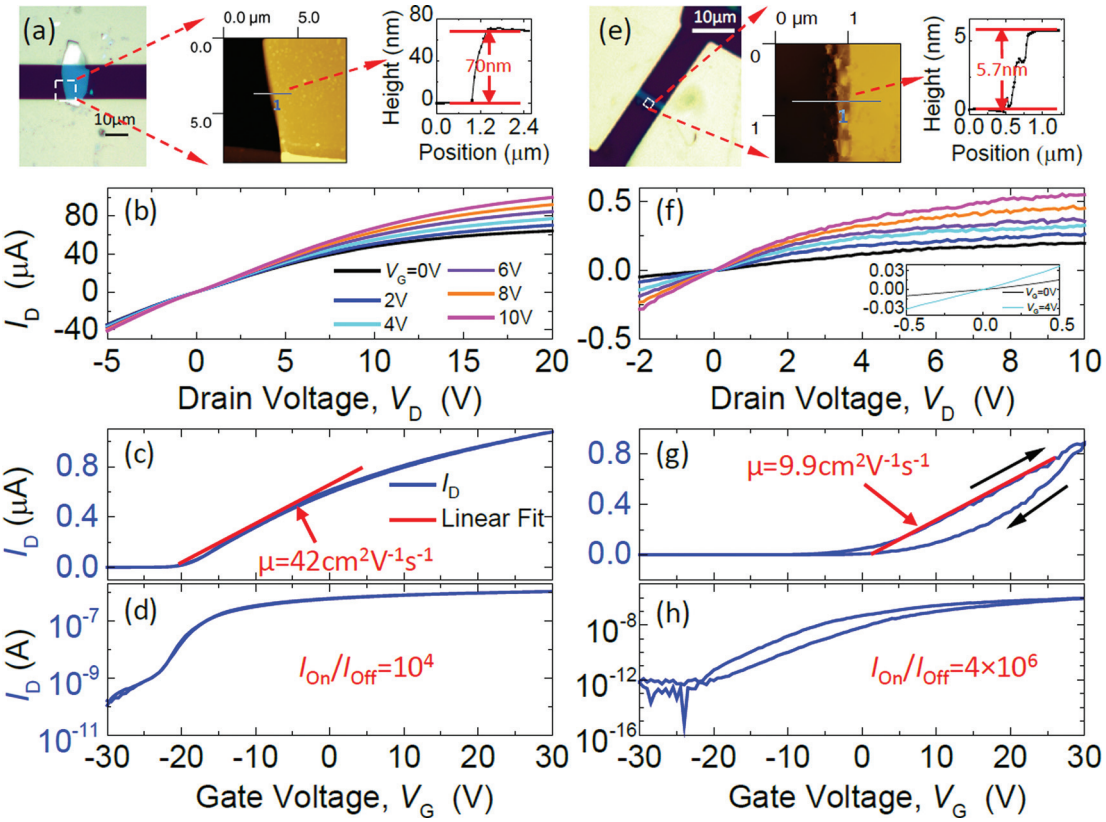

Fig. 2 (a)–(d) Measurement of MoS_2 device A (contact: 3 nm Ti/50 nm Ni). (a) Optical image, AFM image, and the height profile. (b) Transport characteristics. (c) & (d) Transfer curves in linear and logarithmic scales measured at V_D = 0.1 V. *Red line*: field-effect mobility extracted from the slope of the I_D–V_G curve. (e)–(h) Measurement of MoS_2 device B (contact: 2 nm Ti/150 nm Ni). The contents of (e)–(h) are in the same sequence as in (a)–(d). The inset of (f) shows linear behavior at small V_D. Data in (g) are taken at V_D = 1 V.

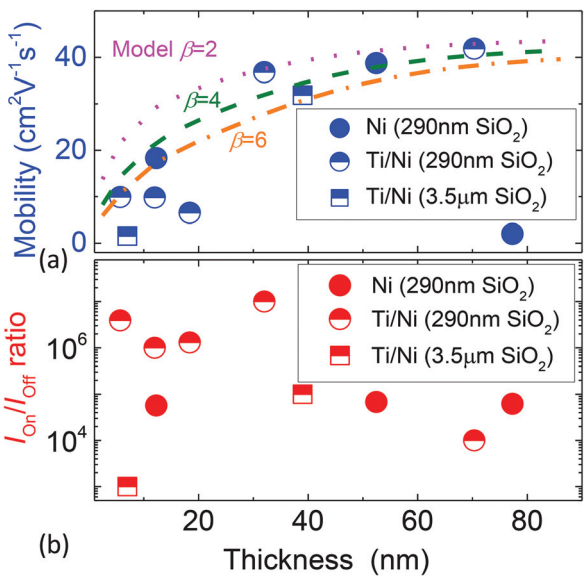

Fig. 3 Extracted (a) mobility and (b) on/off ratio of devices with different MoS_2 thicknesses and with Ni (solid circles) and Ti/Ni contact (half-filled circles: 290 nm SiO_2; half-filled squares: 3.5 μm SiO_2). Magenta, olive and orange lines in (a) show the calculated thickness dependence of mobility from multiple scattering terms with fitting parameters β = 2, 4, and 6, respectively.

acoustic, polar optical (POP), and homopolar optical (HOP) phonons (effect from surface optical phonon is expected to be negligible in our devices with SiO_2 gate dielectric[35]). To date, only phonon and impurity scatterings have been analyzed for MoS_2 FETs,[32,35,36] as the other mechanisms were deemed negligible for single layer devices, which does not necessarily hold for multilayer devices. All these mechanisms have different scattering strengths and thickness dependences. Among them, phonon is the most common scattering source at room temperature, and is expected to be independent of MoS_2 thickness.[19,32,35,37] Charged impurity scattering is also important, and is thickness dependent.[36] Electron-boundary, generating less scattering than charged impurity, is also thickness dependent.[38] Lattice vacancy is the most common (and a native) defect in MoS_2,[39] and vacancy scattering does not depend on thickness. The calculated vacancy scattering rate is comparable with other scattering mechanisms.[40] We also include scattering due to thickness steps created in the mechanical exfoliation process, and find it also important.[41]

Combining contributions from all the mechanisms above, we calculate the total scattering rate $(\tau_{total})^{-1}$ using the empirical expression: $\frac{1}{\tau_{total}} = \frac{1}{\tau_{phonon}} + \beta \frac{1}{\tau_{imp}} + \frac{1}{\tau_{bdr}} + \frac{1}{\tau_{va}} + \frac{1}{\tau_{step}}$,

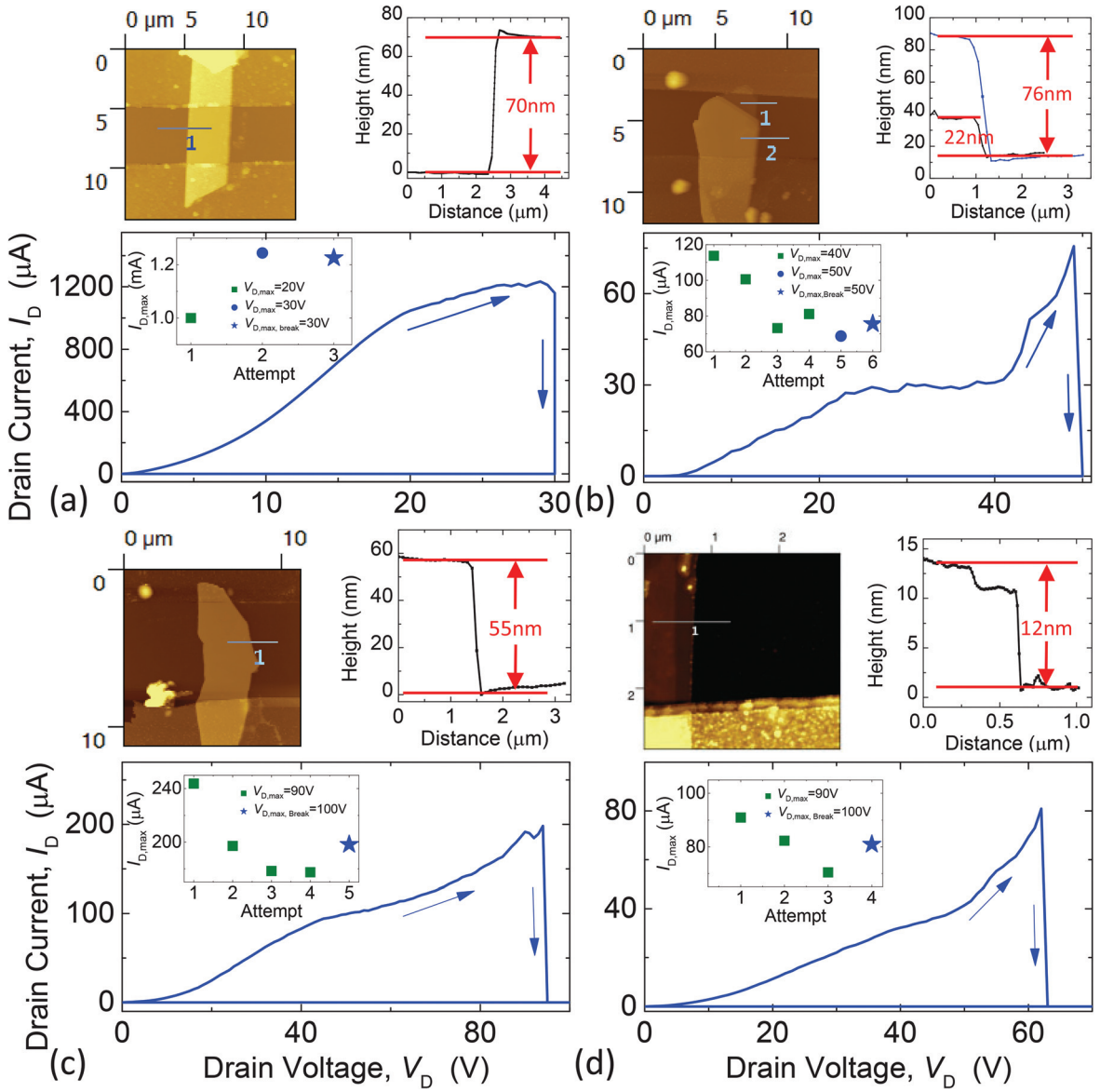

Fig. 4 Electrical breakdown of multilayer MoS_2 FETs. AFM images and height profiles are shown for all the devices. (a) I_D–V_D curve of a 70 nm thick device, showing breakdown at $I_D \approx 1.2$ mA. (b)–(d) Measurement of three other devices with different thicknesses. *Insets*: maximum I_D in subsequent V_D sweeps with increasing ranges prior to breakdown.

where the 5 terms represent contributions from phonon, impurity, boundary, vacancy, and step, respectively, with the phonon term further consisting of multiple mechanisms: $\frac{1}{\tau_{phonon}} = \frac{1}{\tau_{acoustic}} + \frac{1}{\tau_{POP}} + \frac{1}{\tau_{HOP}}$, and β is an empirical fitting parameter (see ESI† for details). We find that at small thickness, charged impurity scattering is the main scattering mechanism, and at larger thickness, vacancy scattering and thickness step scattering become dominant. Mobility calculated from this model $\mu_n = \frac{q\tau_{total}}{m^*}$ (q: elementary charge, and m^*: electron effective mass) shows good agreement with our data, with thicker devices exhibiting higher mobilities (Fig. 3(a)). Fig. 3(b) shows that typically thinner devices have higher I_{On}/I_{Off}. Our results illustrate the tradeoff between mobility and on/off ratio in MoS_2 devices, suggesting that choosing proper device thickness can be helpful for achieving the desired performance.

While mobility and on/off ratio are important device parameters for logical circuits, the current carrying limit is critical for applications requiring high current/power. Here, we study electrical breakdown in multilayer MoS_2 devices with different thicknesses (Fig. 4). All the measured devices have 50 nm Ni (nickel) contacts, and we perform annealing in N_2 at 350 °C in vacuum (1 Torr) to improve the MoS_2–metal contact. We first calibrate the transfer characteristics of the devices, and then perform transport measurements at $V_G \approx 50$ V to turn on the device, while gradually increasing the range of drain voltage sweeps. As shown in Fig. 4(a), an ~70 nm thick MoS_2 device breaks down when V_D is swept from 0 to 30 V for the second time, at the breakdown current I_{BD} = 1.2 mA. This is among

the highest current values reported to date for MoS_2 transistors, corresponding to a breakdown current density $J_{BD} = 4.9 \times 10^9$ A m^{-2} (device width $W = 3.5$ μm). In three other devices tested (Fig. 4(b)–(d)), we observe discrete decreases in device conductance after each V_D sweep (Fig. 4(b)–(d), insets). This is consistent with Joule-heating-induced oxidation which has been observed in graphene nanoribbons.[29]

We find that thicker devices exhibit higher breakdown current limit than thinner devices. This suggests that multilayer MoS_2 FETs are advantageous compared to single-layer devices by carrying more power while having the same device footprint. We also compare the normalized "per-layer" current-carrying capability between single-layer and multilayer devices. We find that a higher "per-layer" current limit (1.18×10^6 A m^{-1}) has been reported for single-layer MoS_2 FET[30] than for the multilayer devices we measure here (1.76×10^4 A m^{-1}). Besides differences in detailed device structure and parameters, the decrease in "per-layer" current limit is in fact intrinsic to multilayer devices with regular device geometries due to two main reasons, both of which have important implications for designing high-performance devices. First, for devices with conventional, 2D surface contacts, the contact area remains roughly unchanged as the device layer number increases (Fig. 5(a) & (b)), thus limiting the increase in current carrying capability of the device. With such limitations on current injection into the MoS_2 channel, it is not meaningful to directly compare the "per-layer" current limit, because different layers do not necessarily carry the same share of electrical current (and thus do not contribute equally to the overall current carrying ability of the multilayer devices). This limitation, however, may be removed if pure 1D edge contacts[42] are used (Fig. 5(c) & (d)). Therefore, using an edge contact in multilayer MoS_2 FETs shall enhance device performance by improving the current injection efficiency. Second, even for devices with pure edge contacts (and each layer may carry and contribute the same amount of electrical current), multilayer devices still have lower breakdown current values than single-layer devices because the efficiency of heat dissipation to the surrounding environment does not scale with the device thickness. It has been shown that heat dissipation to the substrate is the main cooling mechanism in substrate-supported graphene devices[29,43] (and we expect similar cases in MoS_2 devices): while the thermal conductance may be lower at the layered material–substrate interface (compared to the in-plane value), the footprint area (length × width) of a device is usually orders of magnitude larger than its in-plane cross-section area (thickness × width); this determines that the thermal conductance to the substrate dominates (Fig. 5(e)). As a result, while

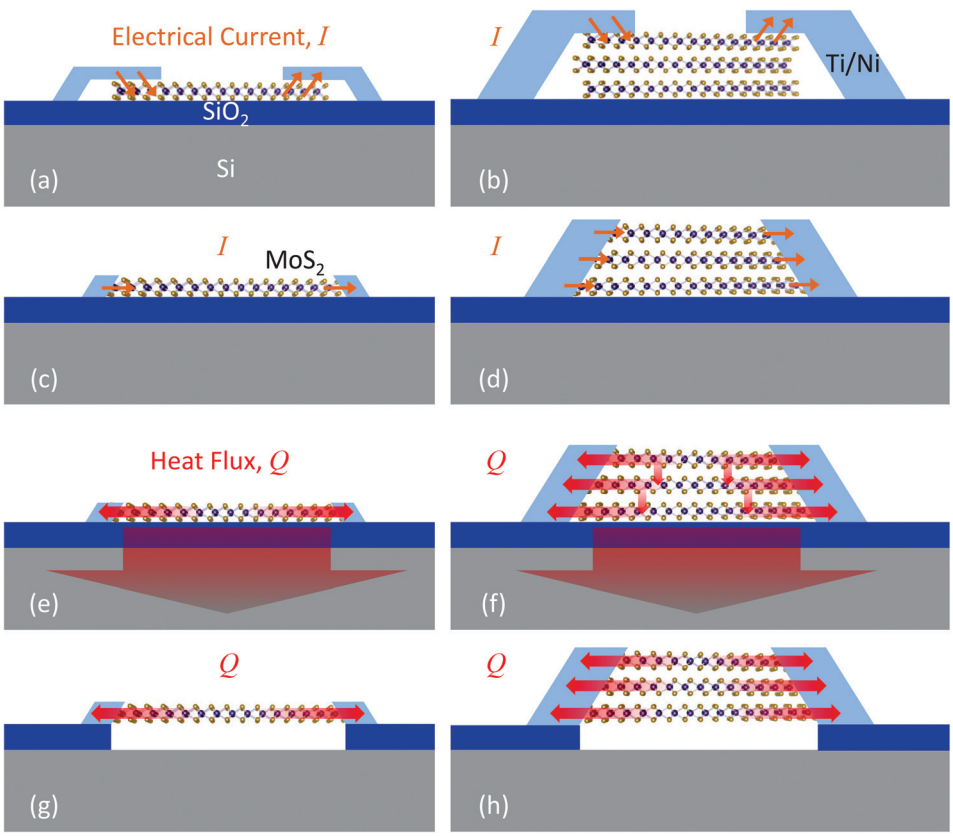

Fig. 5 Illustration of electrical current (a–d, orange arrows) and heat flux (e–h, red arrows) in single layer (a, c, e, g) and multilayer (b, d, f, h) MoS_2 FETs. (a) and (b) show the electrical current injection at 2D surface contacts to MoS_2 channels, while (c) and (d) show the scenario for 1D edge contacts. (e) and (f) illustrate the heat flux in substrate-supported MoS_2 devices under Joule heating, while (g) and (h) show that in suspended MoS_2 channels.

heat generation scales linearly with device layer number (assuming a constant current density), the device's thermal conductance to its surroundings does not increase proportionally (Fig. 5(f)). This causes the temperature of the device to rise more readily for thicker devices, and is responsible for their relatively lower "per-layer" current density (note that the total breakdown current is still higher) compared with thinner devices. Finally, for fair comparison between multilayer and single-layer devices, with a normalized "per-layer" performance that would directly scale with the number of layers, both of the following conditions are needed: (i) pure 1D edge contacts are ensured in both single-layer and multilayer devices and (ii) substrate effects should be removed or made independent of device thickness. We illustrate, in Fig. 5(g) & (h), that suspended MoS_2 FETs with 1D edge contacts will have both electrical conductance and thermal conductance scaling linearly with the number of layers (device thickness), in which performance can be normalized to "per-layer" measures. We note, however, that removal of the substrate in suspended devices also eliminates the large-area, efficient heat dissipation pathway;[44] thus suspended MoS_2 FETs (regardless of thickness) are expected to have earlier breakdown than their substrate-supported counterparts, and are hence undesirable for applications requiring higher electrical current and thermal budget.

To quantitatively understand the effect of device parameters on Joule heating, thermal dissipation, and consequently the current carrying limit, we perform FEM simulations to study the device breakdown current and voltage with varying MoS_2 channel thickness, length, and conductivity (Fig. 6). While our measurements are performed in air, where the MoS_2 oxidation rate increases above 400 °C, to study the ultimate device performance we model the process in vacuum, using the ideal device structure illustrated in Fig. 5(f) (substrate supported, with 1D edge contacts). Under Joule heating, MoS_2 temperature rises until reaching its melting temperature T_M (1458 K), at which point the device breaks down (Fig. 6(a)). In the simulation, we use a MoS_2 thermal conductivity of 34.5 W (m K)$^{-1}$.[45] Consistent with the trend observed in experiments, our FEM results show that thicker MoS_2 devices break down at higher currents (Fig. 6(b)), confirming that multilayer devices are better suited for applications that require high current. Longer device channel (large L value) leads to higher voltage and lower current at breakdown (Fig. 6(c)). The breakdown current can also be affected by the electrical conductivity (σ) of

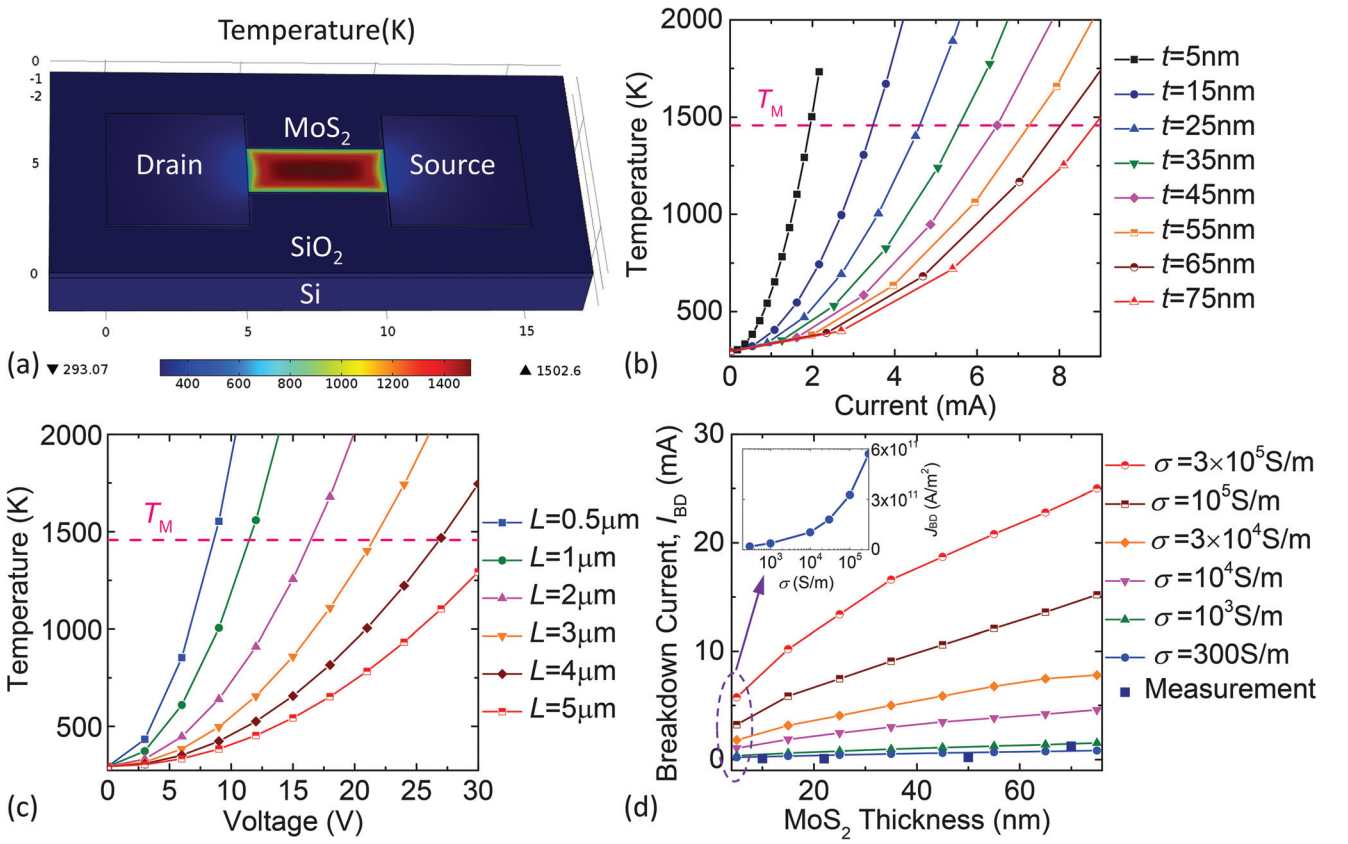

Fig. 6 FEM simulation of breakdown of MoS_2 transistors due to Joule heating. (a) Temperature profile of a 14.3 kΩ FET with MoS_2 channel dimension t = 5 nm, L = 5 μm, W = 2 μm, with V_D = 33 V. Plotted in (b) & (c) is the maximum temperature in the MoS_2 channel, as a function of (b) I_D (for different MoS_2 thicknesses), and (c) V_D (for different channel lengths). *Horizontal dashed line*: T_M = 1458 K, the melting temperature of MoS_2. (d) I_{BD} as a function of MoS_2 thickness for different channel conductivities. *Blue squares*: experimental data. *Inset*: J_{BD} as a function of MoS_2 conductivity for t = 5 nm devices (in the dashed oval).

the MoS_2 channel: when σ increases, less Joule heating will be generated for a given current, resulting in higher breakdown current. In practice, both V_G and temperature can affect σ. Here, we show the σ dependence of I_{BD} and J_{BD} (Fig. 6(d)). We find that both I_{BD} (Fig. 6(d)) and J_{BD} (inset) increase with σ. This suggests that improving device conductance is an effective approach to boost the current carrying and power handling capacity of MoS_2 transistors.

In summary, we have studied multilayer MoS_2 FETs and their device performance dependence on parameters such as thickness. We have investigated the electrical breakdown of multilayer MoS_2 devices. Both experiments and FEM simulations show that multilayer MoS_2 transistors possess higher current-carrying capacities. Both experiments and analytic modeling show that multilayer devices exhibit higher mobility compared to mono- or few-layer devices, which contributes to the more conductive channel and higher current limit. Our results suggest that multilayer MoS_2 devices outperform their single- or few-layer counterparts in certain aspects, and their performance can be further improved by carefully engineering the devices and contacts.

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References

1 Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman and M. S. Strano, *Nat. Nanotechnol.*, 2012, **7**, 699.
2 Y. Yoon, K. Ganapathi and S. Salahuddin, *Nano Lett.*, 2011, **11**, 3768.
3 D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks and M. C. Hersam, *ACS Nano*, 2014, **8**, 1102.
4 B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, *Nat. Nanotechnol.*, 2011, **6**, 147.
5 B. Radisavljevic and A. Kis, *Nat. Mater.*, 2013, **12**, 815.
6 B. W. H. Baugher, H. O. H. Churchill, Y. Yang and P. Jarillo-Herrero, *Nano Lett.*, 2013, **13**, 4212.
7 H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou and P. D. Ye, *ACS Nano*, 2014, **8**, 1031.
8 H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo and A. Javey, *Nano Lett.*, 2013, **13**, 1991.
9 D. Fu, J. Zhou, S. Tongay, K. Liu, W. Fan, T.-J. K. Liu and J. Wu, *Appl. Phys. Lett.*, 2013, **103**, 183105.
10 J.-R. Chen, P. M. Odenthal, A. G. Swartz, G. C. Floyd, H. Wen, K. Y. Luo and R. K. Kawakami, *Nano Lett.*, 2013, **13**, 3106.
11 I. Popov, G. Seifert and D. Tomanek, *Phys. Rev. Lett.*, 2012, **108**, 156802.
12 B. Radisavljevic, M. B. Whitwick and A. Kis, *ACS Nano*, 2011, **5**, 9934.
13 H. Wang, L. Yu, Y.-H. Lee, W. Fang, A. Hsu, P. Herring, M. Chin, M. Dubey, L.-J. Li, J. Kong and T. Palacios, *IEEE Int. Electron Devices Meet.*, 2012, 4.6.1–4.6.4.
14 H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong and T. Palacios, *Nano Lett.*, 2012, **12**, 4674.
15 M. S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. H. Lee, P. Kim, J. Hone and W. J. Yoo, *Nat. Commun.*, 2013, **4**, 1624.
16 H. Liu, A. T. Neal and P. D. Ye, *ACS Nano*, 2012, **6**, 8563.
17 H. Liu and P. D. Ye, *IEEE Electron Device Lett.*, 2012, **33**, 546.
18 S. Das, H.-Y. Chen, A. V. Penumatcha and J. Appenzeller, *Nano Lett.*, 2013, **13**, 100.
19 S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi and K. Kim, *Nat. Commun.*, 2012, **3**, 1011.
20 W. S. Hwang, M. Remskar, R. Yan, T. Kosel, J. K. Park, B. J. Cho, W. Haensch, H. Xing, A. Seabaugh and D. Jena, *Appl. Phys. Lett.*, 2013, **102**, 043116.
21 W. Liu, J. Kang, W. Cao, D. Sarkar, Y. Khatami, D. Jena and K. Banerjee, *IEEE Int. Electron Devices Meet.*, 2013, 19.4.1–19.4.4.
22 W. Bao, X. Cai, D. Kim, K. Sridhara and M. S. Fuhrer, *Appl. Phys. Lett.*, 2013, **102**, 042104.
23 H. Nam, S. Wi, H. Rokni, M. Chen, G. Priessnitz, W. Lu and X. Liang, *ACS Nano*, 2013, **7**, 5870.
24 S. Das and J. Appenzeller, *Phys. Status Solidi RRL*, 2013, **7**, 268.
25 H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu and D. Akinwande, *ACS Nano*, 2013, **7**, 5446.
26 J. Lee, H.-Y. Chang, T.-J. Ha, H. Li, R. S. Ruoff, A. Dodabalapur and D. Akinwande, *IEEE Int. Electron Devices Meet.*, 2013, 19.2.1–19.2.4.
27 D. J. Late, Y.-K. Huang, B. Liu, J. Acharya, S. N. Shirodkar, J. Luo, A. Yan, D. Charles, U. V. Waghmare, V. P. Dravid and C. N. R. Rao, *ACS Nano*, 2013, **7**, 4879.
28 Z. Tan, H. Tian, T. Feng, L. Zhao, D. Xie, Y. Yang, L. Xiao, J. Wang, T.-L. Ren and J. Xu, *Appl. Phys. Lett.*, 2013, **103**, 263506.
29 A. D. Liao, J. Z. Wu, X. Wang, K. Tahy, D. Jena, H. Dai and E. Pop, *Phys. Rev. Lett.*, 2011, **106**, 256801.
30 D. Lembke and A. Kis, *ACS Nano*, 2012, **6**, 10070.
31 D. Jariwala, V. K. Sangwan, D. J. Late, J. E. Johns, V. P. Dravid, T. J. Marks, L. J. Lauhon and M. C. Hersam, *Appl. Phys. Lett.*, 2013, **102**, 173107.
32 K. Kaasbjerg, K. S. Thygesen and K. W. Jacobsen, *Phys. Rev. B: Condens. Matter*, 2012, **85**, 115317.
33 M. Fuhrer and J. Hone, *Nat. Nanotechnol.*, 2013, **8**, 146.
34 R. Ganatra and Q. Zhang, *ACS Nano*, 2014, **8**, 4074.
35 N. Ma and D. Jena, *Phys. Rev. X*, 2014, **4**, 011043.
36 S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira and K. Tsukagoshi, *Nano Lett.*, 2013, **13**, 3546.
37 B. L. Gelmont, M. Shur and M. Stroscio, *J. Appl. Phys.*, 1995, **77**, 657.

38 P. E. Hopkins, *J. Appl. Phys.*, 2009, **105**, 093517.
39 M. Ghorbani-Asl, A. N. Enyashin, A. Kuc, G. Seifert and T. Heine, *Phys. Rev. B: Condens. Matter*, 2013, **88**, 245440.
40 J.-H. Chen, W. G. Cullen, C. Jang, M. S. Fuhrer and E. D. Williams, *Phys. Rev. Lett.*, 2009, **102**, 236805.
41 Y. Tokura, T. Saku and Y. Horikoshi, *Phys. Rev. B: Condens. Matter*, 1996, **53**, R10528.
42 L. Wang, I. Meric, P. Y. Huang, Q. Gao, Y. Gao, H. Tran, T. Taniguchi, K. Watanabe, L. M. Campos, D. A. Muller, J. Guo, P. Kim, J. Hone, K. L. Shepard and C. R. Dean, *Science*, 2013, **342**, 614.
43 K. F. Mak, C. H. Lui and T. F. Heinz, *Appl. Phys. Lett.*, 2010, **97**, 221904.
44 E. Pop, D. Mann, J. Cao, Q. Wang, K. Goodson and H. Dai, *Phys. Rev. Lett*, 2005, **95**, 155505.
45 R. Yan, J. R. Simpson, S. Bertolazzi, J. Brivio, M. Watson, X. Wu, A. Kis, T. Luo, A. R. H. Walker and H. G. Xing, *ACS Nano*, 2014, **8**, 986.

Electronic Supplementary Material (ESI) for Nanoscale.

– Supplementary Information –

Electrical Breakdown of Multilayer MoS_2 Field-Effect Transistors with Thickness-Dependent Mobility

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1. Experimental Details of Electrical Breakdown Measurements

The multilayer MoS_2 devices experience multiple sweeping cycles in the electrical breakdown measurement (as shown in Fig. 4 in the Main Text). In the measurements, we start with smaller sweeping ranges for V_D, and then gradually increase the voltage range. We repeat multiple times for each V_D range and observe changes in device characteristics, including breakdown. Figure S1 shows the details of V_D sweeps. We observe in multiple devices (Figs. S1 (c)-(h)) that the current levels gradually decrease with subsequent sweeping cycles. Different breakdown locations on the devices are observed (Fig. S1 insets).

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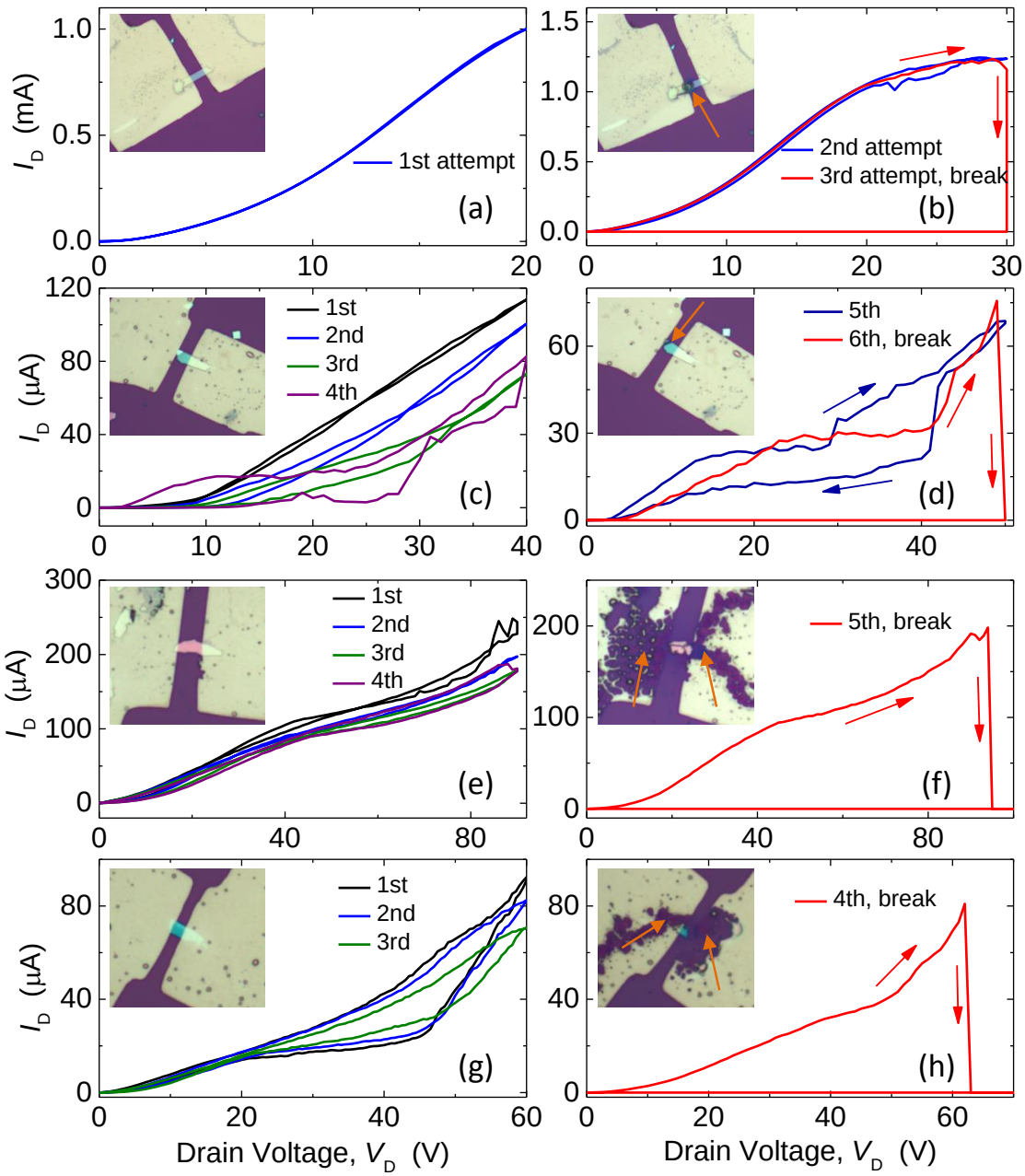

Fig. S1: V_D sweeps during the electrical breakdown measurement of multilayer MoS_2 transistors shown in Fig. 4 in the main text, with (a)-(b) for the device in Fig. 4(a), (c)-(d) for the device in Fig. 4(b), (e)-(f) for the device in Fig. 4(c), and (g)-(h) for the device in Fig. 4(d). The red curves show the final breakdown sweeps. Insets: Optical microscope images before (a,c,e,g) and after (b,d,f,h) the breakdown.

2. **Scattering Mechanisms**

We model the device mobility dependence on thickness with different scattering mechanisms, and the relaxation time for each scattering mechanism is plotted in Fig. S2 for MoS_2 thickness of 2.5nm to 86nm, which corresponds to 4 to 140 layers, using 0.615nm as the layer spacing[1]. As phonon scattering and charged impurity scattering in MoS_2 has been reported elsewhere[1,2,3,4,5], here we focus on other mechanisms, including boundary scattering (assuming the electron mean free path is on the order of MoS_2 thickness)[6], vacancy scattering (in calculation we use values of vacancy defect density n_v=10^{13}cm^{-2}, electron density n_e=10^{12}cm^{-2}, and vacancy radius comparable to the lattice constant)[7], and thickness step scattering (assuming average step distance of ~1.5μm, and step height comparable to the single layer thickness)[8]. We calculate these scattering mechanisms in MoS_2 and the results are shown in Fig. S2. The total relaxation time is calculated for different fitting parameters β (2, 4, and 6) as shown in the main text.

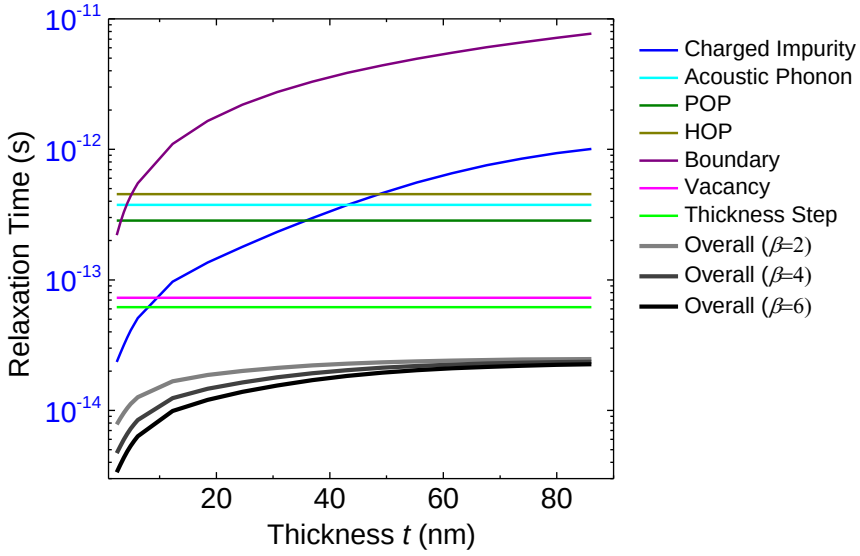

Fig. S2: Relaxation time for different scattering mechanisms with different MoS_2 thickness.

3. Details of FEM Simulation for Electrical Breakdown

In the electrical breakdown simulation (as shown in Fig. 6 in the Main Text), we use σ=35000S/m in Figs. 6(a)-(c)[9]. In the model we assume the MoS_2 extends 1μm into the contact, with 8kΩ contact resistance[10]. The heat is generated in MoS_2 channel and contact region and is dissipated to the SiO_2 and Si substrate, using thermal conductivity of SiO_2 and Si of 1.4W/(m K) and 130W/(m K), respectively. The surface of the substrate is held at room temperature (293.15K). The cross-section view of the FEM result (Fig. S3) shows that the heat dissipation into the substrate dominates.

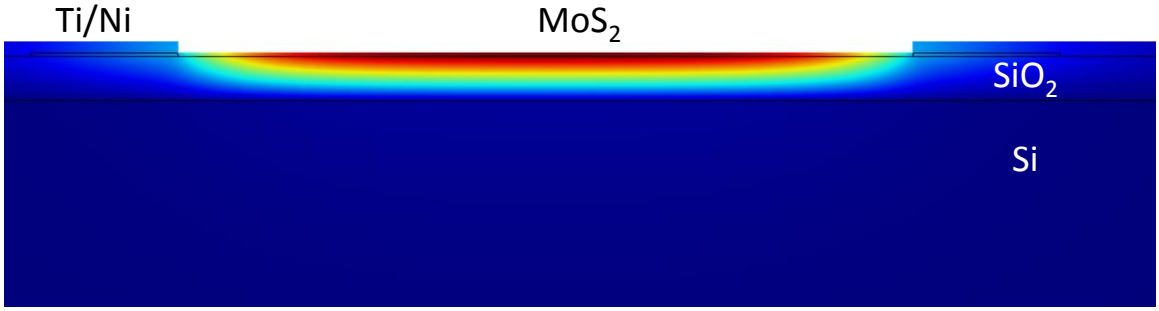

Fig. S3: The cross-section view of the FEM result of the temperature profile under Joule heating. In simulation the MoS_2 has t=25nm, L=5μm, W=2μm.

4. Summary of All the Measured Devices

Table S1: List of measured multilayer MoS_2 FETs and the parameters

Device ID #	MoS_2 Thickness (nm)	SiO_2 Substrate Thickness	Contact Materials	Mobility ($cm^2/(V\ s)$)	I_{On}/I_{Off} Ratio	Comments
1	70.3	290nm	Ti(3nm) /Ni(50nm)	42	10^4	Figs. 2(a)-2(d), Highest Mobility
2	5.7	290nm	Ti(2nm) /Ni(150nm)	9.9	4×10^6	Figs. 2(e)-2(h)
3	12	290nm	Ni(50nm)	18.3	6×10^4	Fig. 4(d)
4	18.4	290nm	Ti(2nm) /Ni(150nm)	6.5	10^6	
5	55	290nm	Ni(50nm)	38.7	7×10^4	Fig. 4(c)
6	76/22 Step	290nm	Ni(50nm)	2	6×10^4	Fig. 4(b)
7	32	290nm	Ti(5nm) /Ni(100nm)	36.8	10^7	Highest I_{On}/I_{Off} Ratio
8	12	290nm	Ti(5nm) /Ni(100nm)	9.8	10^6	
9	39	3.5μm	Ti(5nm) /Ni(150nm)	31.9	10^5	
10	7	3.5μm	Ti(5nm) /Ni(70nm)	1.6	10^3	

References

[1] S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira, K. Tsukagoshi, Nano Lett. **13**, 3546 (2013).

[2] N. Ma, D. Jena, Phys. Rev. X **4**, 011043 (2014).

[3] K. Kaasbjerg, K. S. Thygesen, K. W. Jacobsen, Phys. Rev. B **85**, 115317 (2012).

[4] B. L. Gelmont, M. Shur, M. Stroscio, J. Appl. Phys. **77**, 657 (1995).

[5] S. Kim, A. Konar, W.-S. Hwang, J. H. Lee, J. Lee, J. Yang, C. Jung, H. Kim, J.-B. Yoo, J.-Y. Choi, Y. W. Jin, S. Y. Lee, D. Jena, W. Choi, K. Kim, Nat. Commun. **3,** 1011 (2012).

[6] P. E. Hopkins, J. Appl. Phys. **105**, 093517 (2009).

[7] J.-H. Chen, W. G. Cullen, C. Jang, M. S. Fuhrer, E. D. Williams, Phys. Rev. Lett. **102**, 236805 (2009).

[8] Y. Tokura, T. Saku, Y. Horikoshi, Phys. Rev. B **53**, R10528 (1996).

[9] B. Radisavljevic, A. Kis, Nat. Mater. **12**, 815 (2013).

[10] B. W. H. Baugher, H. O. H. Churchill, Y. Yang, P. Jarillo-Herrero, Nano Lett. **13**, 4212 (2013).