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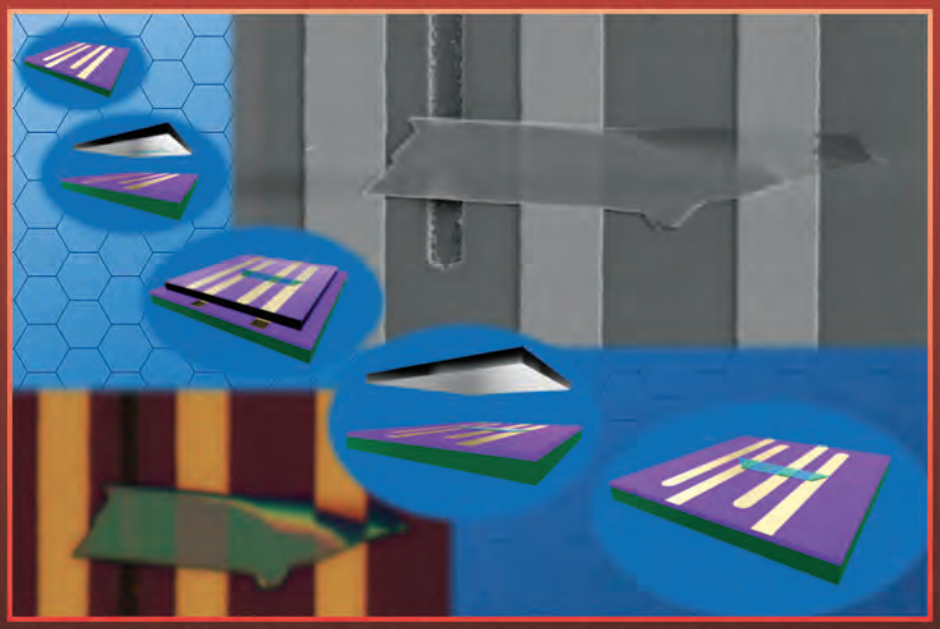

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Review Article:

Oxide-based Chromogenic Coatings and Devices for Energy Efficient Fenestration: Brief Survey and Update on Thermochromics and Electrochromics

-by Claes G. Granqvist

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Multilayer MoS_2 transistors enabled by a facile dry-transfer technique and thermal annealing

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Molybdenum disulfide (MoS_2) two-dimensional nanostructures have been actively explored for ultrasmall transistors beyond graphene. The current prevailing methods for producing MoS_2 devices involve multiple wet chemistry steps, which not only are time consuming, but may also unfavorably affect material quality and impair device performance through the chemical processes. Here, the authors report the first dry-transferred pristine MoS_2 field-effect transistors (FETs) without any post-transfer lithographical and chemical processes, by using a facile, completely dry transfer technique with high throughput and high precision in alignment. The authors also show that the device performance can be greatly boosted by thermal annealing. Combining the dry-transfer technique with thermal annealing, the authors achieve MoS_2 FETs with mobility up to 76 $cm^2/(V\ s)$ and on/off ratios exceeding 10^7. The authors further show how continued annealing cycles improve the MoS_2 devices' conductance, mobility, on/off ratio, transconductance, threshold voltage, and contact quality. © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4898117]

I. INTRODUCTION

Molybdenum disulfide (MoS_2) has recently emerged as a promising two-dimensional (2D) layered material for novel electronic and optoelectronic nanodevices.[1–4] MoS_2 field-effect transistors (FETs),[5–13] in particular multilayer MoS_2 devices,[14–25] have shown significant potential for enabling 2D electronic devices, by demonstrating increasingly competitive performance including improving mobility, contact quality, and excellent on/off ratios. All the MoS_2 FETs reported to date, however, are fabricated using electron-beam- or photo-lithography on top of MoS_2 flakes,[5–25] and/or polymer-assisted transfer of MoS_2 sheets followed by dissolving the polymer,[26,27] both of which involve multiple wet processing steps where the 2D crystals are in direct contact with various wet chemicals. Such processes may contaminate or even degrade the MoS_2 surface, and adversely affect device performance.[28–30] Here, we demonstrate multilayer MoS_2 FETs fabricated by using a completely dry-transfer method, which not only obviates the undesirable wet chemistry steps, but also has high device yield, and could be potentially more scalable than the lithography methods currently used for making MoS_2 2D electronic and optoelectronic devices. As outlined in Fig. 1, in contrast to the conventional device fabrication schemes [Figs. 1(b)–1(d)] where the MoS_2 flake on the substrate undergoes a series of steps involving wet chemistry, in the new scheme, the MoS_2 crystal experience no chemical process [Figs. 1(e)–1(g)], and can thus remain pristine. The performance of as-transferred devices can be further improved through vacuum thermal annealing treatments. While experiments on graphene FETs suggest that annealing may lead to dissolving of graphene into metal and thus improve contact,[31] annealing effects on MoS_2 devices remain to be systematically explored. Here, by treating dry-transferred MoS_2 FETs with vacuum annealing at different temperatures, we examine the annealing effects on various device parameters including the device conductance, electron mobility, current on/off ratio, transconductance, and threshold voltage. We further show that

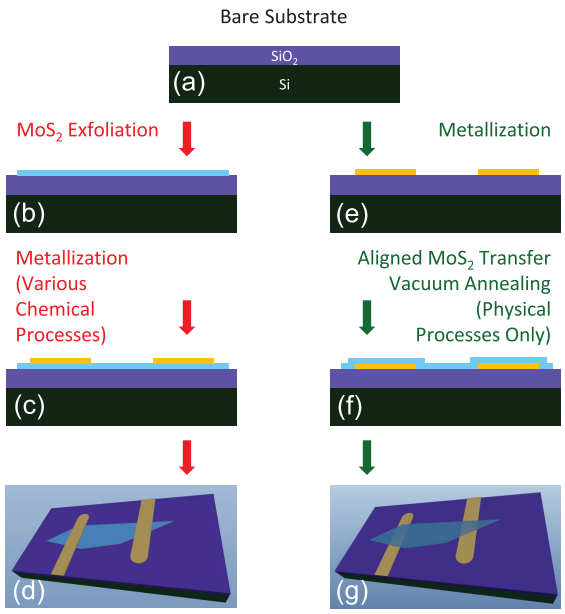

FIG. 1. (Color online) Outline and comparison of the different device fabrication schemes. (a) Substrate before processing. (b) In the conventional fabrication scheme, MoS_2 flake is first exfoliated, grown or transferred onto the substrate, and (c) then the electrodes are patterned on top of the MoS_2 crystal through a series of lithographic and chemical processes. (d) The resulting device is therefore subject to possible chemical contamination and degradation. (e) In the dry-transfer scheme, all the structural fabrication steps are performed before (f) the MoS_2 transfer, and only physical processes are involved afterward, thus resulting in (g) pristine MoS_2 devices.

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the contact quality can also be significantly improved by vacuum thermal annealing.

II. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Substrate fabrication

To facilitate the dry-transfer scheme that obviates any post-processing on the MoS_2 crystal, we pre-pattern the required device structure on the substrate (Fig. 2). We start with a p++ doped silicon (Si) wafer [Fig. 2(a)] coated with 290 nm thermally grown silicon dioxide (SiO_2). We first spin coat photoresist (Shipley Microposit S1813) at 4000 rpm [Fig. 2(b)], and expose the resist using ABM contact aligner with near-UV filter (405–365 nm) followed by automated development using Hamatech–Steag wafer processor [Fig. 2(c)]. We then deposit 5 nm Cr and 30 nm Au using electron-beam evaporation [Fig. 2(d)], followed by lift-off [Fig. 2(e)]. Substrates for nonsuspended devices become complete after this step. For suspended structures and mechanically moveable devices, we perform a second layer of lithography. Upon examining the metalized wafer, we spin coat the same photoresist again [Fig. 2(f)]. The wafer is then carefully aligned to the second layer mask (etch windows), and exposed/developed using the same parameters [Fig. 2(g)]. We then use reactive ion etch (RIE) to remove the exposed oxide [Fig. 2(h)]. The etch depth is 190 nm (CHF_3/O_2 recipe on an Oxford PlasmaLab 80+ RIE System, with SiO_2 etch rate 27 nm/min) and 100 nm SiO_2 remains above Si. Upon removing the photoresist and dicing the wafer [Fig. 2(i)], we obtain the final substrate with patterned electrodes and microtrenches [Fig. 2(j)] for making suspended MoS_2 FET devices.

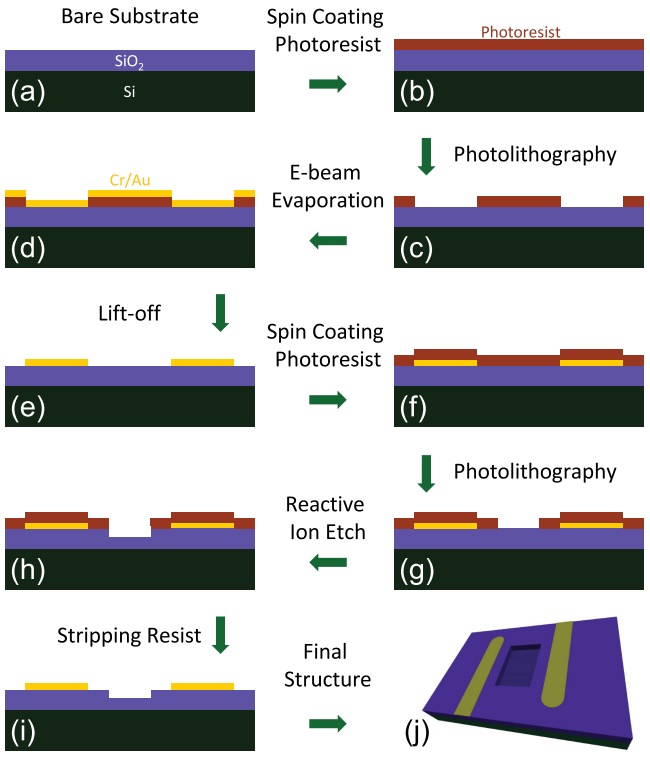

FIG. 2. (Color online) Fabrication of the substrate. (a) Substrate before processing. (b) Substrate coated with photoresist. (c) Windows on the resist layer opened through photolithography. (d) Metal layer deposited on the wafer. (e) Lift-off removing the metal layer except in the exposed area. (f) Resist coated for the second exposure. (g) Photolithography defining the etch windows. (h) RIE removing oxide. (i) Resist stripped. (j) Illustration of the final substrate structure.

B. MoS_2 flake preparation and dry-transfer

An elastomer stamp, polydimethylsiloxane (PDMS), is used for MoS_2 flake exfoliation and transfer (Fig. 3). First, we cut a small piece of PDMS [Fig. 3(a)]. After peeling off the protecting layers on both sides of it [Fig. 3(b)], the stamp is gently applied onto a clean glass slide [Fig. 3(c)]. Then, with sufficient pre-exfoliation iterations [Fig. 3(d)], MoS_2 flakes are exfoliated onto the PDMS stamp [Fig. 3(e)]. Both sides of the resulting MoS_2 flake are free of tape residue. Thin MoS_2 flakes on the PDMS stamp are carefully identified using optical microscope (Olympus MX50). The substrate is then mounted on the transfer stage with desired orientation [Fig. 3(f)], and the glass slide is mounted upside-down on a micromanipulator [Fig. 3(g)], before the transfer stage is set under a long working distance microscope [Fig. 3(h)].

The details of the transfer process are shown in Figs. 4(a)–4(e) and 5, with great caution required for positioning and transferring a pre-identified MoS_2 flake to the designated location on the prepatterned substrate and obtain the desired device geometry. In Figs. 4(b) and 4(c), we keep adjusting the focus back and forth between the MoS_2 flake (on PDMS stamp) and the target area (on substrate) to continuously monitor their relative position, and fine tuning the location of the flake using the micromanipulator to align the flake and the substrate while gradually lowering the glass slide. By continuously lowering the glass slide in a slow speed, the PDMS stamp is gradually brought into contact with the substrate [Figs. 4(c) and 5(a)–5(c)]. Once fully in contact [Figs. 4(c) and 5(d)], we slowly raise the glass slide [Figs. 5(e) and 5(f)]. As the PDMS is peeled away from the substrate, the MoS_2 flake remains on the substrate due to van der Waals force [Fig. 4(d)]. As the flake is readily contacted by the metal electrodes, no further chemical processing is necessary [Figs. 4(e), 4(f), and 6].

With this wet-chemical-free method, we have achieved nearly 100% success rate in obtaining pristine MoS_2 FETs. Since each flake can be aligned to the electrodes during the transfer, we fabricate the electrodes at wafer scale, which significantly improves the efficiency and yield, and makes this technique partially scalable (for the substrate part). The dry-transfer scheme (here on 290 nm-SiO_2-on-Si) is also readily applicable to different substrates, such as those made with much thinner high-κ dielectric (e.g., Al_2O_3) layers, to obtain high-performance MoS_2 FETs toward low-threshold-voltage, low-power operations.

C. Initial characterization prior to annealing

Electrical characterization is performed with a probe station (for contacting the prepatterned Au electrodes), and with high-precision source measurement units (SMUs) in

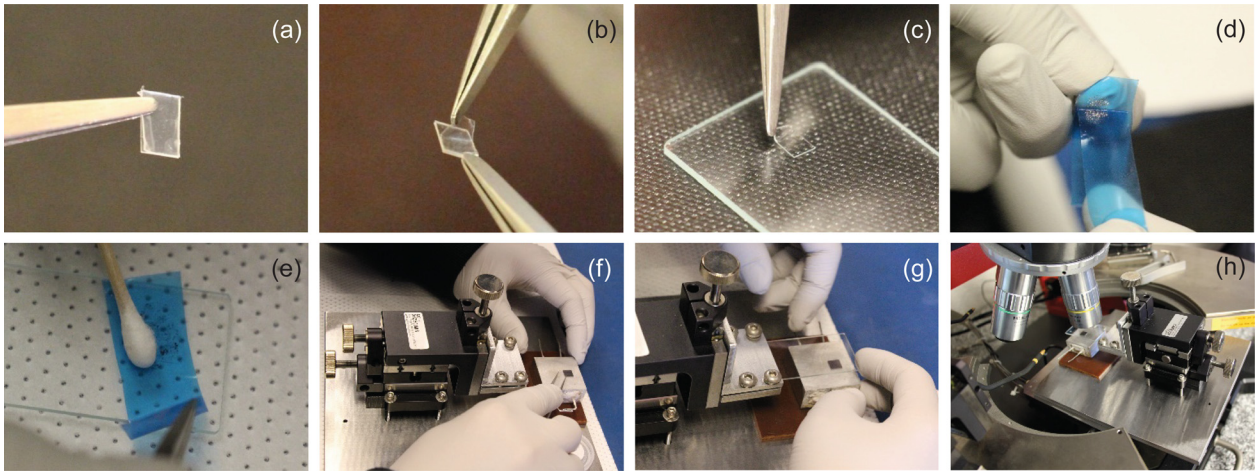

FIG. 3. (Color online) MoS_2 flake exfoliation and transfer preparation. (a) Small PDMS stamp piece cut from a large film. (b) Peeling off the protecting layers. (c) Applying PDMS stamp onto a glass slide. (d) Exfoliating MoS_2 flakes with Nitto tape. (e) Exfoliating MoS_2 flakes onto a PDMS stamp. (f) Mounting the prefabricated substrate onto the stage with desired position and orientation. (g) Clamping the glass slide onto the micromanipulator. (h) The transfer stage mounted under a microscope.

Keithley 4200 SCS (for applying voltage and measuring current) [Fig. 7(a)]. By applying a positive gate voltage (V_G) at SMU1, the Schottky barrier between the MoS_2 flake and the Au contact narrows down, and the Fermi level of MoS_2 moves closer to the conduction band. When V_G surpasses the threshold voltage (V_T), the MoS_2 FET is switched on. The transport property is characterized by connecting the drain electrode to SMU2 for supplying drain voltage (V_D), and grounding the source electrode. Figure 7(c) shows the measured data for an as-transferred MoS_2 FET device [Fig. 7(b)].

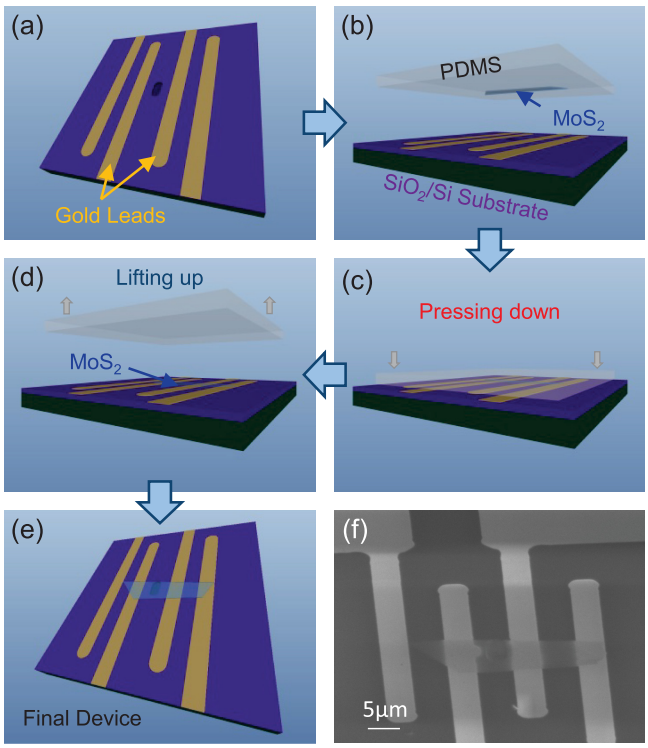

FIG. 4. (Color online) Schematic illustration of the dry-transfer steps. (a) Pre-patterned substrate. (b) Aligning PDMS stamp with exfoliated MoS_2 flake to the substrate. (c) Stamp engaged. (d) Stamp disengaged. (e) Resulting device. (f) SEM image of the device.

The drain current (I_D) is low (<1 nA), presumably due to the nonideal contact between MoS_2 and Au as well as the adsorbed oxygen (O_2) and water molecules from the ambient.

D. Investigation of thermal annealing effects

While the dry-transfer method reliably produces devices with desired geometry, the gentle pressing from the PDMS

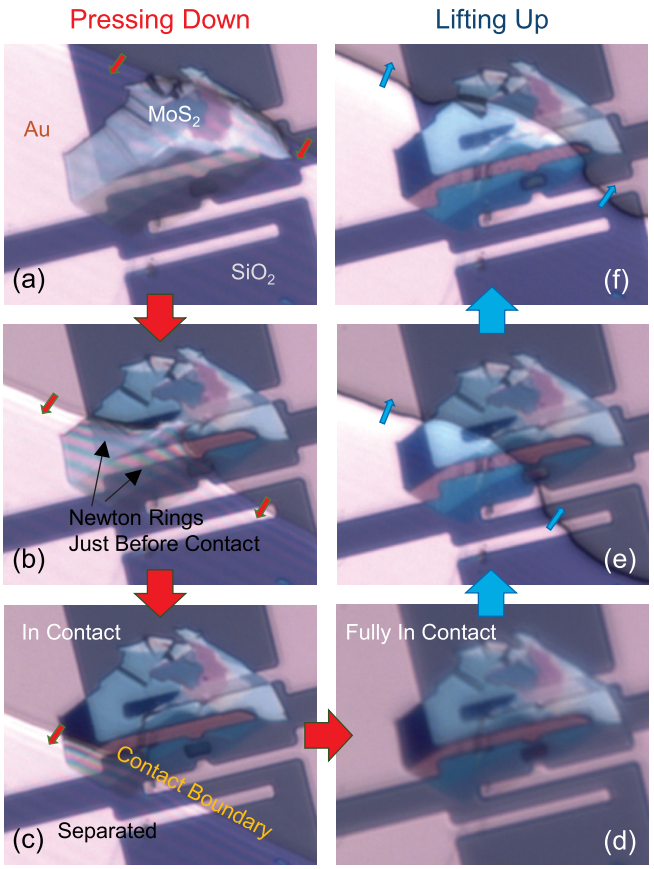

FIG. 5. (Color online) Optical microscope images capturing the dry-transfer process. (a)–(c) Engaging the PDMS stamp and MoS_2 flake onto the substrate. (d) MoS_2 and substrate fully in contact. (e)–(f) Disengaging the PDMS stamp.

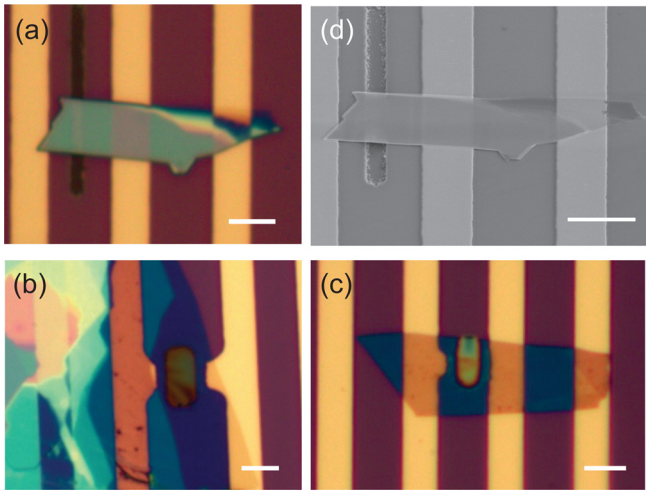

FIG. 6. (Color online) Optical microscope and SEM images of resulting devices. (a)–(c) Dry-transferred MoS_2 FETs with suspended and nonsuspended FET channels. (d) SEM image of the suspended device in (a) after 300 °C annealing, showing that it remains suspended. All scale bars are 5 μm.

stamp may not always guarantee ideal contact between the MoS_2 flake and the metal electrodes underneath [Fig. 7(c)]. To address this issue and attain highly reliable contacts for the dry-transferred MoS_2 FETs, we use vacuum thermal annealing to improve the contact quality and achieve enhanced device performance.[29–34]

We use a home-built split-tube furnace system to conduct thermal annealing of transferred MoS_2 FET devices. The system consists of a nitrogen (N_2) gas source, flow rate control valves, a 1-in.-diameter horizontal quartz tube furnace and a vacuum pump [Fig. 8(a)]. Our typical annealing procedure [Fig. 8(b)] is as follows: after putting the device into the furnace, the vacuum pump is turned on to reach moderate vacuum (~5 mTorr). Then, a N_2 flow (3 SCCM) is introduced, raising the pressure to ~45 mTorr. We then ramp the

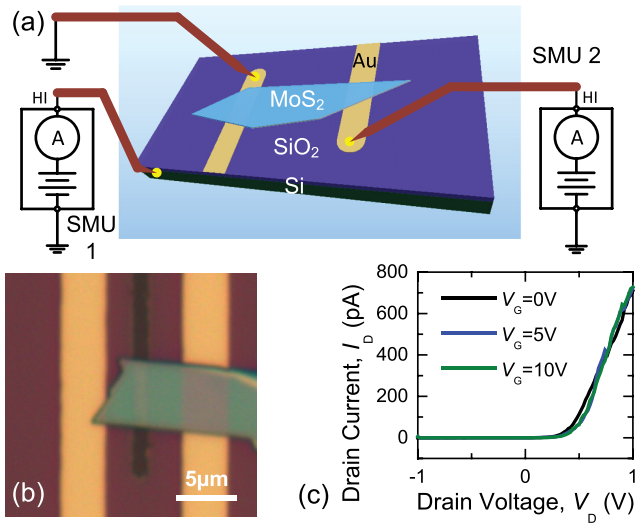

FIG. 7. (Color online) Electrical characterization of an as-transferred device. (a) Measurement system and electrode configuration. (b) Optical microscope image of a dry-transferred device, with part of the MoS_2 flake suspended over a 1.5 μm wide microtrench. (c) Transport characteristic (I_D-V_D) of the device in (b) under different V_G.

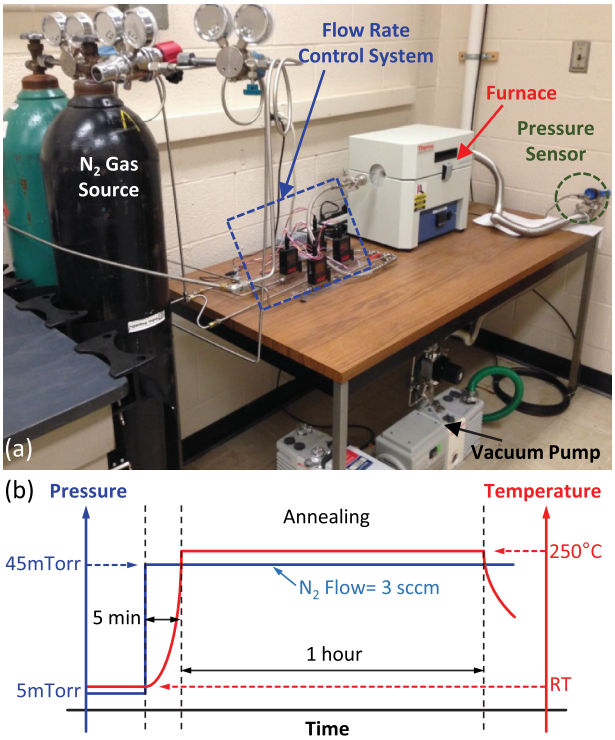

FIG. 8. (Color online) Vacuum thermal annealing. (a) A photo of the vacuum thermal annealing system. (b) A typical annealing recipe showing the temperature and pressure changes in the furnace.

furnace temperature to the setpoint (between 250 and 350 °C). Once the temperature setpoint is reached in about 5 min, annealing is conducted for 1 h. Upon completion, the furnace is cooled down in about 15 min, and the device is retrieved after slowly venting the tube with N_2.

The devices' performance typically exhibits notable improvement after initial annealing. For example, a SiO_2-supported MoS_2 FET [Fig. 9(a) inset] shows more than 1000-fold increase in conductance upon annealing at 250 °C [Figs. 9(a) and 9(b)]. The contact also becomes more Ohmic after annealing, and the drain current/conductance start to show clear V_G dependences [Fig. 9(b)]. We further characterize the transfer characteristics of the MoS_2 FET after annealing by sweeping V_G (between −10 and 10 V) while keeping V_D constant (at 1 V). From the linear region of the transfer curve, we extract the field-effect mobility using $\mu = (dI_D/dV_G)/[(w/L)C_{ox}V_D]$, where w and L are, respectively, the width and length of the MoS_2 channel (obtained from the optical image), C_{ox} is the capacitance per unit area to the back gate of the MoS_2 channel ($C_{ox} = \varepsilon_0\varepsilon_r/d_{ox} = 1.19 \times 10^{-4}$(F/m), ε_0: vacuum permittivity; ε_r: relative permittivity of SiO_2; d_{ox}: SiO_2 thickness). The device shows mobility of 17 cm^2/(V s) and a current on/off ratio of $I_{on}/I_{off} \approx 2 \times 10^6$ [Fig. 9(c)], with small hysteresis (in V_G) and minimal leakage through the gate dielectric (<5 pA).

Further enhancement of device performance can often be achieved via additional thermal annealing. Figure 10 shows the performance of a substrate-supported device (already annealed at 250 °C) continues to improve upon additional annealing at 300 and 350 °C. The on state current increases and the contact becomes more Ohmic after annealing at 300 °C, compared to the performance after the initial

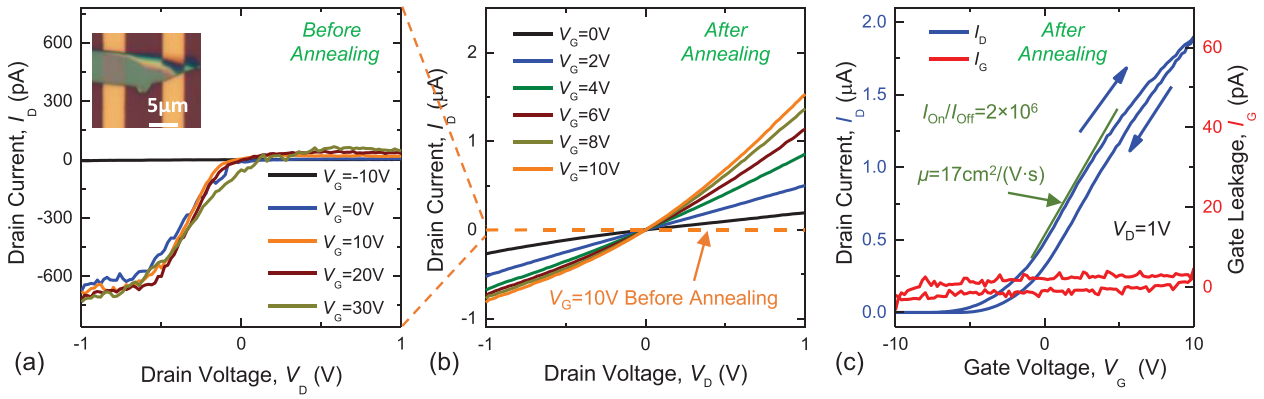

FIG. 9. (Color online) Effect of initial thermal annealing on device performance. (a) and (b) Transport characteristics of device 14 (in Table I) (a) before and (b) after 250 °C annealing, under different V_G. (c) Transfer characteristic (I_G-V_D) and gate leakage current (showing there is minimal gate leakage) of the device with $V_D = 1$ V after annealing. Inset in (a): Optical image of the device.

annealing at 250 °C [Figs. 10(a) and 10(c)]. The field-effect mobility increases by a factor of ∼4 upon annealing at 300 °C, as shown in Figs. 10(b) and 10(d). Upon annealing at 350 °C, the current and mobility further increase [Figs. 10(e) and 10(f)], although the difference between 350 and 300 °C annealing is less dramatic than that obtained between 300 and 250 °C annealing, suggesting that the device may be approaching its optimal performance achievable through thermal annealing.

Performance of suspended MoS_2 FET devices could also be improved by thermal annealing. Figure 11 shows measurement of a device with suspended channel fully covering a prepatterned 4 × 8 μm microtrench [Fig. 11(a) inset]. Annealing at 250 °C improves the conductance by ∼70 times [Figs. 11(a) and 11(c)] and enhances the gating effect [Figs. 11(b) and 11(d)].

To categorize and quantify the effects of thermal annealing on the performance of MoS_2 transistors, we plot various device parameters as functions of annealing temperatures, for 14 different devices fabricated using the dry transfer method and are substrate-supported (Fig. 12). We find that, with thermal annealing treatments at increasing temperatures from 200 to 350 °C, reliable reduction in device total resistance R_{total} (thus increase in conductance G) is observed [Figs. 12(a) and 12(b)], together with consistent increase in mobility μ [Fig. 12(c)], improvement in on/off ratio I_{on}/I_{off} [Fig. 12(d)],

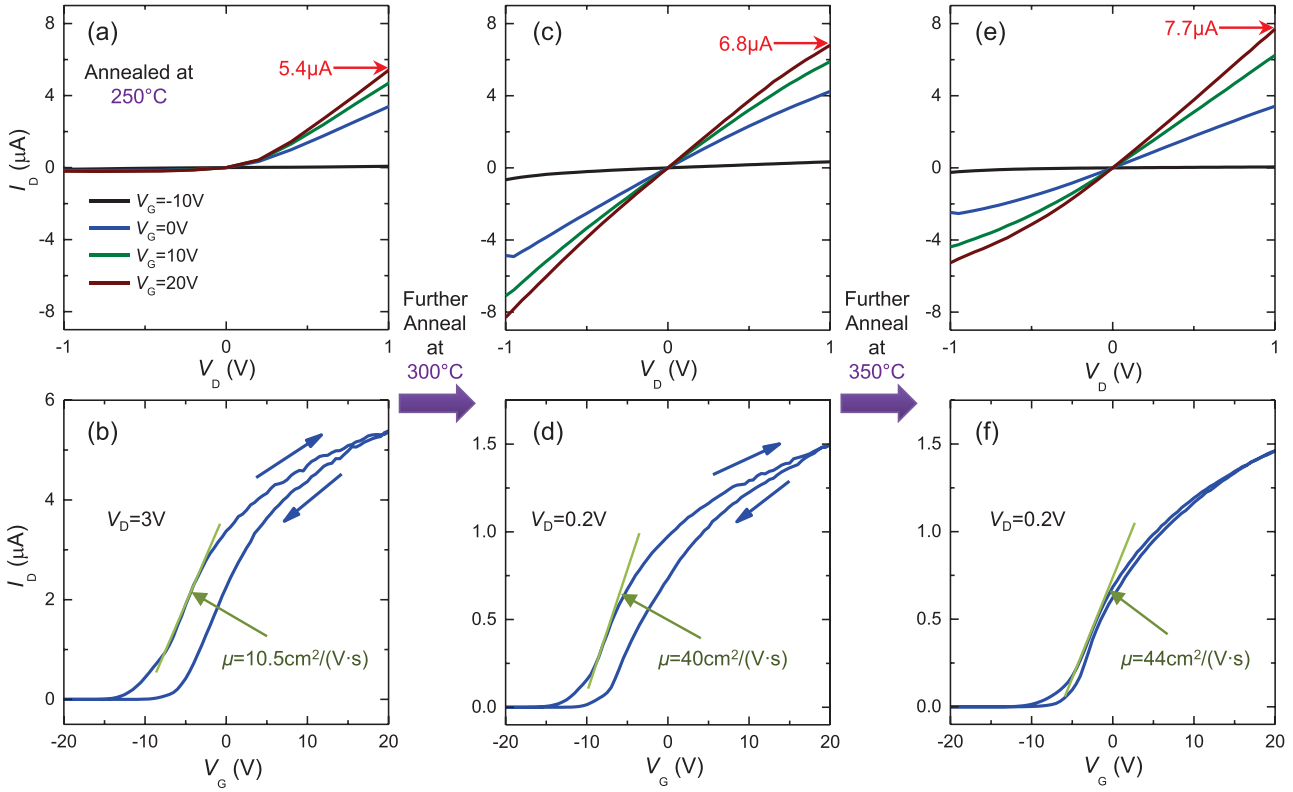

FIG. 10. (Color online) Effect of additional thermal annealing on device performance. (a), (c), and (e) Transport characteristics of device 10 (in Table I) after (a) 250 °C, (c) 300 °C, and (e) 350 °C annealing, under different V_G. (b), (d), and (f) Transfer characteristics after (b) 250 °C, (d) 300 °C, and (f) 350 °C annealing.

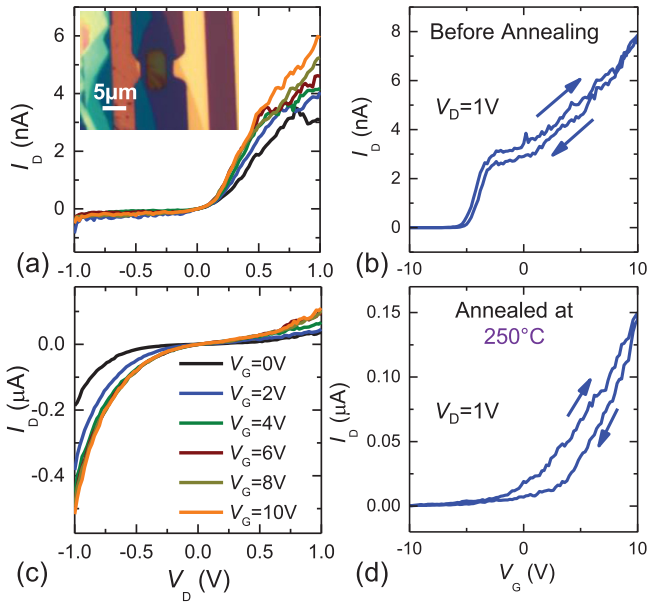

FIG. 11. (Color online) Effect of thermal annealing on suspended MoS_2 FET device. (a) and (c) Transport characteristics (a) before and (c) after 250 °C annealing, under different V_G. (b) and (d) Transfer characteristics (b) before and (d) after 250 °C annealing. Inset in (a): Optical image of the device.

and enhancement in transconductance g_m [Fig. 12(e); for fair comparison, we normalize all the g_m values with the drain bias V_D]. These parameters are essential for FET devices. The highest mobility we achieve is 76 $cm^2/(V\,s)$, and the highest I_{on}/I_{off} is 1.3×10^7, both comparable with other electron-beam-lithography-fabricated multilayer MoS_2 FETs with similar device structure and measurement environments.[14,17–21] The threshold voltage V_T does not continue to shift upon repeated thermal annealing, but appears to stabilize at certain values [Fig. 12(f)].

Besides the quantitative entities demonstrated in Fig. 12, the qualitative measure of whether the contact is Ohmic or not is also important. We find that, while sometimes thermal annealing at higher temperature can convert non-Ohmic contacts into Ohmic [Figs. 13(a) and 13(b)], occasionally such conversion may not be complete but still with improvement clearly observable ["improved contact," Figs. 13(c) and 13(d)]. Improvements in contact Ohmicity by thermal annealing is summarized in Figs. 13(e) and 13(f). Among the 14 devices, all of them have non-Ohmic contact before thermal annealing. After thermal annealing at 300 °C or higher, more than 90% of the devices exhibit Ohmic or improved contacts. In general, devices becomes more Ohmic after thermal annealing at higher temperature in the 200–350 °C range. Table I lists the different device parameters before and after thermal annealing for 14 substrate-supported MoS_2 transistor devices, showing R_{total} as low as 100 kΩ and g_m/V_D as high as 1040 nA/V^2.

In order to better understand the mechanism of thermal annealing on the improvements of MoS_2 FET performance, we propose several possible mechanisms that can contribute to the observed effects as illustrated in Fig. 14. Since the MoS_2 crystals in our devices are free from tape residues and other post-transfer chemical residues, the commonly referenced thermal annealing effect of cleaning organic residue does not apply. Accordingly, we mainly consider two alternative contributions from thermal annealing:[33] improving the contact and removing the surface adsorbates.

First, there are dangling bonds and defects in MoS_2 crystals, especially for mechanically exfoliated flakes. Upon thermal annealing, the dangling bonds in MoS_2 could form stable chemical bonds with the metal electrodes, resulting in end-contacts, which could reduce the contact resistance, similar to that in graphene devices.[34] This is consistent with our observation of improvement in Ohmicity of the contacts upon annealing (Fig. 13).

Second, as MoS_2 sample is exposed to the ambient, different species (e.g., nitrogen, oxygen, and water molecules)

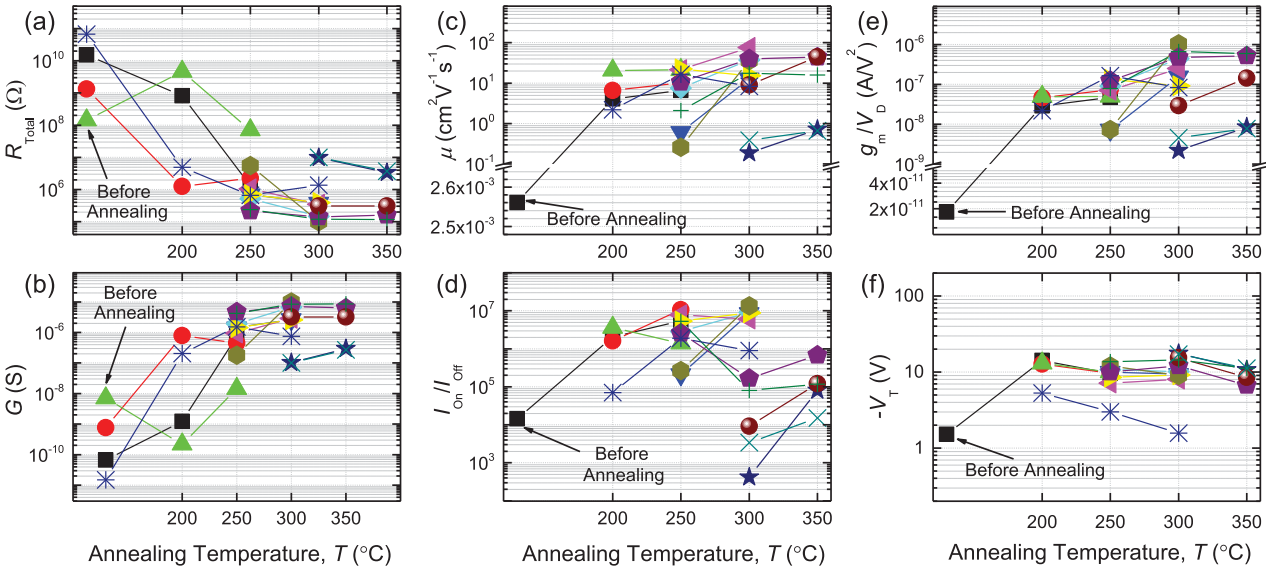

FIG. 12. (Color online) (a)–(f) Summary of annealing effects for 14 devices under different annealing temperatures, on their (a) on-state resistance R_{total}, (b) on-state conductance G, (c) mobility μ, (d) current on/off ratio I_{on}/I_{off}, (e) normalized transconductance g_m/V_D, and (f) magnitude of measured V_T.

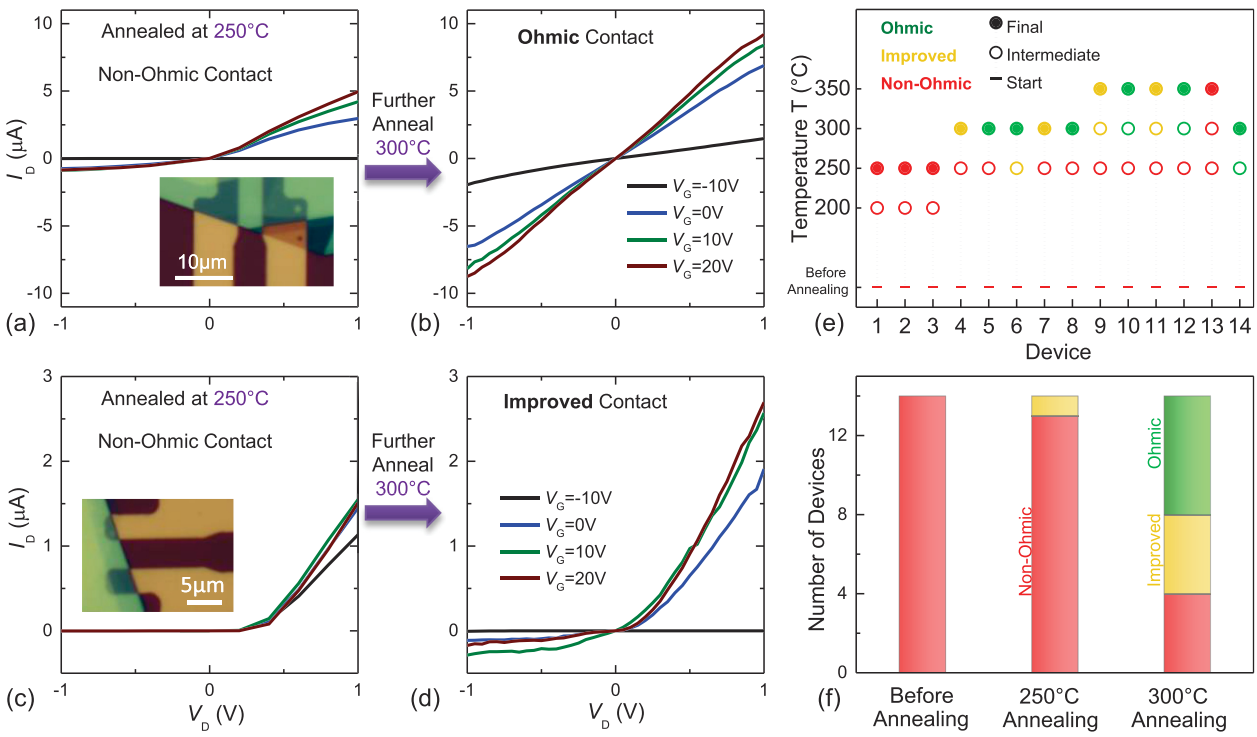

FIG. 13. (Color online) Annealing effect on contacts, with non-Ohmic contact becoming (a) and (b) Ohmic, or (c) and (d) improved. (e) Summary of contact improvement upon annealing for 14 devices (listed in Table I). (f) Statistics of 11 devices annealed at 300 °C (devices 4-14). Insets in (a) and (c): Optical images of the respective devices.

can be adsorbed on the MoS_2 surface and degrade device performances, such as mobility.[32,35] Vacuum thermal annealing effectively removes adsorbed molecules, resulting in improved device performance. The efficiency of adsorbates removal is determined by the desorption rate:[36] $R_{des} = \nu N^x \exp(-E_a/RT)$, where ν is the attempt frequency, N is the concentration of adsorbates, x is kinetic order of desorption, E_a is desorption activation energy, R is the gas constant, and T is temperature. For nitrogen and oxygen on silica, $E_a \sim 51$ kJ/mol,[37] and for water on silica $E_a \sim 80$ kJ/mol.[38] We find that at annealing temperature (~600 K), R_{des} of nitrogen and oxygen is ~5 times higher than at room temperature (~300 K), and for water the ratio is ~13. The accelerated desorption at high temperature and significantly reduced adsorption in vacuum therefore results in effective surface adsorbates removal during the thermal annealing process.

To further experimentally examine the above proposed mechanisms, we perform long-baseline measurements on two representative devices [devices 12 and 13 from Fig. 13(e)],

TABLE I. Summary of the total resistance R_{total}, mobility μ, on/off ratio, normalized transconductance g_m/V_D, and threshold voltage V_T for all the 14 substrate-supported devices after final annealing. R_{total} for all devices are measured at $V_D = 1$ V and $V_G = 10$ V. Bold values represent the best device performance. Final annealing temperatures: No. 1–3: 250 °C; No. 4–8 and No. 14: 300 °C; No. 9–13: 350 °C.

No.[a]	R_{total} (MΩ)	μ (cm^2 V^{-1} s^{-1})	I_{on}/I_{off}	g_m/V_D (nA/V^2)	V_t (V)
1	1.31	6.6	5.46×10^6	47	−9.6
2	2.24	10.3	1.1×10^7	73	−9.6
3	69.7	21.2	1.4×10^6	50	−10.0
4	0.37	13.0	8.5×10^6	155	−9.4
5	0.15	37.1	9.0×10^6	441	−10.1
6	0.35	**76.0**	6.0×10^6	250	−8.0
7	0.39	15.3	8.8×10^6	92	−9.1
8	**0.10**	36.4	$\mathbf{1.3 \times 10^7}$	**1040**	−9.0
9	3.37	0.72	8.0×10^4	9	−10.7
10	0.16	44.1	6.8×10^5	520	−6.7
11	0.31	44.4	1.2×10^5	143	−8.5
12	0.12	15.8	1.2×10^5	595	−11.3
13	3.69	0.7	1.5×10^4	8	−11.2
14	1.35	8.4	8.9×10^5	83	−1.6

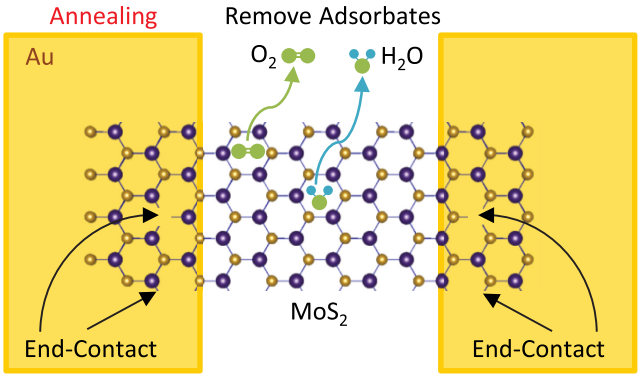

FIG. 14. (Color online) Illustration of annealing effect on device performance, showing formation of end-contact between the dangling bonds and metal, as well as removal of surface adsorbates.

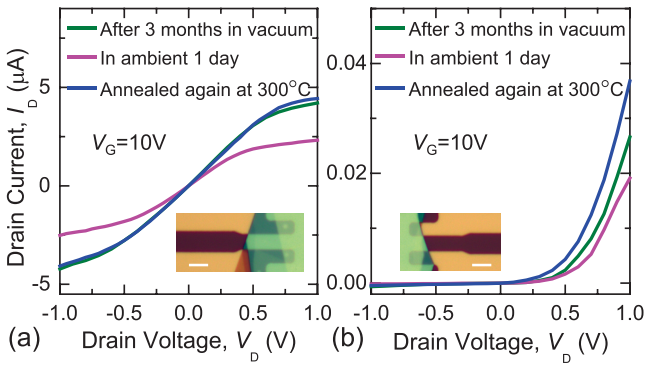

FIG. 15. (Color online) Transport characteristics of (a) device 12 and (b) device 13 after storing the devices in vacuum for 3 months since the initial annealing, after exposing in ambient for 1 day, and after annealing again in vacuum at 300 °C for 1 h. All the data are taken at $V_G = 10$ V. Insets: Optical microscope images of the devices. Scale bars: 5 μm.

one from each representative group (being Ohmic and non-Ohmic after the initial annealing), by monitoring their performance evolution upon (1) storing in vacuum for 3 months after annealing, (2) then exposing to the ambient for 1 day, and (3) finally annealing in vacuum for 1 h at 300 °C (Fig. 15). There are two main observations. First, the performance of both devices clearly degrades after being left in open air for 1 day, and recovers after further thermal annealing. This is consistent with the proposed mechanism involving adsorption and removal of adsorbate molecules. Second, the device performance upon postannealing air exposure does not fully degrade to the preannealing state, suggesting part of the anneal effect is nonreversible through further air exposure—which likely involves improvements in contacts. In fact, a closer examination of the data in Fig. 15 shows that the degradation from post-annealing air exposure does not alter the Ohmicity of the contact—the device remains Ohmic or non-Ohmic in this intentionally introduced degradation (1 day exposure in ambient air), suggesting that the contacts remain unchanged. This again agrees with the proposed dual mechanism of both improving contact quality (not reversible) and removing surface adsorbates (reversible upon air exposure), which could be different from MoS_2 FETs fabricated with electron-beam lithography.[39]

III. CONCLUSIONS

In conclusion, we have demonstrated a new type of high-performance pristine MoS_2 FETs using a novel dry-transfer technique, in which a variety of device structures can be achieved while the MoS_2 crystal remains pristine without experiencing any wet process or chemical treatment. The quality of the as-transferred devices can be greatly enhanced by vacuum thermal annealing at increasing temperatures. We have quantified the significant improvements in devices parameters including conductance, mobility, on/off ratio, transconductance, and Ohmicity of contacts. This dry-transfer and vacuum thermal annealing approach offers a new efficient route toward high-quality MoS_2 FETs.

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[1]Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, Nat. Nanotechnol. **7**, 699 (2012).
[2]D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, ACS Nano **8**, 1102 (2014).
[3]Y. Yoon, K. Ganapathi, and S. Salahuddin, Nano Lett. **11**, 3768 (2011).
[4]R. Ganatra and Q. Zhang, ACS Nano **8**, 4074 (2014).
[5]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**, 147 (2011).
[6]B. Radisavljevic and A. Kis, Nat. Mater. **12**, 815 (2013).
[7]B. W. H. Baugher, H. O. H. Churchill, Y. Yang, and P. Jarillo-Herrero, Nano Lett. **13**, 4212 (2013).
[8]H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou, and P. D. Ye, ACS Nano **8**, 1031 (2014).
[9]H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo, and A. Javey, Nano Lett. **13**, 1991 (2013).
[10]D. Fu, J. Zhou, S. Tongay, K. Liu, W. Fan, T.-J. K. Liu, and J. Wu, Appl. Phys. Lett. **103**, 183105 (2013).
[11]B. Radisavljevic, M. B. Whitwick, and A. Kis, ACS Nano **5**, 9934 (2011).
[12]H. Wang *et al.*, IEEE Int. Electron Devices Meet. **2012**, 4.6.1.
[13]H. Wang *et al.*, Nano Lett. **12**, 4674 (2012).
[14]H. Liu, A. T. Neal, and P. D. Ye, ACS Nano **6**, 8563 (2012).
[15]H. Liu and P. D. Ye, IEEE Electron Device Lett. **33**, 546 (2012).
[16]S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, Nano Lett. **13**, 100 (2013).
[17]S. Kim *et al.*, Nat. Commun. **3**, 1011 (2012).
[18]W. S. Hwang *et al.*, Appl. Phys. Lett. **102**, 043116 (2013).
[19]W. Liu, J. Kang, W. Cao, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, IEEE Int. Electron Devices Meet. **2013**, 19.4.1.
[20]W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhrer, Appl. Phys. Lett. **102**, 042104 (2013).
[21]H. Nam, S. Wi, H. Rokni, M. Chen, G. Priessnitz, W. Lu, and X. Liang, ACS Nano **7**, 5870 (2013).
[22]S. Das and J. Appenzeller, Phys. Status Solidi RRL **7**, 268 (2013).
[23]H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, and D. Akinwande, ACS Nano **7**, 5446 (2013).
[24]J. Lee, H.-Y. Chang, T.-J. Ha, H. Li, R. S. Ruoff, A. Dodabalapur, and D. Akinwande, IEEE Int. Electron Devices Meet. **2013**, 19.2.1.
[25]D. J. Late *et al.*, ACS Nano **7**, 4879 (2013).
[26]D. Dumcenco *et al.*, e-print arXiv:1405.0129.
[27]G.-H. Lee *et al.*, ACS Nano **7**, 7931 (2013).
[28]S.-L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W.-W. Li, Y.-F. Lin, A. Aparecido-Ferreira, and K. Tsukagoshi, Nano Lett. **13**, 3546 (2013).
[29]Y.-C. Lin, C.-C. Lu, C.-H. Yeh, C. Jin, K. Suenaga, and P.-W. Chiu, Nano Lett. **12**, 414 (2012).
[30]A. G. F. Garcia, M. Neumann, F. Amet, J. R. Williams, K. Watanabe, T. Taniguchi, and D. Goldhaber-Gordon, Nano Lett. **12**, 4449 (2012).
[31]W. S. Leong, C. T. Nai, and J. T. L. Thong, Nano Lett. **14**, 3840 (2014).
[32]H. Qiu, L. Pan, Z. Yao, J. Li, Y. Shi, and X. Wang, Appl. Phys. Lett. **100**, 123104 (2012).
[33]D. Ovchinnikov, A. Allain, Y.-S. Huang, D. Dumcenco, and A. Kis, ACS Nano **8**, 8174 (2014).
[34]Z. Cheng, Q. Zhou, C. Wang, Q. Li, C. Wang, and Y. Fang, Nano Lett. **11**, 767 (2011).

[35]D. Jariwala, V. K. Sangwan, D. J. Late, J. E. Johns, V. P. Dravid, T. J. Marks, L. J. Lauhon, and M. C. Hersam, Appl. Phys. Lett. **102**, 173107 (2013).
[36]G. A. Somorjai and Y. Li, *Introduction to Surface Chemistry and Catalysis* (Wiley, New York, 2010).
[37]Y. C. Kim and M. Boudart, Langmuir **7**, 2999 (1991).
[38]V. M. Gun'ko, V. I. Zarko, B. A. Chuikov, V. V. Dudnik, Y. G. Ptushinskii, E. F. Voronin, E. M. Pakhlov, and A. A. Chuiko, Int. J. Mass Spectrom. **172**, 161 (1998).
[39]R. Yang, Z. Wang, and P. X.-L. Feng, Nanoscale **6**, 12383 (2014).